July 1993
Edition 1.0

FUJITSU

DATA SHEET

MBM28F010-12/-15/-20
1-MBIT CMOS FLASH MEMORY

DESCRIPTION

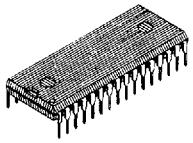
The MBM28F010 is a 1-Mbit flash memory incorporating fast erase and byte-programming functions. As in conventional EPROMs, a stuck gate transistor is used for the memory cell. The CMOS structure of the peripheral circuits provides high-speed processing and low power consumption during operation and standby.

The MBM28F010 is arranged as 128 Kbytes of 8 bits with pin assignments meeting JEDEC standards. It is available as a 32-pin plastic dual inline package (DIP), 32-pin small outline package (SOP), 32-pin plastic leadless chip carrier (PLCC) and 32-pin thin small outline package (TSOP).

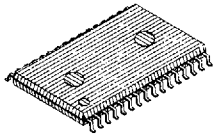
The MBM28F010 has two operation modes: read-only, and read/write. It serves as ROM in the read-only mode, and data programming and erasing by commands can be performed in the read/write mode. Data can be programmed by a quick programming algorithm at 10 µs per 1 byte, and erasing can be performed by a quick erase algorithm at 10 ms per 1 byte. Consequently, it typically takes about 2 seconds to program and erase whole the whole chip. The programming and erase timings are generated automatically in the chip.

Data can be programmed and erased by external commands, which provides data conversion in the system.

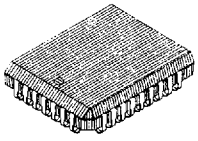
32-Pin Plastic DIP
(DIP-32P-M01)



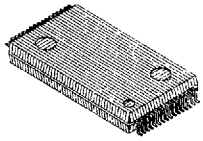
32-Pin Plastic SOP
(FPT-32P-M03)



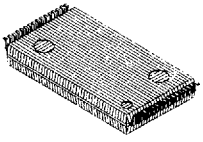
32-Pin Plastic PLCC
(LCC-32P-M02)



32-Pin Plastic TSOP
(FPT-32P-M06)



32-Pin Plastic TSOP
(FPT-32P-M07)



FEATURES

- **131,072 bytes of 8-bit organization**
- **Silicone-gate CMOS process**
- **Stuck-gate structure cell technology**
- **Quick programming: Around 2 seconds for whole chip**
  - 10 µs pulse per 1 byte
  - Quick programming algorithm
- **Quick erase: Around 2 seconds for whole chip**
  - 10 ms pulse
  - Quick erase algorithm
- **Required power voltage**
  - Read: Single 5 V
  - Program/erase: 12 V
- **Command set operation**
- **Minimum program/erase cycles: 10,000**
- **TTL level input/output**
- **Three-state output**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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FEATURES

- **Easily-expandable with output enable pin**
- **JEDEC-standard 32-pin packages**
  - DIP
  - SOP
  - PLCC
  - TSOP

PRODUCT SERIES

Model	Max. Access Time (Unit: ns)	Max. Power Consumption (Unit: mW)	
		Operation state	Standby state
MBM28F010-12	120	165	0.55
MBM28F010-15	150	165	0.55
MBM28F010-20	200	165	0.55

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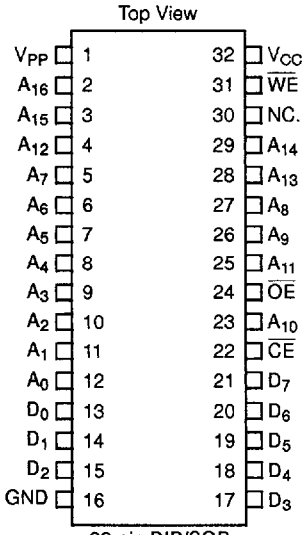
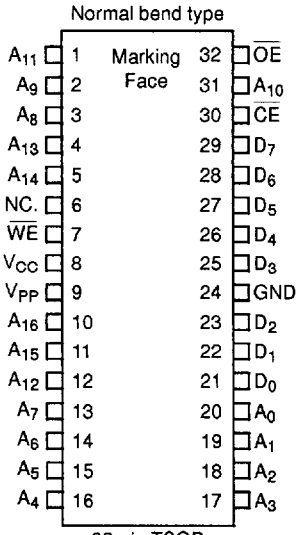
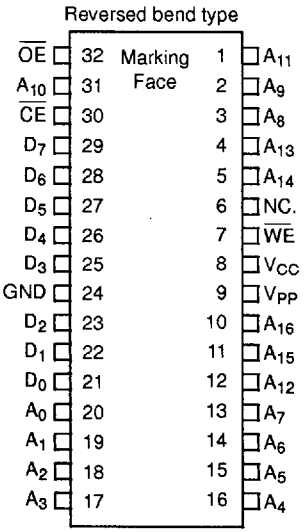
PIN ASSIGNMENT



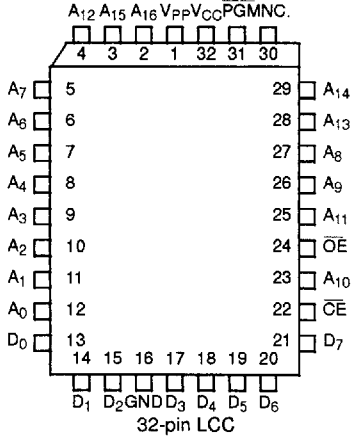
32-pin DIP/SOP
(DIP-32P-M01)
(FPT-32P-M03)



32-pin TSOP
(FPT-32P-M06)



32-pin TSOP
(FPT-32P-M07)



32-pin LCC
(LCC-32P-M02)

Symbol	Pin Name	Symbol	Pin Name
A_0 to A_{16}	Address Input	V_{PP}	Program/Erase power voltage
D_0 to D_7	Data Input/Output	V_{CC}	Power supply (+5 V)
$\overline{CE}$	Chip Enable	GND	Ground
$\overline{OE}$	Output Enable	NC.	No connection
$\overline{WE}$	Write Enable		

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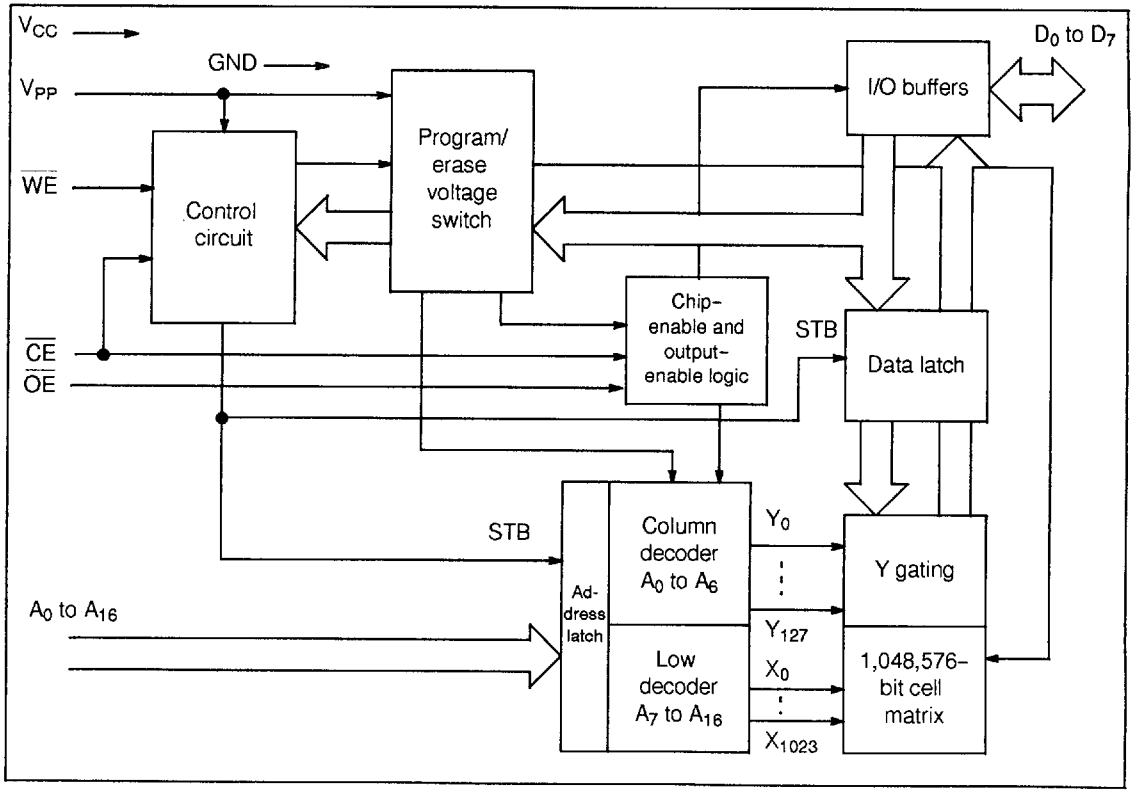
BLOCK DIAGRAM



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FUNCTIONS AND PIN CONNECTIONS

1. Read-Only Mode

Mode \ Symbol	V_{CC}	V_{PP}	Input pin	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	Output pin	Operation state
Read	V_{CC}	V_{PPL}	A_{IN}	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Standby	V_{CC}	V_{PPL}	×	×	V_{IH}	×	Hi-Z	Standby
Output Disable	V_{CC}	V_{PPL}	A_{IN}	V_{IH}	V_{IL}	×	Hi-Z	Active

Note: X can be V_{IH} or V_{IL}.

2. Read/Write Mode

Mode \ Symbol	V_{CC}	V_{PP}	Input pin	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	Output pin	Operation state
Read	V_{CC}	V_{PPH}	A_{IN}	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Standby	V_{CC}	V_{PPH}	×	×	V_{IH}	×	Hi-Z	Standby
Output Disable	V_{CC}	V_{PPH}	A_{IN}	V_{IH}	V_{IL}	×	Hi-Z	Active
Write	V_{CC}	V_{PPH}	A_{IN} (Note 2)	V_{IH}	V_{IL}	V_{IL}	D_{IN} (Note 2)	Write

Notes: 1. X can be V_{IH} or V_{IL}.
2. See the Command Definition Table.

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Command Definition Table

Command	First Bus Cycle			Second Bus Cycle		
	Bus	Address	Data	Bus	Address	Data
Data read	Write	×	#00	———	———	———
Setup Program/Program	Write	×	#40	Write	PA	PD
Program Verify	Write	×	#C0	Read	×	PVD
Setup Erase/Erase	Write	×	#20	Write	×	#20
Erase Verify	Write	EA	#A0	Read	×	EVD
Reset	Write	×	#FF	Write	×	#FF
Signature Read	Write	×	#90	Read	(Note 2)	(Note 2)

PA: Program address
PD: Program data
PVD: Program verify data
EA: Erase verify address
EVD: Erase verify data

Notes: 1. X can be V_{IH} or V_{IL}.
2. See Electronic Signature Mode.

3. Electronic Signature Mode

(1) The electronic signature is activated when 12 V +1.0/-0.5 V is applied to the address line A_9 under $V_{PP} = V_{PPL}$.

Symbol	V_{CC}	A_0	A_1 to A_{16} (Note 2)	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	D_7 to D_0
BYTE0	V_{CC}	V_{IL}	×	V_{IL}	V_{IL}	V_{IH}	#04
BYTE1	V_{CC}	V_{IH}	×	V_{IL}	V_{IL}	V_{IH}	#8F

Notes: 1. X can be V_{IH} or V_{IL}.
2. A9 = 12.0 V +1.0/-0.5 V

(2) The electronic signature is activated by command operation when $V_{PP} = V_{PPH}$.

Symbol	V_{CC}	A_0	A_1 to A_{16}	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	D_7 to D_0
BYTE0	V_{CC}	V_{IL}	×	V_{IL}	V_{IL}	V_{IH}	#04
BYTE1	V_{CC}	V_{IH}	×	V_{IL}	V_{IL}	V_{IH}	#8F

Note: X can be V_{IH} or V_{IL}.

The following table lists the electronic signatures for the MBM28F010.

	A_0	Code Data								
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Hexadecimal
Manufacturer code	V_{IL}	0	0	0	0	0	1	0	0	04
Device code	V_{IH}	1	0	0	0	1	1	1	1	8F

The electronic signatures are used to identify the manufacturer and device type for each EPROM and flash memory. Correct program voltages, conditions, and algorithms can be set automatically for each device by reading these data when using the ROM writer.

Function Descriptions

1. Read-only mode

The MBM28F010 operates as ROM in read-only mode under $V_{PP} = V_{PPL}$.

- Read — Set $\overline{CE}$ to Low level (active operation), $\overline{OE}$ to Low level and $\overline{WE}$ to High level to read data. The specified address data is output.
- Standby — Setting $\overline{CE}$ to High level enables standby operation, independent of the level of the $\overline{OE}$ and $\overline{WE}$. The output impedance is high.
- Output disable — Set $\overline{OE}$ to High level at active operation to make the data-bus impedance high. Controlling the $\overline{OE}$ and $\overline{CE}$ signals prevents system-bus competition.

2. Read/Write mode

The MBM28F010 performs data programming and erase in the read/write mode under $V_{PP} = V_{PPH}$.

- Read — Same as for read-only mode. Set $\overline{CE}$ to Low level (active state), $\overline{OE}$ to Low level and $\overline{WE}$ to High level to read data. The specified address data is output.
- Standby — Same as for read-only mode. Setting CE to High level enables standby operation, independent of the level of the $\overline{OE}$ and $\overline{WE}$. The output impedance is high.
- Output disable — Set $\overline{OE}$ to High level in the active operation to make the data-bus impedance high. Controlling the $\overline{OE}$ and CE signals prevents system-bus competition.
- Write — Set $\overline{OE}$ to High level, $\overline{CE}$ to Low level and $\overline{WE}$ to Low level to set the MBM28F010 to the write mode. The following operations are enabled by entering commands to the data pin in the write mode. The $\overline{WE}$ or $\overline{CE}$ low-level pulses can be used for the write signal. Control by the former is called $\overline{WE}$ control and by the latter, CE control.
  - Data reading: Data also can be read by writing command #00 in the write mode. The read mode is maintained until the command contents are changed. The Read mode is set automatically when V_{PP} is set to High level immediately after power-on.
  - Byte programming: Data is written in the device by repeating the write cycle twice. Write command #40 during the first cycle and then specify targeted addresses and input data in the second cycle. The addresses are latched on the falling edge of the $\overline{WE}$ pulse while the data is latched on the rising edge. Writing is accomplished automatically by an internal timer within 10 µs after data is latched.
  - Program Verify: This operation must be performed after programming (each byte). Write command #C0 and the written one-byte data is read out by the read mode operation. No address latch is needed for this operation because the addresses latched at programming are saved until program verification.
  - Erase: This operation erases whole bytes. Write command #20 twice to prevent erroneous erasing. The erase operation starts on the rising edge of the second $\overline{WE}$ pulse and is ended automatically by an internal timer within 9.5 ms.
  - Erase verify: This operation must be performed after erasing every byte. Write command #A0. The addresses to be verified are latched on the falling edge of the $\overline{WE}$ pulse. Erase verify is performed for unerased bytes or all bytes up to the last address.
  - Reset: This operation aborts the program or erase operation. When command #FF is written twice after a write or erase command is written, the current command operation is aborted and the read mode is entered. The memory contents are not changed.

3. Electronic Signature Mode

- In read-only mode — An electronic signature can be read by applying a voltage of 12 V to the A_9 address pin. The manufacturer code #04 is output to D_7 to D_0 when $A_0 = V_{IL}$ and the device code #8F is output to D_7 to D_0 when $A_0 = V_{IH}$.
- In read/write mode — An electronic signature can also be read by writing the command #90.

ABSOLUTE MAXIMUM RATINGS

(Referenced to GND)

Parameter	Symbol	Input Voltage	Unit
Operating Temperature	T_A	-25 to +85	°C
Storage Temperature Range	T_{stg}	-45 to +125	°C
Input/Output Voltage	V_{IN}, V_{OUT}	-0.6 to V_{CC} +0.6	V
Input Voltage (A9)	V_{IN}	-0.6 to +13.5	V
Programming Voltage	V_{PP}	-0.6 to +14.0	V
Supply Voltage	V_{CC}	-0.6 to +7.0	V

Note: Exceeding the ratings may affect the reliability of the device or damage the elements.

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min.	Typical	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	—	0.0	—	V
Operating Temperature	T_A	0	—	+70	°C

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ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(at recommended operating conditions)

Parameter	Symbol	Conditions	Min.	Typical	Max.	Unit
V_{CC} Operation Current	I_{CC1}	Cycle = min.	—	—	30	mA
V_{CC} Programing Current	I_{CC2}	$V_{PP} = V_{PPH}$	—	—	10	mA
V_{CC} Erase Current	I_{CC3}	$V_{PP} = V_{PPH}$	—	—	15	mA
V_{CC} Program Verify Current	I_{CC4}	$V_{PP} = V_{PPH}$	—	—	15	mA
V_{CC} Erase Verify Current	I_{CC5}	$V_{PP} = V_{PPH}$	—	—	15	mA
V_{CC} Standby Current	I_{SB1}	$\overline{CE} = V_{IH}$	—	—	1	mA
V_{CC} Standby Current	I_{SB2}	$\overline{CE} = V_{CC} \pm 0.3$ V	—	—	100	µA
V_{PP} Read/Standby Current	I_{PP1}	$V_{PP} > V_{CC}$	—	—	200	µA
V_{PP} Programming Current	I_{PP2}	$V_{PP} = V_{PPH}$	—	—	30	mA
V_{PP} Erase Current	I_{PP3}	$V_{PP} = V_{PPH}$	—	—	30	mA
V_{PP} Standby Current	I_{PP4}	$V_{PP} \leq V_{cc}$	-10	—	10	µA
Input High Voltage	V_{IH}		2.0	—	V_{CC} +0.3	V
Input Low Voltage	V_{IL}		-0.3	—	0.8	V
Input Leakage Current	I_{LI}	V_{IN} = 5.5/0 V	-10	—	10	µA
Output Leakage Current	I_{LO}	V_{OUT} = 5.5/0 V	-10	—	10	µA
Output High Voltage	V_{OH1}	I_{OH} = -400 µA	2.4	—	—	V
	V_{OH2}	I_{OH} = -100 µA	V_{CC}-0.7	—	—	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA	—	—	0.45	V
V_{CC} Erase/Write Lock Voltage	V_{LKO}		2.5	—	—	V
V_{PP} during read-only operation	V_{PPL}		0.0	—	6.5	V
V_{PP} during read/write operation	V_{PPH}		11.4	—	12.6	V

Notes:
1. The power switching order is not specified for V_{PP} and V_{CC}.
2. V_{PP} must not exceed 13.5 V including overshoot.
3. The reliability of the device is affected by plugging in or out when $V_{PP} = V_{PPH}$.

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2. AC Characteristics

(1) Read-only operations

(at recommended operating conditions)

Parameter	Symbol	Conditions	MBM28F010-12			MBM28F010-15			MBM28F010-20			Unit
			Min.	Typical	Max.	Min.	Typical	Max.	Min.	Typical	Max.	
Address Access Time	t_{ACC}	$\overline{CE} = \overline{OE} = V_{IL}$	—	—	120	—	—	150	—	—	200	ns
$\overline{CE}$ to Output Delay Time	t_{CE}	$\overline{OE} = V_{IL}$	—	—	120	—	—	150	—	—	200	ns
$\overline{OE}$ to Output Delay Time	t_{OE}	$\overline{CE} = V_{IL}$	—	—	50	—	—	55	—	—	60	ns
$\overline{CE}$ or $\overline{OE}$ to Output Float Delay	t_{DF}	$\overline{CE}$, $\overline{OE} = V_{IL}$	0	—	30	0	—	30	0	—	30	ns
Address to Output Hold Time	t_{OH}	$\overline{CE} = \overline{OE} = V_{IL}$	0	—	—	0	—	—	0	—	—	ns
$\overline{CE}$ or $\overline{OE}$ to Output Active	t_{DV}		0	—	—	0	—	—	0	—	—	ns

(2) Programming/Erase Operations ($\overline{WE}$ control)

(at recommended operating conditions)

Parameter		Symbol	Min.	Typical	Max.	Unit
Write Cycle Time	MBM28F010-12	t_{WC}	120	—	—	ns
	MBM28F010-15		150	—	—	ns
	MBM28F010-20		200	—	—	ns
Address Setup Time		t_{AS}	0	—	—	ns
Address Hold Time		t_{AH}	60	—	—	ns
Data Setup Time		t_{DS}	50	—	—	ns
Data Hold Time		t_{DH}	10	—	—	ns
Write Recovery Time		t_{RE}	6	—	—	µs
Read Recovery Time		t_{GH}	0	—	—	µs
$\overline{CE}$ Setup Time		t_{CS}	20	—	—	ns
$\overline{CE}$ Hold Time		t_{CH}	0	—	—	ns
Write Pulse Width		t_{WP}	60	—	—	ns
Write Pulse Width High		t_{WPH}	20	—	—	ns
Programming Duration*		t_{WHWH1}	10	—	—	µs
Erasure Duration*		t_{WHWH2}	9.5	—	—	ms
Programming Pulse Cycle		X	—	—	—	Cycles
Erase Cycle		S	—	—	—	Cycles
V_{PP} Setup Time		t_{VPEL}	1.0	—	—	µs

* The internal timer terminates the Write/Erase operations, thereby eliminating the need for a maximum specification.

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(3) Programming/Erase Operations ($\overline{CE}$ control)

(at recommended operating conditions)

Parameter		Symbol	Min.	Typical	Max.	Unit
Write Cycle Time	MBM28F010-12	t_{WC}	120	—	—	ns
	MBM28F010-15		150	—	—	ns
	MBM28F010-20		200	—	—	ns
Address Setup Time		t_{AS}	0	—	—	ns
Address Hold Time	MBM28F010-12/-15	t_{AH}	80	—	—	ns
	MBM28F010-20		95	—	—	ns
Data Setup Time		t_{DS}	50	—	—	ns
Data Hold Time		t_{DH}	10	—	—	ns
Write Recovery Time		t_{RE}	6	—	—	µs
Read Recovery Time		t_{GH}	0	—	—	µs
$\overline{WE}$ Setup Time		t_{WS}	0	—	—	ns
$\overline{WE}$ Hold Time		t_{WH}	0	—	—	ns
Write Pulse Width	MBM28F010-12/-15	t_{WP}	70	—	—	ns
	MBM28F010-20		80	—	—	ns
Write Pulse Width High		t_{WPH}	20	—	—	ns
Programming Duration*		t_{EHEH1}	10	—	—	µs
Erasure Duration*		t_{EHEH2}	9.5	—	—	ms
Programming Pulse Cycle		X	—	—	25	Cycles
Erase Cycle		S	—	—	3000	Cycles
V_{PP} Setup Time		t_{VPEL}	1.0	—	—	µs

* The internal timer terminates the Write/Erase operations, thereby eliminating the need for a maximum specification.

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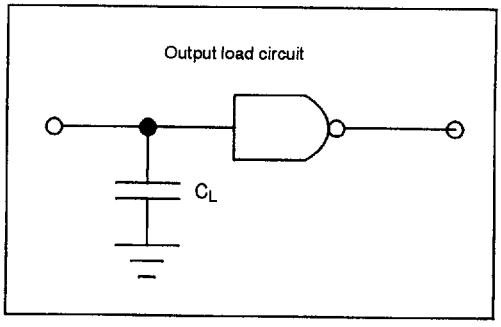
3. CAPACITANCE

(TA = +25°C, f = 1 MHz)

Parameter	Symbol	Conditions	Min.	Typical	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	—	TBD	TBD	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	—	TBD	TBD	pF

4. AC Characteristics Test Conditions

- Input pulse voltage: 0.45 V to 2.4 V
- Input pulse rise time: ≤ 20 ns
- Input pulse fall time: ≤ 20 ns
- Input timing reference voltage: 0.8 V and 2.0 V
- Output timing reference voltage: 0.8 V and 2.0 V
- Output load: 1TTL + C_L (100 pF)



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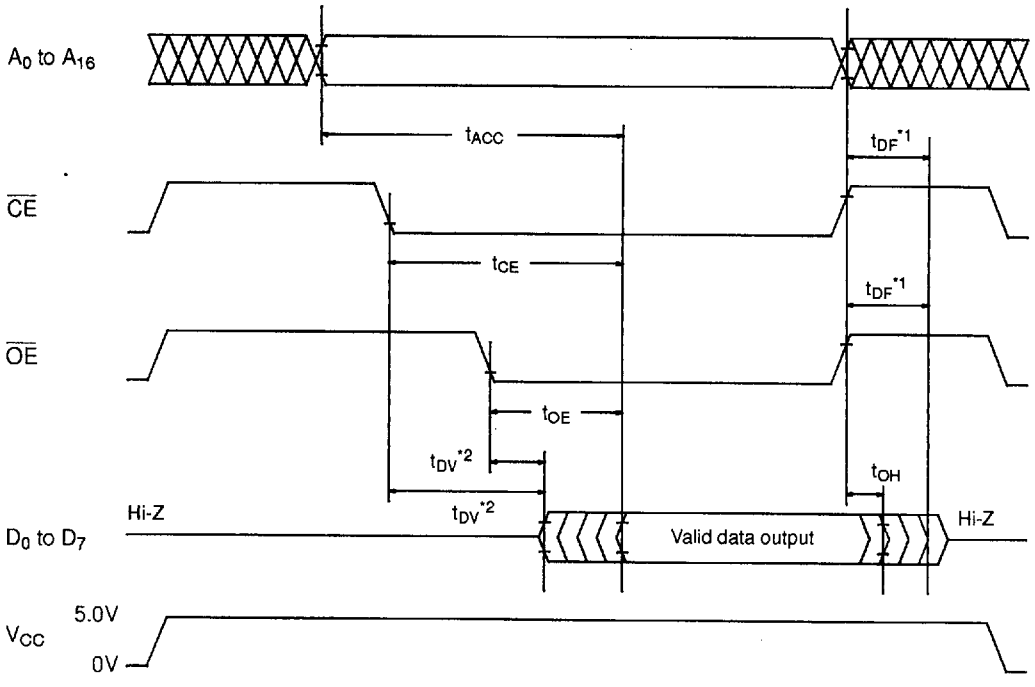
TIMING DIAGRAMS

1. Read Cycle



Note 1: t_{DF} is specified by either of the $\overline{CE}$ or $\overline{OE}$ signal rising first.

Note 2: t_{DV} is specified by either of the $\overline{CE}$ or $\overline{OE}$ signal falling last.

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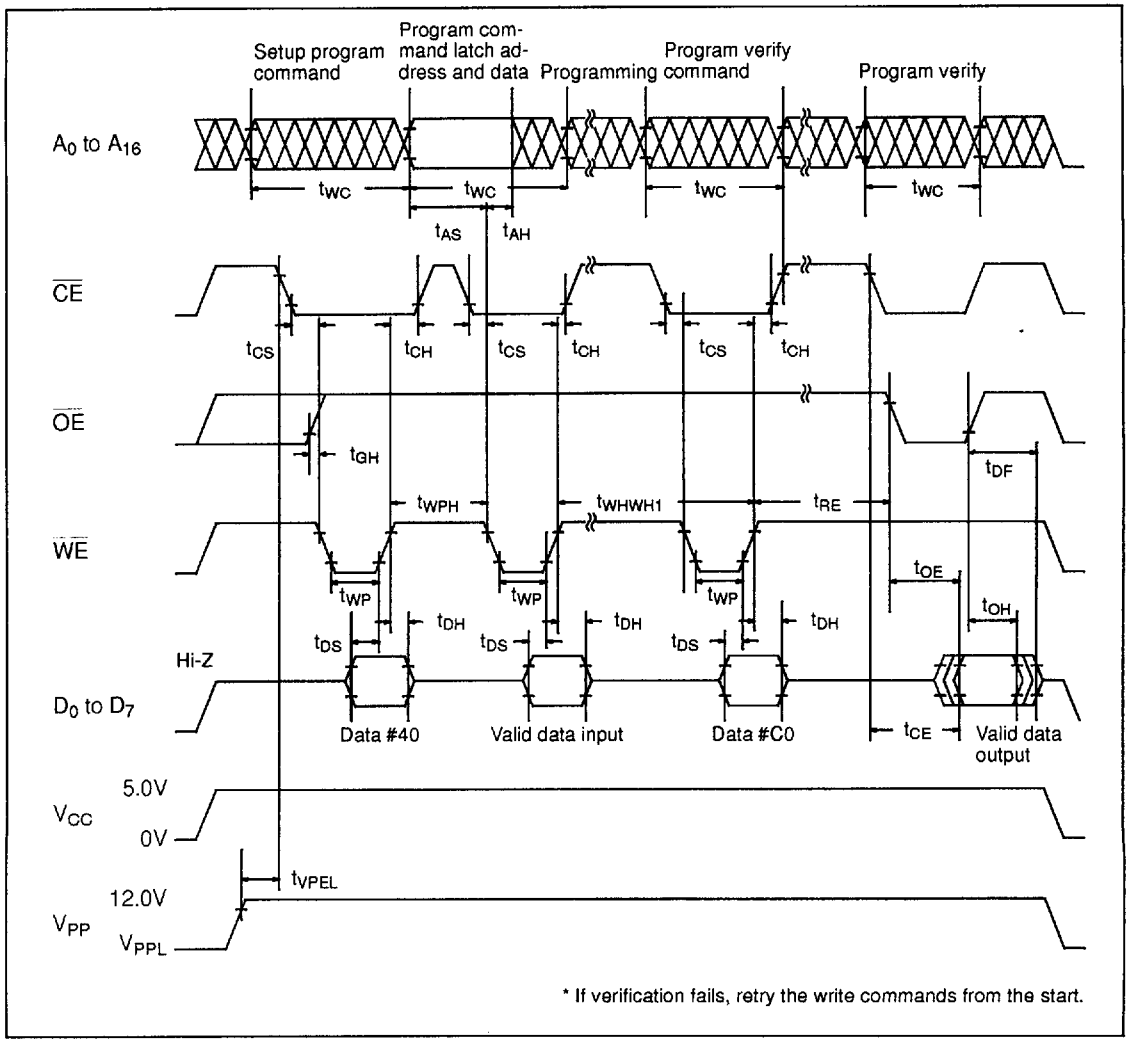
2. Programming Cycle ($\overline{WE}$ Control)



* If verification fails, retry the write commands from the start.

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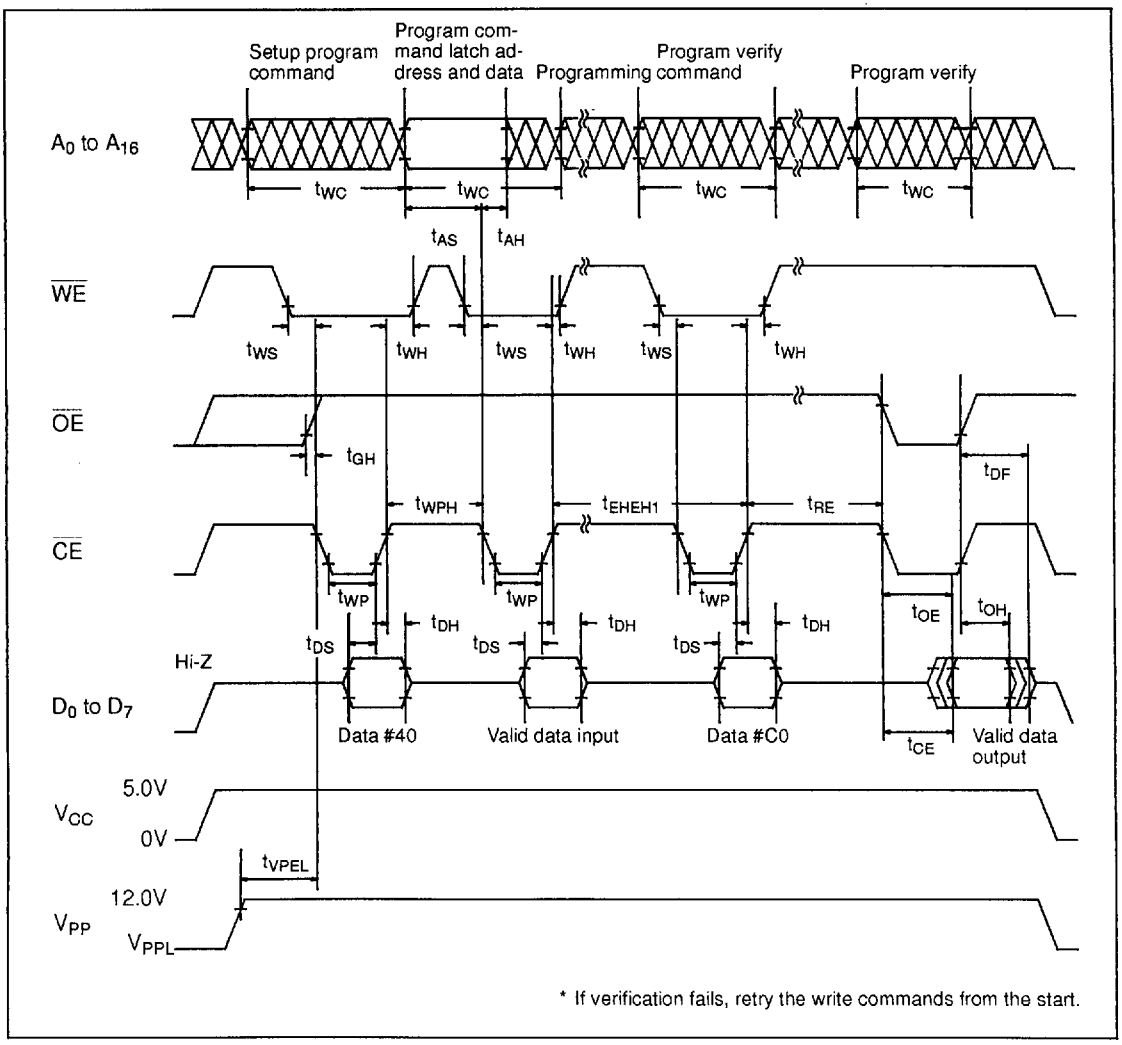
3. Programming Cycle ($\overline{CE}$ Control)



* If verification fails, retry the write commands from the start.

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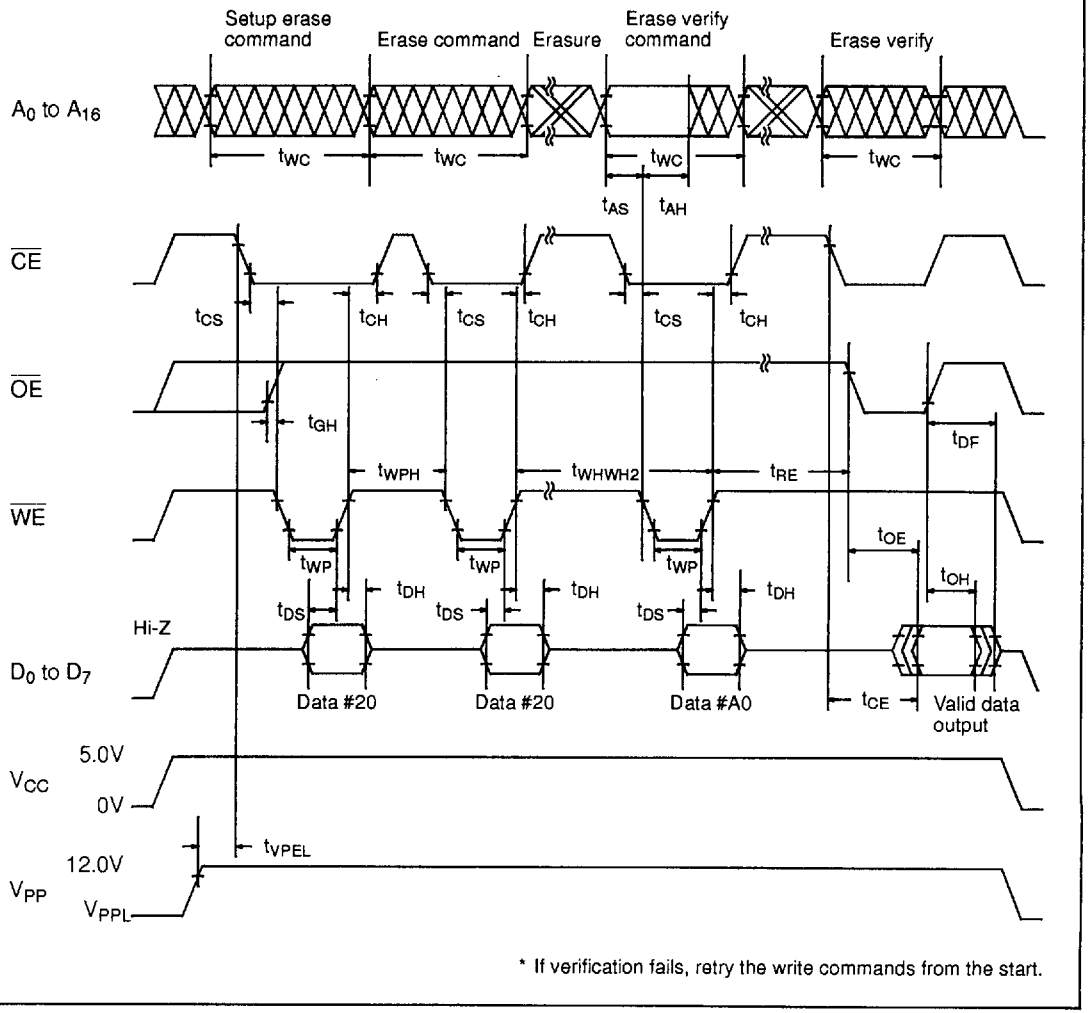
4. Erase Cycle ($\overline{WE}$ Control)



* If verification fails, retry the write commands from the start.

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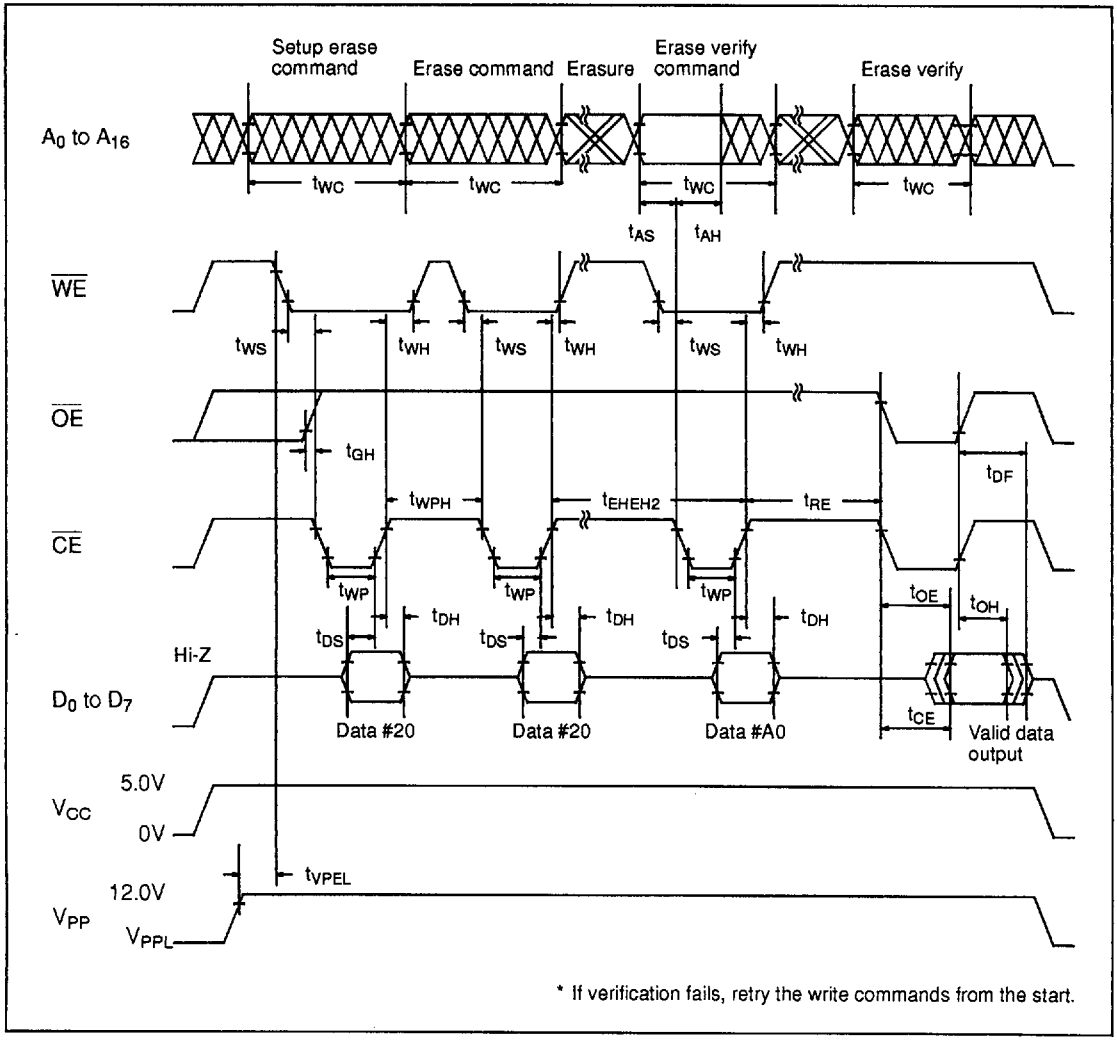
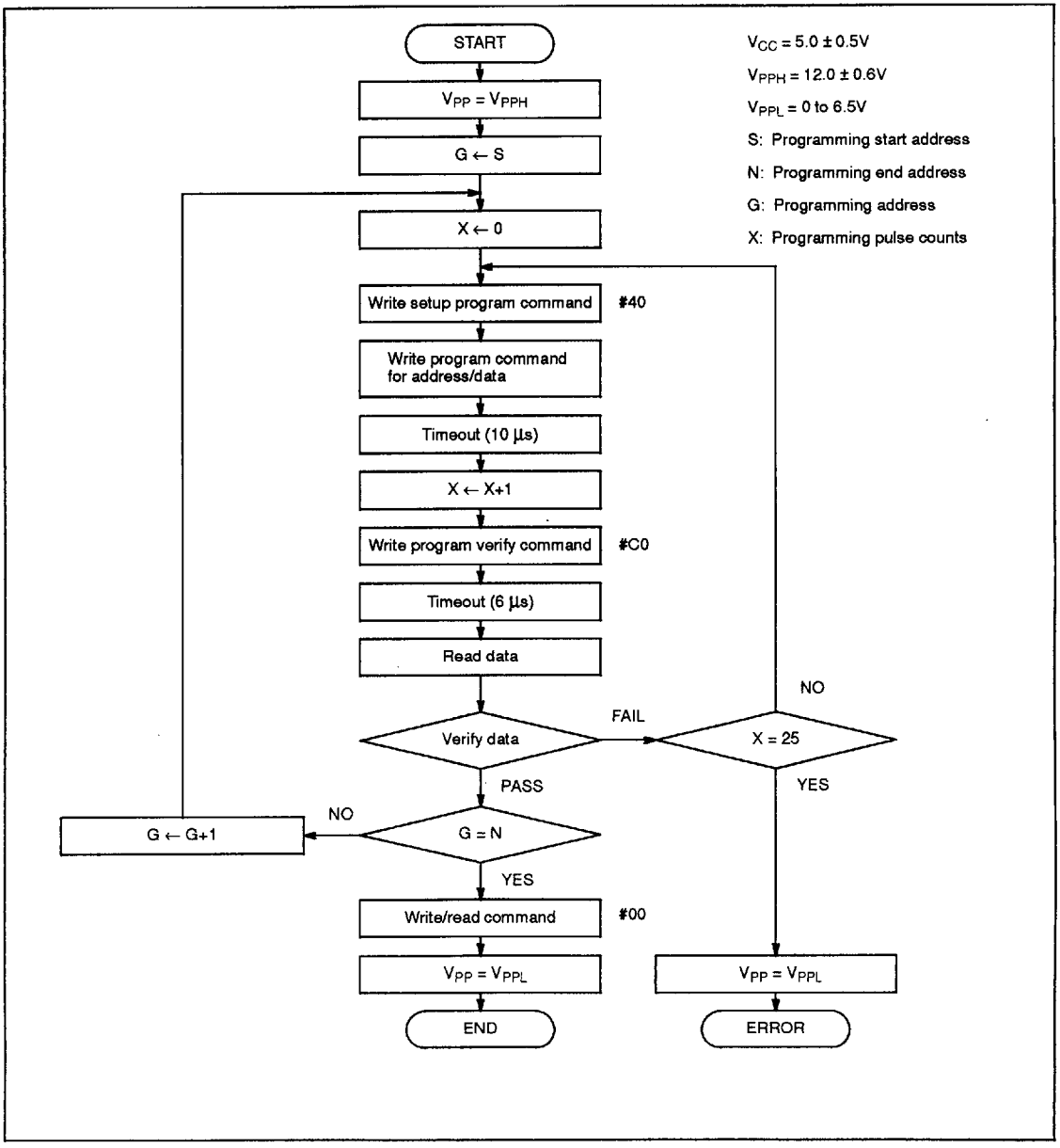
5. Erase Cycle ($\overline{CE}$ Control)



* If verification fails, retry the write commands from the start.

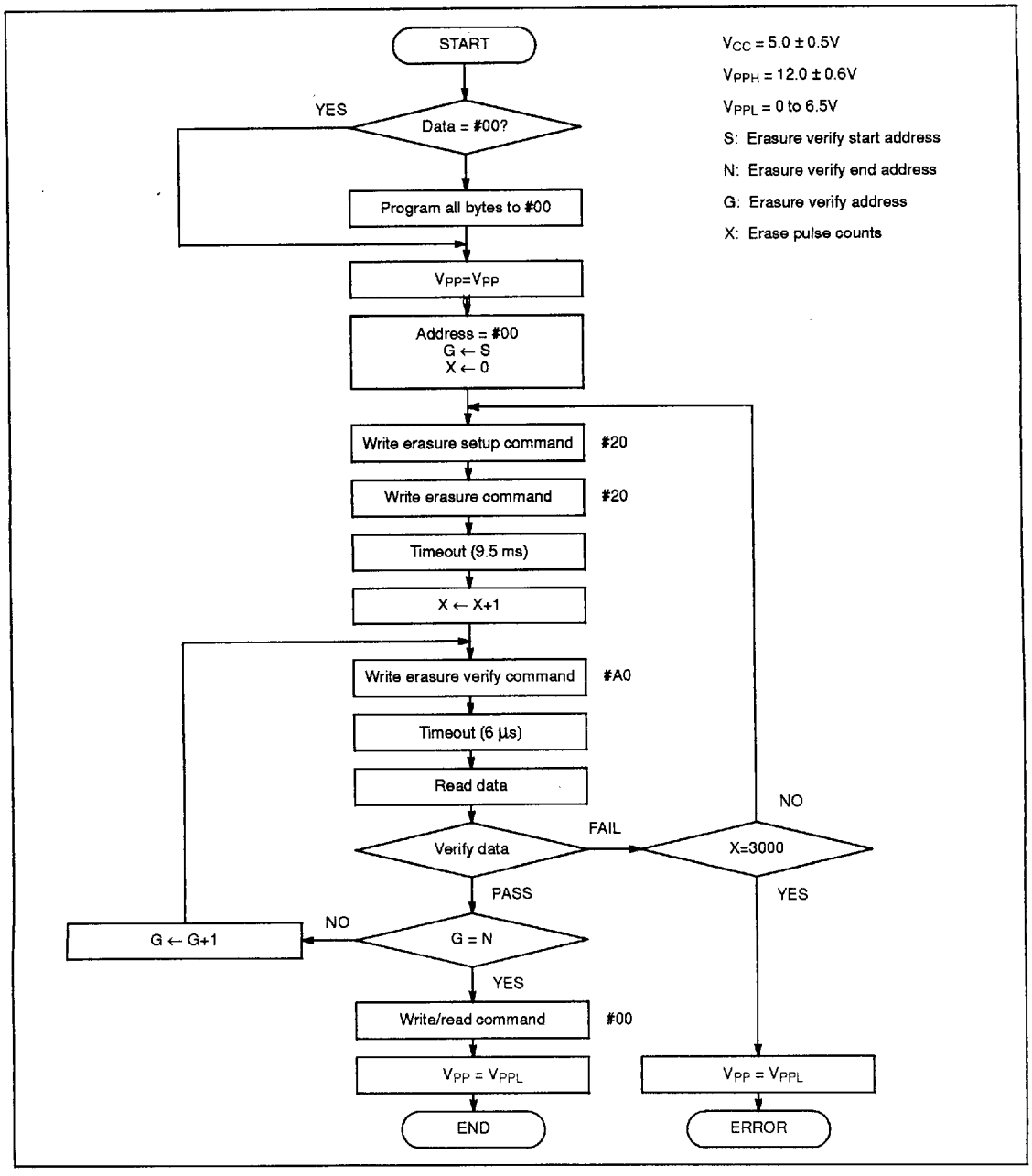
ALGORITHM FLOWCHARTS

1. Programming operation



6

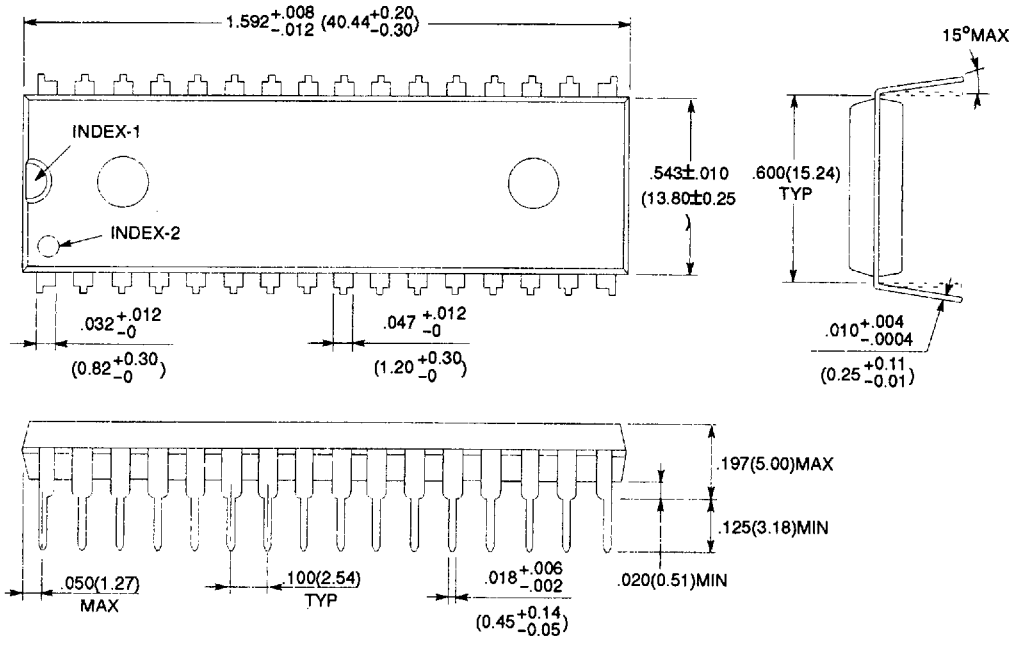
2. Erase Operation



6

PACKAGE DIMENSIONS

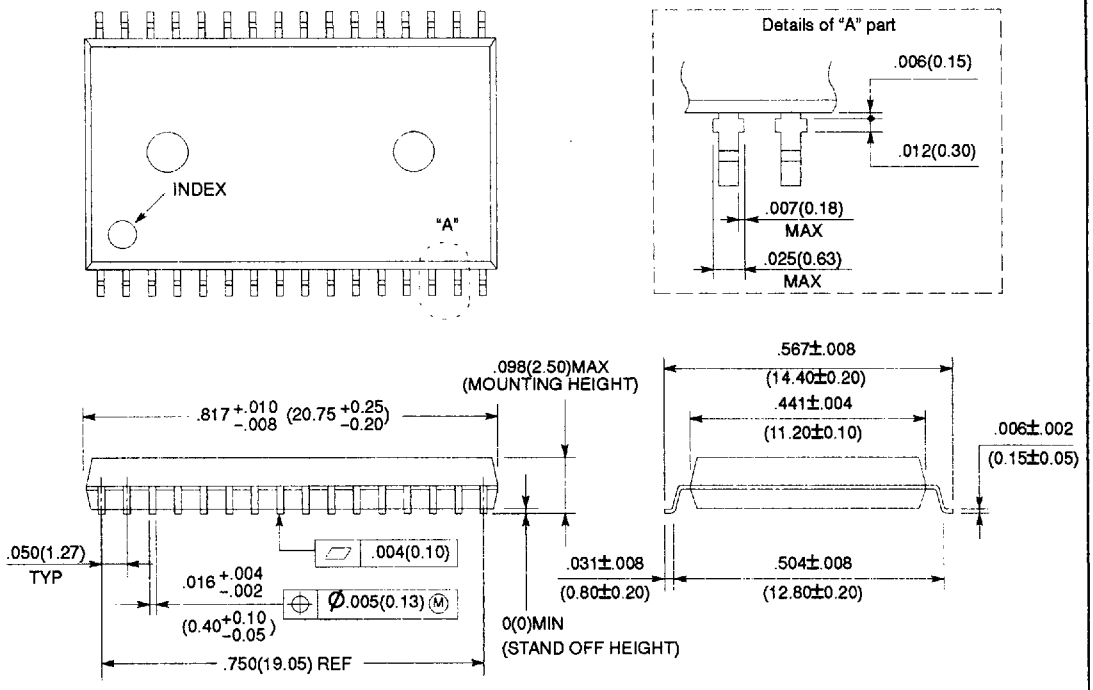
32-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-32P-M01)



Dimensions in
inches (millimeters)

6

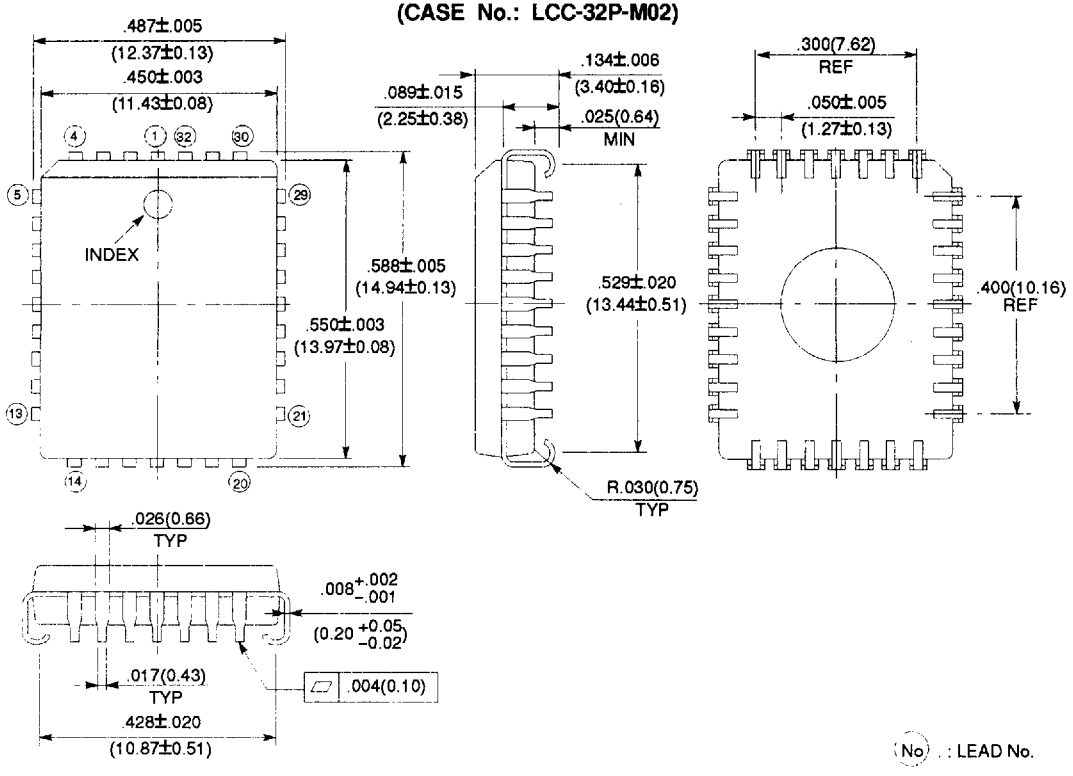
32-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-32P-M03)



Dimensions in
inches (millimeters)

6

32-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-32P-M02)

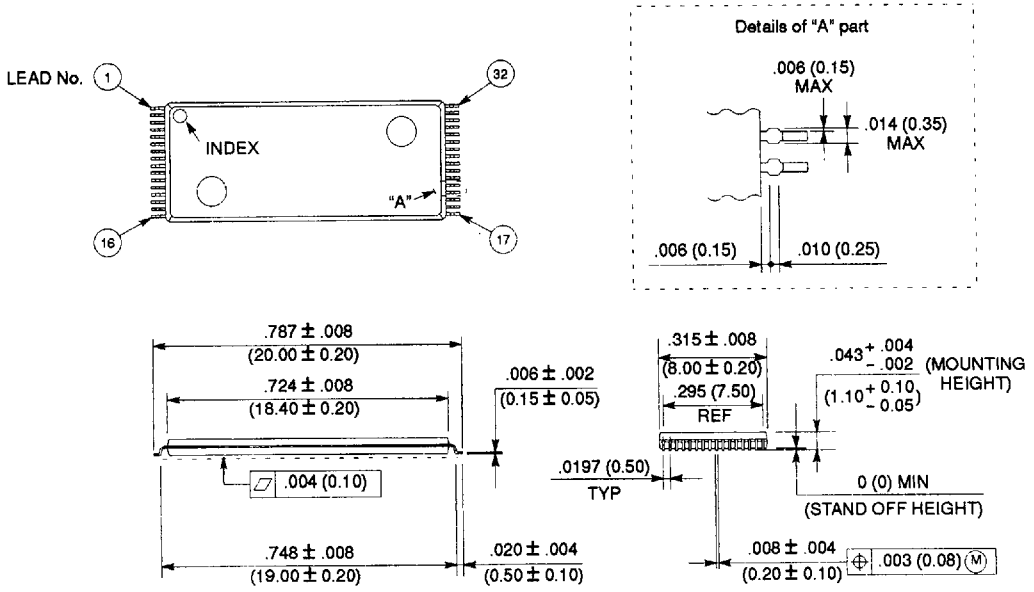


(No) : LEAD No.

Dimensions in
inches (millimeters)

6

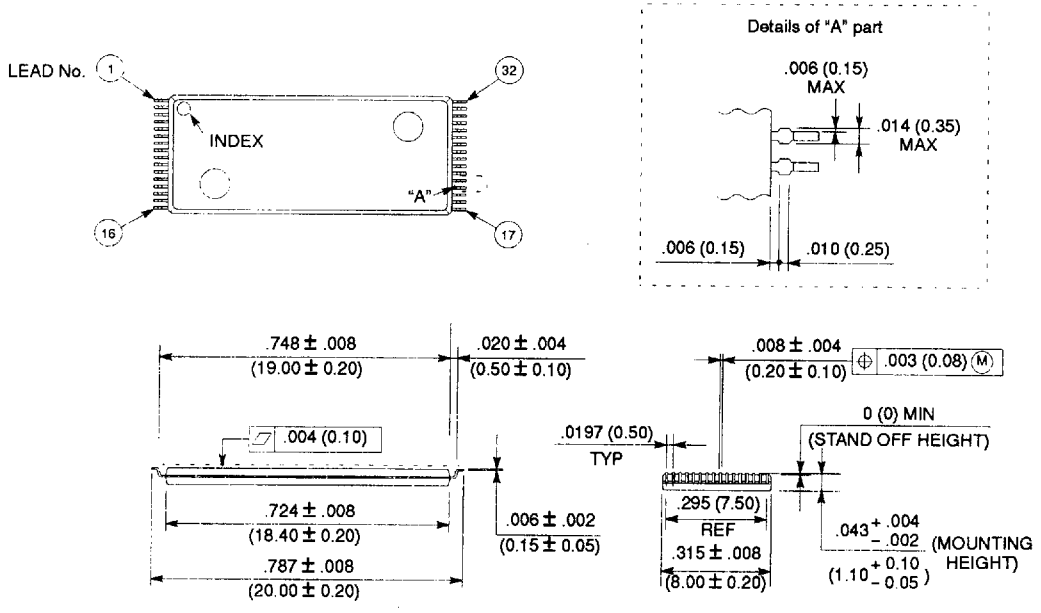
32-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-32P-M06)



Dimensions in inches (millimeters)

6

32-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-32P-M07)



Dimensions in
inches (millimeters)

6