National Semiconductor

ADVANCE INFORMATION

74LVT16500
3.3V ABT 18-Bit Universal Bus Transceivers with TRI-STATE® Outputs

General Description

The LVT16500 consist of eighteen universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock ($\overline{CLKAB}$ and $\overline{CLKBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CLKAB}$ is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the high-to-low transition of $\overline{CLKAB}$. Output-enable OEAB is active-high. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, and $\overline{CLKBA}$. The output enables are complementary (OEAB is active high and $\overline{OEBA}$ is active low).

The transceivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16500 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/ +64 mA
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 16500
- Latch-up performance exceeds 500 mA

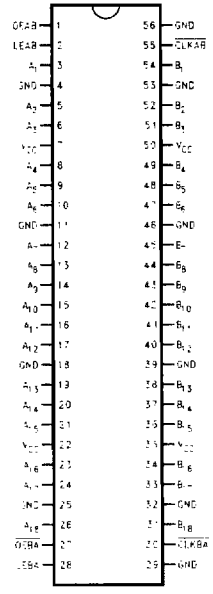
Pin Description

Pin Names	Description
A_0–A_{17}	Data Register A Inputs/TRI-STATE Outputs
B_0–B_{17}	Data Register B Inputs/TRI-STATE Outputs
$\overline{CLKAB}$, $\overline{CLKBA}$	Clock Pulse Inputs
LEAB, LEBA	Latch Enable Inputs
OEAB, $\overline{OEBA}$	Output Enable Inputs

	SSOP EIAJ	TSSOP
Order Number	74LVT16500MEA 74LVT16500MEAX	74LVT16500MTD 74LVT16500MTDX
NS Package Number	MS56A	MTD56

Connection Diagram

Pin Assignment for SSOP and TSSOP



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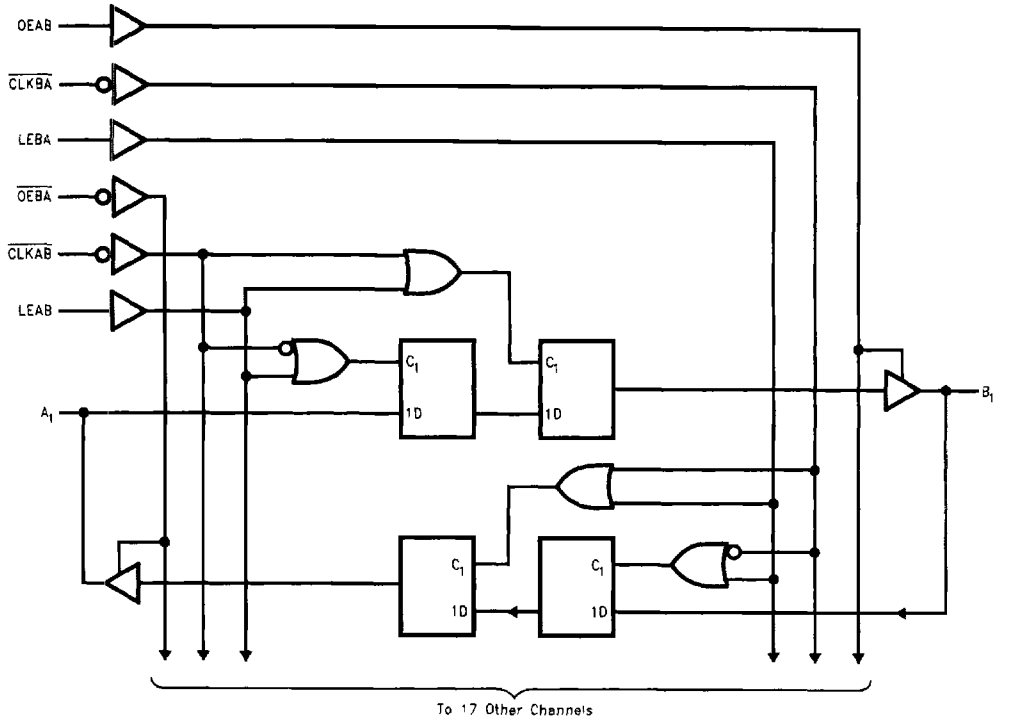
Logic Diagram



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Function Table†

Inputs				Output
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and $\overline{CLKBA}$.

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that $\overline{CLKAB}$ was low before LEAB went low.