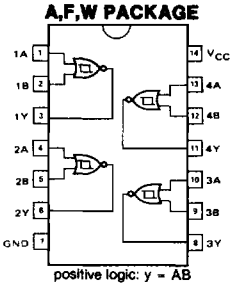
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L=15pF R_L=400Ω			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time				
t_{PLH} Low-to-high		15	22	ns
t_{PHL} High-to-low		15	22	

Load circuit and typical waveforms are shown at the front of section.

PIN CONFIGURATION

A,F,W PACKAGE



positive logic: y = AB

HYSTERESIS VS. TEMPERATURE-TYPICAL VALUES

PARAMETER		54/74 -55°C	+25°C	+125°C	UNIT
V_{T+}	Positive going threshold	1.5	1.7	2	V
V_{T-}	Negative going threshold	0.6	0.9	1.1	V
	Hysteresis	0.4	0.8		V

SPEED/PACKAGE AVAILABILITY

54 F,W 74 A

DATA SELECTOR/MULTIPLEXER W/3-STATE OUTPUTS 54/74251

SPEED/PACKAGE AVAILABILITY

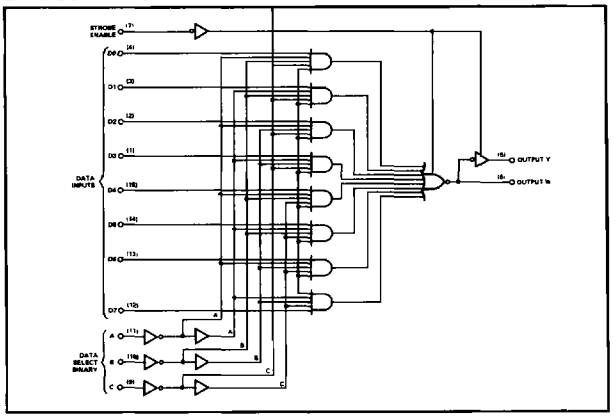
54LS F,W 74LS B
54S F,W 74S B

DESCRIPTION

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources and feature a strobe-controlled three-state output. The strobe must be at a low logic level to enable these devices. The three-state outputs permit up to 49 54LS251 and 129 74LS251 outputs to be connected to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

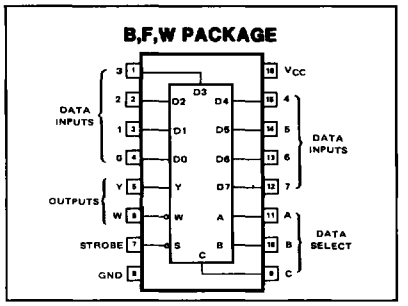
To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time.

BLOCK DIAGRAM



PIN CONFIGURATION

B,F,W PACKAGE



TRUTH TABLE

INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	S		
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high logic level, L = low logic level
X = irrelevant, Z = high impedance (off)
D0, D1 . . . D7 = the level of the respective D input

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C - PAGE 212

TEST CONDITIONS			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
t_{PLH} Low-to-high	A,B,C (4 levels)	Y		29	45		12	18	ns
t_{PHL} High-to-low				28	45		13	19.5	
t_{PLH} Low-to-high	A,B,C (3 levels)	W		20	33		10	15	
t_{PHL} High-to-low				21	33		9	13.5	
t_{PLH} Low-to-high	Any D	Y		17	28		8	12	
t_{PHL} High-to-low				18	28		8	12	
t_{PLH} Low-to-high	Any D	W		10	15		4.5	7	
t_{PHL} High-to-low				9	15		4.5	7	
Output enable time									
t_{ZH} To high level	Strobe	Y		17	27		13	19.5	
t_{ZL} To low level				26	40		14	21	
t_{ZH} To high level	Strobe	W		17	27		13	19.5	
t_{ZL} To low level				24	40		14	21	
Output disable time				C_L=5pf R_L=2kΩ					
t_{HZ} From high level	Strobe	Y		30	45		5.5	8.5	
t_{ZL} From low level				15	25		9	14	
t_{HZ} From high level	Strobe	W		30	45		5.5	8.5	
t_{LZ} From low level				15	25		9	14	

LOGIC