

February 1985

OBJECTIVE
SPECIFICATIONS

Dual J-K Negative-Edge-Triggered Flip-Flops with Preset and Clear

Features

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5\text{V}$
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
74HCTLS: -40°C to $+85^{\circ}\text{C}$
54HCTLS: -55°C to $+125^{\circ}\text{C}$

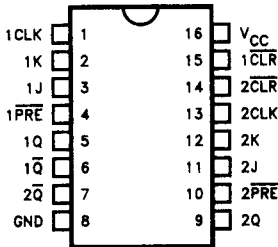
Description

These parts consist of two negative-edge-triggered J-K flip-flops with independent J, K, preset, clear and clock inputs and complementary outputs. The J-K inputs at each flip-flop are enabled when the clock goes high. The input data are transferred to the outputs on the negative-going edge of the clock pulse, provided the setup requirements have been met.

Fabricated using Zytrex's proprietary ICE-MOS process, these devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Pin Configuration



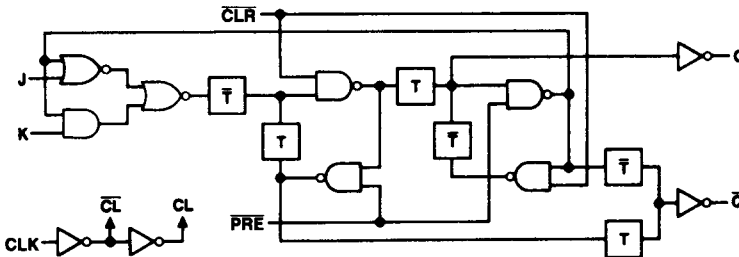
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Function Table

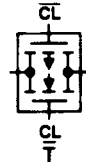
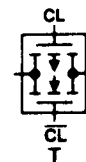
Inputs					Outputs	
PRE	CLR	CLK	J	K	Q	Q-bar
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q ₀	Q ₀ -bar
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q ₀	Q ₀ -bar

*Both outputs will remain high as long as PRE and CLR are low, but the output states are unpredictable if PRE and CLR go high simultaneously.

Logic Diagrams



0079-2



0079-3

Absolute Maximum Ratings*

Supply Voltage Range, V_{CC} -0.5V to 7V
 DC Input Diode Current, I_{IK}
 ($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) ± 20 mA
 DC Output Diode Current, I_{OK}
 ($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) ± 20 mA
 Continuous Output Current Per Pin, I_O
 ($-0.5V < V_O < V_{CC} + 0.5V$) ± 35 mA
 Continuous Current Through
 V_{CC} or GND pins ± 125 mA
 Storage Temperature Range, T_{STG} .. -65°C to +150°C
 Power Dissipation Per Package, P_D † 500 mW

*Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:

Plastic Package (N): -12 mW/°C from 65°C to 85°C
 Ceramic Package (J): -12 mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V
 DC Input & Output Voltages*, V_{IN} , V_{OUT} 0V to V_{CC}
 Operating Temperature
 Range ZX74HCTLS: -40°C to +85°C
 ZX54HCTLS: -55°C to +125°C
 Input Rise & Fall Times, t_r , t_f Max 500 ns

*Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC Electrical Characteristics ($V_{CC} = 5V \pm 10\%$ Unless Otherwise Specified)

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$		74HCTLS	54HCTLS	Unit
			Typ	Guaranteed Limits			
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	$T_A = -55^\circ\text{C to } +125^\circ\text{C}$		
V_{IH}	Minimum High-Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low-Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_O = -20 \mu\text{A}$ $I_O = -4 \text{mA}$	V_{CC} 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_O = 20 \mu\text{A}$ $I_O = 4 \text{mA}$ $I_O = 8 \text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND		± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu\text{A}$		4.0	40.0	80.0	μA

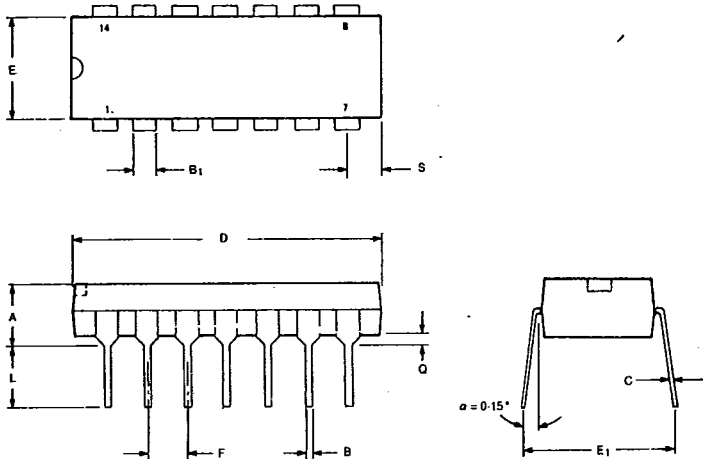
AC Electrical Characteristics (Input $t_r, t_f \leq 6$ ns), HCTLS112A

Symbol	Parameter	Conditions†	T _A = 25°C V _{CC} = 5.0V		74HCTLS	54HCTLS	Unit	
					T _A = -40°C to +85°C V _{CC} = 5.0V ± 10%	T _A = -55°C to +125°C V _{CC} = 5.0V ± 10%		
			Typ		Guaranteed Limits			
f _{max}	Maximum Clock Frequency	C _L = 50 pF	40	30	25	21	MHz	
t _{PLH}	Maximum Propagation Delay, CLK to Q or \bar{Q}		15	20	25	30	ns	
t _{PHL}	Maximum Propagation Delay, PRE or \bar{CLR} to Q or \bar{Q}		15	20	25	30	ns	
t _{PLH}	Minimum Setup Time before CLK ↓		J or K	10	13	17	20	ns
t _{PHL}			\bar{PRE} or \bar{CLR} Inactive	10	13	17	20	ns
t _h	Minimum Hold Time, J or K after CLK ↓			0	0	0	0	ns
t _w	Minimum Pulse Width	CLK High or Low	10	13	17	20	ns	
		\bar{PRE} or \bar{CLR} Low	10	13	17	20		
C _{IN}	Maximum Input Capacitance		5				pF	
C _{PD}	Power Dissipation Capacitance*	(per flip-flop)	40				pF	

*C_{PD} determines the no-load dynamic power dissipation: P_D = C_{PD} V_{CC}² f + I_{CC} V_{CC}.
†For AC switching test circuits and timing waveforms see section 2.

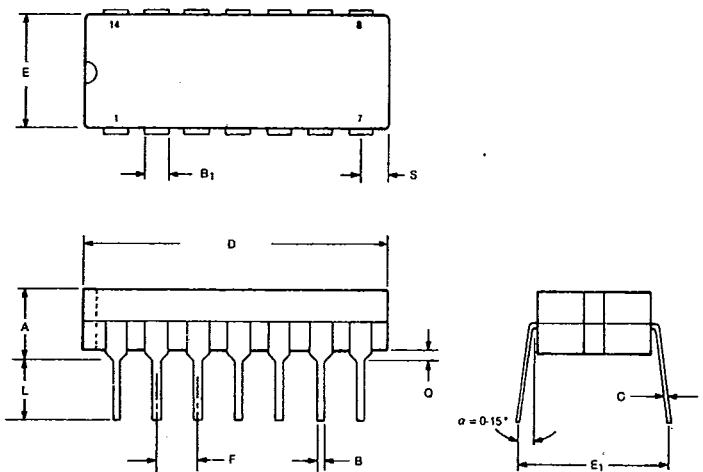
14-Pin Packages

Plastic Package



DIM	Millimeters		Inches	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
B	0.38	0.58	0.015	0.023
B ₁	1.40	1.78	0.055	0.070
C	0.20	0.38	0.008	0.015
D	18.16	19.56	0.715	0.770
E	6.10	7.49	0.240	0.295
E ₁	7.62	10.03	0.300	0.395
F	2.54		0.100	
L	3.18	4.19	0.125	0.165
Q	0.51	1.02	0.020	0.040
S	1.91	2.29	0.075	0.090

Ceramic Package

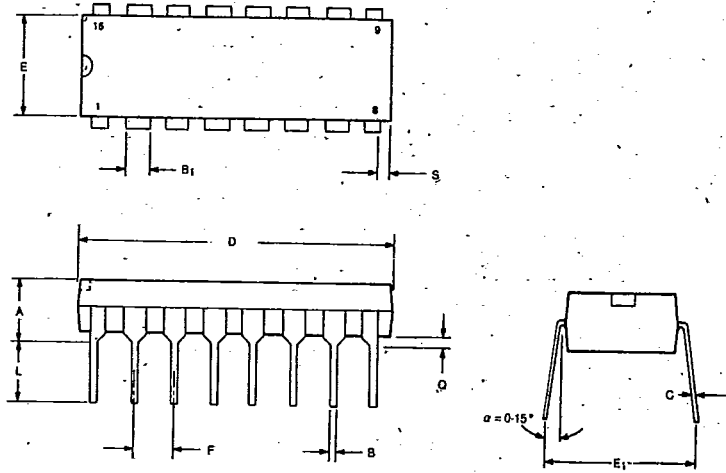


DIM	Millimeters		Inches	
	Min	Max	Min	Max
A	—	5.08	—	0.200
B	0.38	0.58	0.015	0.023
B ₁	1.40	1.78	0.055	0.070
C	0.20	0.38	0.008	0.015
D	19.05	19.94	0.750	0.785
E	6.10	7.49	0.240	0.295
E ₁	7.62	10.03	0.300	0.395
F	2.54		0.100	
L	3.18	4.19	0.125	0.165
Q	0.51	1.02	0.020	0.040
S	1.91	2.29	0.075	0.090

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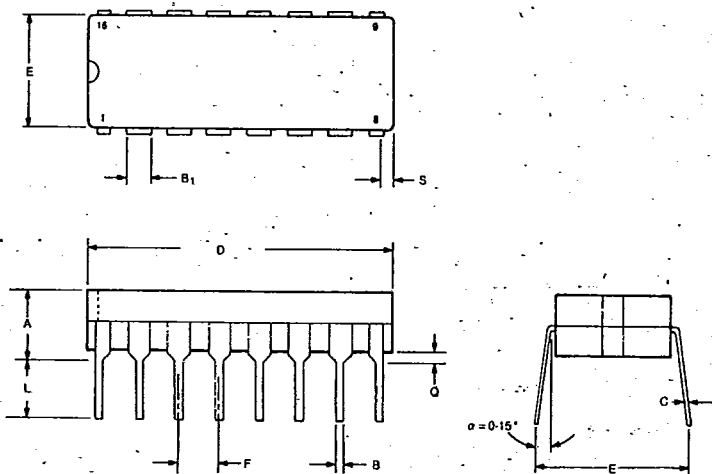
16-Pin Packages

Plastic Package



DIM	Millimeters		Inches	
	Min	Max	Min	Max
A	3.81	4.32	0.150	0.170
B	0.38	0.58	0.015	0.023
B ₁	1.40	1.78	0.055	0.070
C	0.20	0.38	0.008	0.015
D	19.05	19.94	0.750	0.785
E	6.10	7.49	0.240	0.295
E ₁	7.62	8.89	0.300	0.350
F	2.54		0.100	
L	3.18	4.19	0.125	0.165
Q	0.51	1.02	0.020	0.040
S	1.91	2.29	0.075	0.090

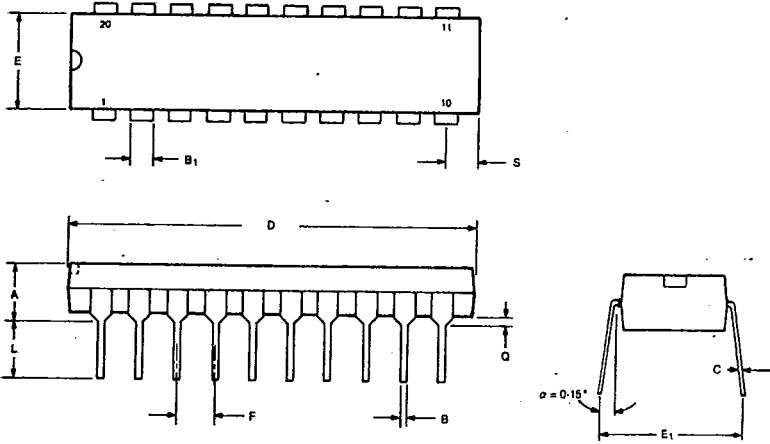
Ceramic Package



DIM	Millimeters		Inches	
	Min	Max	Min	Max
A	—	5.08	—	0.200
B	0.38	0.58	0.015	0.023
B ₁	1.40	1.78	0.055	0.070
C	0.20	0.38	0.008	0.015
D	19.05	19.94	0.750	0.785
E	6.10	7.49	0.240	0.295
E ₁	7.62	10.03	0.300	0.395
F	2.54		0.100	
L	3.18	4.19	0.125	0.165
Q	0.51	1.02	0.020	0.040
S	1.51	1.14	0.020	0.045

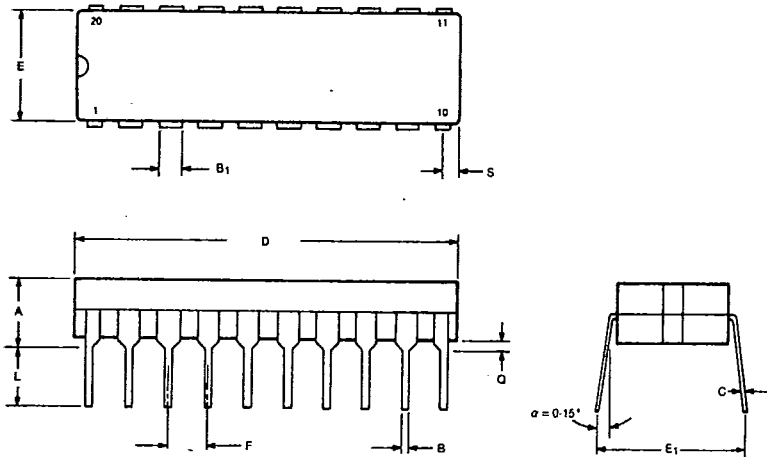
20-Pin Packages

Plastic Package



DIM	Millimeters		Inches	
	Min	Max	Min	Max
A	4.06	5.08	0.160	0.200
B	0.38	0.53	0.015	0.021
B ₁	1.14	1.52	0.045	0.060
C	0.20	0.38	0.008	0.015
D	25.65	27.18	1.010	1.070
E	6.10	6.60	0.240	0.260
E ₁	7.77	8.89	0.306	0.350
F	2.54		0.100	
L	3.30	4.01	0.130	0.158
Q	0.38	0.89	0.015	0.035
S	1.85	1.93	0.073	0.076

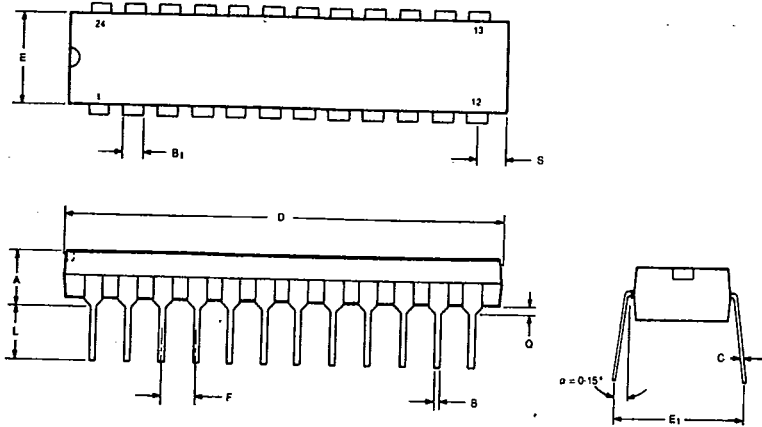
Ceramic Package



DIM	Millimeters		Inches	
	Min	Max	Min	Max
A	4.06	5.08	0.160	0.200
B	0.38	0.53	0.015	0.021
B ₁	1.14	1.52	0.045	0.060
C	0.20	0.38	0.008	0.015
D	25.78	25.93	1.015	1.021
E	6.10	6.60	0.240	0.260
E ₁	7.77	7.98	0.306	0.314
F	2.54		0.100	
L	3.73	4.01	0.147	0.158
Q	0.38	0.89	0.015	0.035
S	0.51	1.14	0.020	0.045

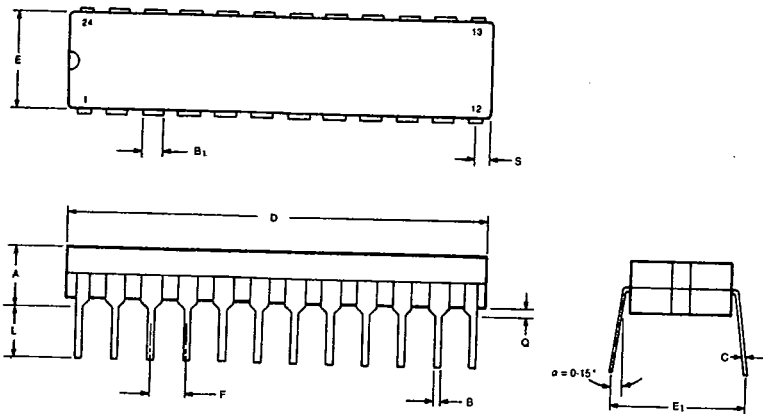
24-Pin Packages

Plastic Package



DIM	Millimeters		Inches	
	Min	Max	Min	Max
A	4.06	5.08	0.160	0.200
B	0.38	0.53	0.015	0.021
B ₁	1.14	1.52	0.045	0.060
C	0.20	0.38	0.008	0.015
D	31.24	32.13	1.230	1.265
E	6.10	6.60	0.240	0.260
E ₁	7.77	8.89	0.306	0.350
F	2.54		0.100	
L	3.30	4.01	0.130	0.158
Q	0.38	0.89	0.015	0.035
S	0.51	1.14	0.020	0.045

Ceramic Package



DIM	Millimeters		Inches	
	Min	Max	Min	Max
A	4.06	5.08	0.160	0.200
B	0.38	0.53	0.015	0.021
B ₁	1.14	1.52	0.045	0.060
C	0.20	0.38	0.008	0.015
D	31.50	32.64	1.240	1.285
E	7.24	7.75	0.285	0.305
E ₁	7.77	7.98	0.306	0.314
F	2.54		0.100	
L	3.73	4.01	0.147	0.158
Q	0.508	1.778	0.020	0.070
S	1.85	1.93	0.073	0.076