MX8327

MOTHERBOARD CLOCK GENERATOR

FEATURES

- Clock generator for PC/AT and PS/2 system
- Mask programmable CPU clock up to 80 MHz
- Provide seven clock outputs (14.318 MHz, 8/24/48 MHz, CPU clock, CPU clock/2, 12X serial port clock)
- Built-in PLL for low-phase jitter, driven by a 14.318 MHz crystal clock.
- Glitch-free switching for CPU clock
- Provide Tri-State and Power-down control
- Smooth CPU clock period change while switching frequencies
- 20 PDIP and SSOP (209 mil body) package

GENERAL DESCRIPTION

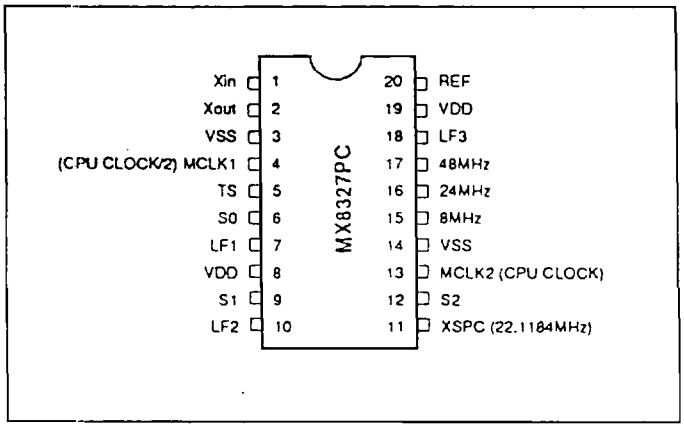
The MX8327 is a CMOS motherboard clock generator used in PC system to eliminate the need of additional crystal oscillators and to reduce overall system cost.

The MX8327 is capable of generating four sets of clock outputs, a 14.31818 MHz master clock output, 8/24/48 MHz peripherial clocks, a 12X serial clock (22.1184 MHz), and programable CPU clocks. If different CPU clock is required, MXIC can make a custom version by changing one mask layer.

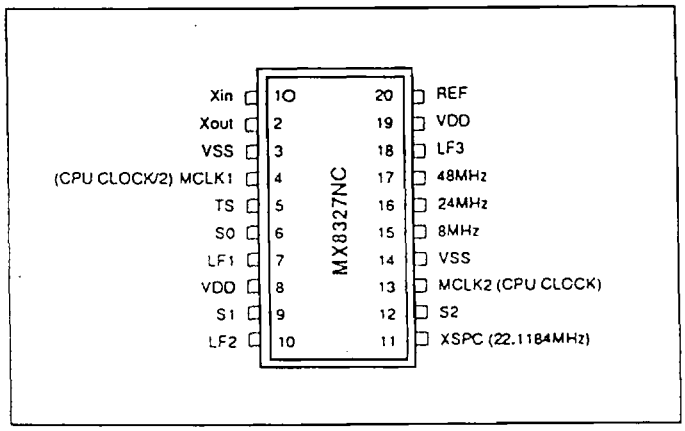
All outputs, VCOs, and oscillator can be turned off or tri-state to reduce the power consumption.

PIN CONFIGURATIONS

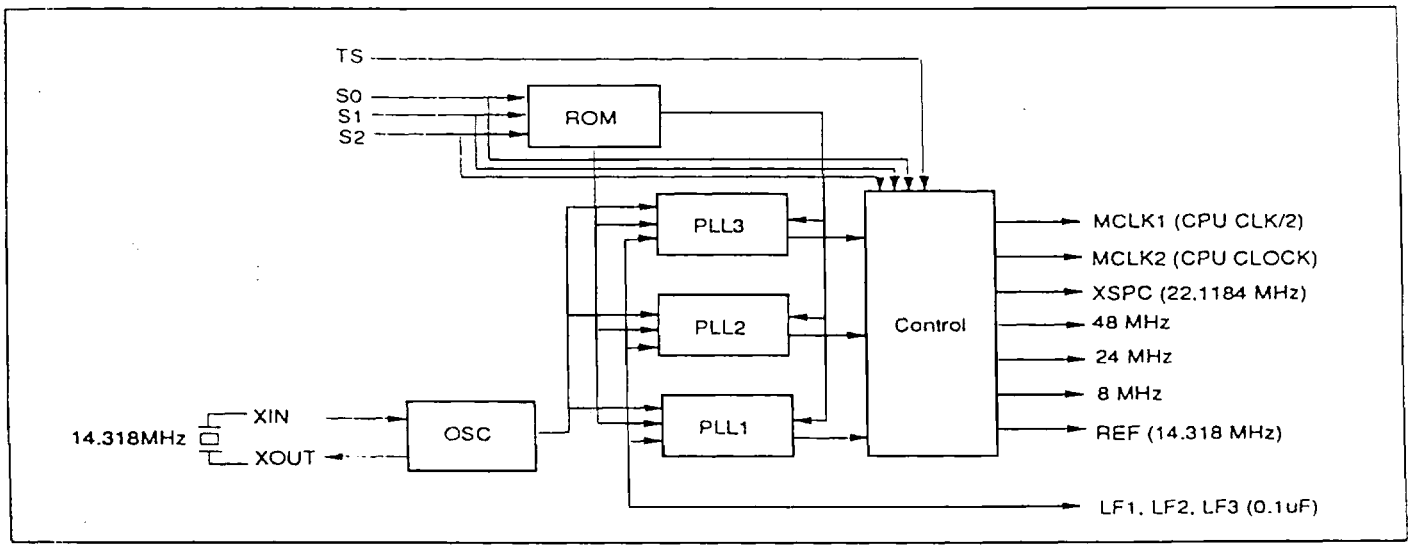
20 PDIP



20 SSOP



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN TYPE	PIN NUMBER	DESCRIPTION
XIN	I	1	Crystal pin or reference clock input.
XOUT	O	2	Crystal pin. No connection if reference clock is used.
VSS		3, 14	Ground pins.
MCLK1	O	4	CPU clock/2 output.
TS	I	5	Tri-state control pin. When high, all output except REF are tri-state. When chip is in power-down mode and TS is high, the REF output goes to tri-state and oscillator is turned off. See Table 2. Internal pull-down resistor.
S0, S1, S2	I	6, 9, 12	Frequency select pins. Internal pull-up resistors. See Table 1 for frequencies selection.
LF1, LF2, LF3		7, 10, 18	Loop filter capacitors. A 0.1uF capacitor should be connected from each pin to ground to form the loop filters.
XSPC	O	11	22.1184 MHz clock output.
MCLK2	O	13	CPU clock output.
8 MHz	O	15	8 MHz output.
24 MHz	O	16	24 MHz output.
48 MHz	O	17	48 MHz output.
REF	O	20	14.318 MHz output.
VDD	I	8, 19	+5V POWER PIN.

FUNCTIONAL DESCRIPTION

The MX8327 motherboard clock generator is an integrated circuit of phase-locked loop frequency synthesizer. The MX8327 consists of three sets of independent phase-locked loop and uses 14.318 MHz external crystal to generate all clock signals. REF pin provides the crystal oscillation frequency (14.31818 MHz). The first PLL generates 8 MHz, 24 MHz, and 48 MHz peripheral clocks. The second PLL generates 12X serial port clock (22.1184 MHz). The third PLL generates CPU clock and CPU clock divided by two output. The CPU clock can be programmable through three select pins (S0, S1, S2) based on the frequency table shown on Table 1.

A PLL consists of feedback and input dividers, phase frequency comparator (PFC), charge pump, voltage-controlled oscillator (VCO), and loop filter. In this chip, the loop filter is formed by internal resistor and an external 0.1 uF capacitor. The loop filter capacitors connected to the chip should be as close as possible to reduce noise susceptibility.

The MX8327 has tri-state control and power-down mode to reduce power consumption. The detailed operation of tri-state and power-down mode is shown on Table 2. When TS is high, all output except REF are in the tri-state. When chip is in the power-down mode, VCOs are turned off and all output except REF are in the low state. When chip is in the static mode, all output are in the tri-state, and VCOs and oscillator are turned off.

A proper resonant crystal should be connected between XIN and XOUT. Crystal range from 10 MHz to 25MHz is recommended. However, a 14.31818 MHz crystal is usually used. The frequencies shown on Table 1 is based on 14.31818 MHz reference clock. If a different reference clock is used, the table should be scaled proportionally. The reference clock can also be suppied by external clock. In this case, the XIN should be connected to the reference clock and XOUT be disconnected.

TABLE 1: CPU FREQUENCY SELECTION TABLE

INPUTS			OUTPUTS	
S2	S1	S0	MCLK2	MCLK1
0	0	0	60.0000 MHz	30.0000 MHz
0	0	1	32.0053 MHz	16.0026 MHz
0	1	0	33.3333 MHz	16.6566 MHz
0	1	1	40.0000 MHz	20.0000 MHz
1	0	0	50.0000 MHz	25.0000 MHz
1	0	1	66.6666 MHz	33.3333 MHz
1	1	0	80.0000 MHz	40.0000 MHz
1	1	1	Power Down	Power Down

TABLE 2: TRI-STATE AND POWER-DOWN CONTROLS

INPUTS				OUTPUTS				
TS	S2	S1	S0	ALL REFQ. OUTPUT	REF	OSCILATOR	VCOs	MODE
0	0	x	x	On	On	On	On	Normal
0	x	0	x	On	On	On	On	Normal
0	x	x	0	On	On	On	On	Normal
0	1	1	1	Low	On	On	Off	Power Down
1	0	x	x	Hi-Z	On	On	On	Tri-state except REF
1	x	0	x	Hi-Z	On	On	On	Tri-state except REF
1	x	x	0	Hi-Z	On	On	On	Tri-state except REF
1	1	1	1	Hi-Z	Hi-Z	Hi-Z	Off	Static

ABSOLUTE MAXIMUM RATINGS

RATING	VAULE
Storage Temperature	-8.5°C to 150°C
Applied Input Voltage	-0.5V to VDD + 0.5V
Applied Output Voltage	-0.5V to VDD + 0.5V
Supply Voltage	-0.5V to 7V
Operating Temperature	0 to 70°C
Power Dissipation	0.5 Watts

NOTICE :
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE :
Specifications contained within the following tables are subject to change.

DC CHARACTERISTICS (TA = 0°C to 70°C, VCC = 5V ± 10%)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
VDD	Supply Voltage	4.5	5	5.5	V	
IDD	Supply Current		TBD		mA	No load, running at 80 MHz
VOL	Output Low Voltage			0.4	V	All outputs, IOL = 12 mA
VOH	Output High Volyage	2.4			V	All outputs, IOH = -12 mA
RPU	Pull up Resistor		80K		Ohms	
RPD	Pull down Resistor		80K		Ohms	

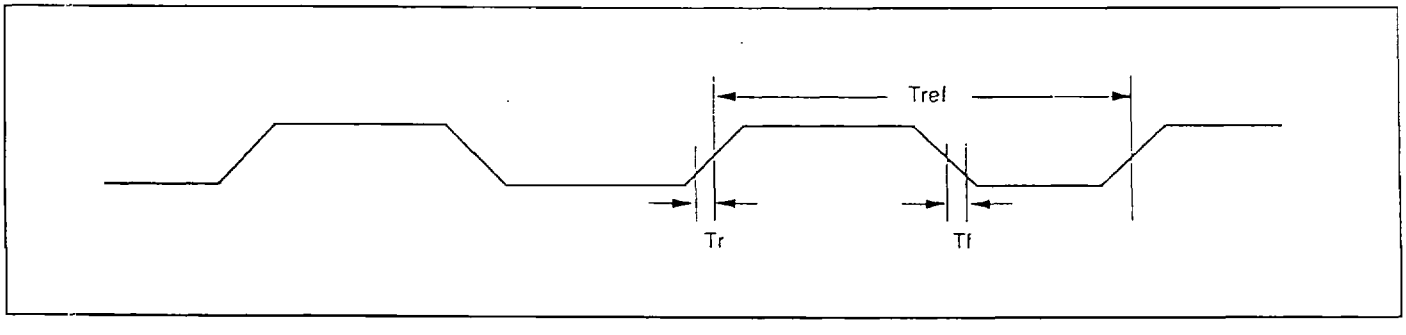
CAPACITANCE (TA = 25°C, f = 1.0 MHz)(Sampled only)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance		8		pF	
COUT	Out Capacitance		8		pF	

AC CHARACTERISTICS (TA = 0°C to 70°C, VCC = 5V ± 10%)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Tr	Rise Time (0.8V- 2.0V)			2	ns	25 pF load
Tf	Fall Time (2.0V-0.8V)			2	ns	25 pF load
Dt	Output Duty Cycle	45/55	50/50	55/45		25pF load
Fref	Reference Clock Frequency	14.318		MHz		
Tref	Reference Clock Period		69.8412		ns	

WAVEFORMS

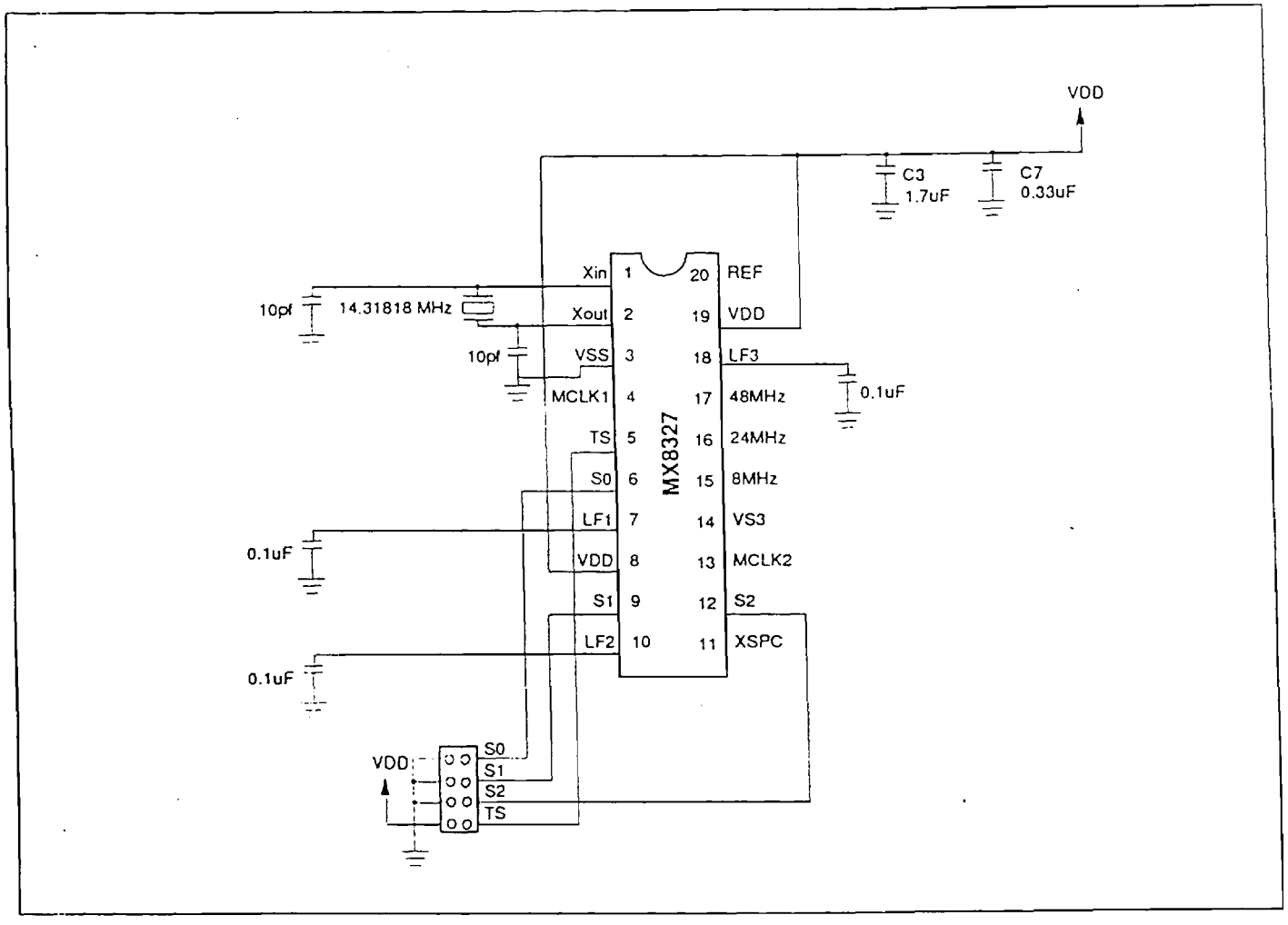


ORDERING INFORMATION

PLSTIC PACKAGE

PART NO.	PACKAGE
MX8327PC	20-PIN PDIP
MX8327NC	20-PIN SSOP

RECOMMENDED EXTERNAL CIRCUIT

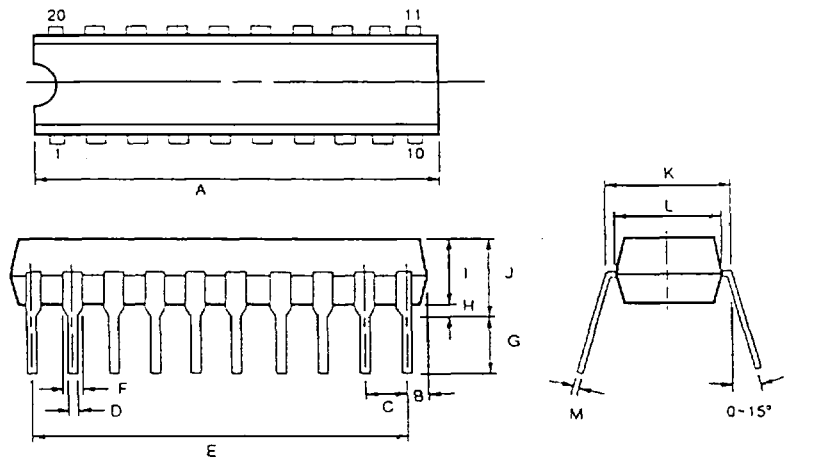


Note : S0, S1, S2 internal pull-up
TS internal pull-down

PACKAGE INFORMATION
20-PIN DIP OUTLINE DIMENSIONS

ITEM	MILIMETERS	INCHES
A	26.42 [max.]	1.04 [max.]
B	1.778 [REF]	.070 [REF]
C	2.54 [TP]	.100 [TP]
D	.457 [Typ.]	.018 [Typ.]
E	22.86 [min.]	.9 [min.]
F	1.524 [Typ.]	.060 [max.]
G	3.302 ± .25	.130 ± .010
H	.635 [REF]	.025 [REF]
I	3.556 ± .12	.140 ± .005
J	4.572[REF]	.18 [REF]
K	7.61 ± .25	.300 ± .010
L	6.48 ± .25	.255 ± .010
M	.25 [Typ.]	.010 [Typ.]

Note: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at a maximum material condition.



PACKAGE INFORMATION
20-PIN SSOP OUTLINE DIMENSIONS

ITEM	MILIMETERS	INCHES
A	7.33 [max.]	.289 [max.]
B	.51 [REF]	.020 [REF]
C	.65 [REF]	.026 [REF]
D	.3 [Tp.]	.012 [Tp.]
E	.05 [min.]	.002 [min.]
F	1.99 [max.]	.078 [max.]
G	1.73 ± .05	.068 ± .002
H	7.8 ± .15	.307 ± .006
I	5.3 ± .1	.209 ± .004
J	1.25 ± .25	..049 ± .01
K	.20[Typ.]	.008 [Typ.]
L	.75	.030

Note: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at a maximum material condition.