

HIGH-PERFORMANCE PRODUCTS

Description

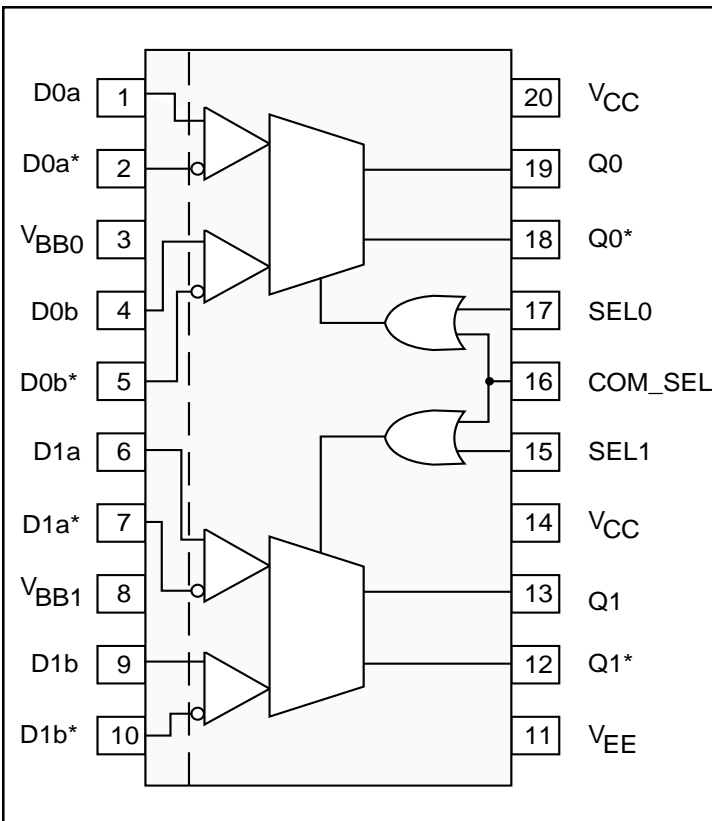
The SK10/100EL56W is a Dual 2:1 Differential Multiplexer. It is fully differential and compatible with MC100EL56 and MC100LVEL56. This device features both individual and common select inputs to address both data path and random logic applications.

Multiple V_{BB} outputs are provided for single-ended use or DC bias for AC coupling to the device. V_{BB} is an output pin and should be used as a bias for the SK10/100EL56W as its current source/sink capability is limited. Whenever used, the V_{BB} output pins should be bypassed to V_{CC} via 0.01 μF capacitors. When both differential inputs are left open, the D input will pull down to V_{EE} , and the D* input will bias at $V_{CC}/2$, forcing the Q output low.

Features

- Extended Supply Voltage Range ($V_{EE} = -5.5\text{V}$ to -3.0V , $V_{CC} = 0\text{V}$) or $V_{CC} = +3.0\text{V}$ to 5.5V , $V_{EE} = 0\text{V}$)
- High Bandwidth Output Transition
- 500 ps Propagation Delay (typical)
- V_{BB} Output
- Internal Input Pulldown Resistors
- New Differential Input Common Mode Range
- Fully Compatible with MC100EL56 and MC100LVEL56
- ESD Protection of $>4000\text{V}$
- Industrial Temperature Range: -40°C to $+85^\circ\text{C}$
- Available in 20 Pin SOIC Package

Functional Block Diagram



Pin Names

Pin	Function
D0a, D0a*, D0b, D0b*	Differential Data Inputs
SEL0, SEL1	Individual Select Inputs
COM_SEL	Common Select Inputs
Q0, Q1	True Outputs
Q0*, Q1*	Inverted Outputs
V_{BB0} , V_{BB1}	Output Reference Voltages

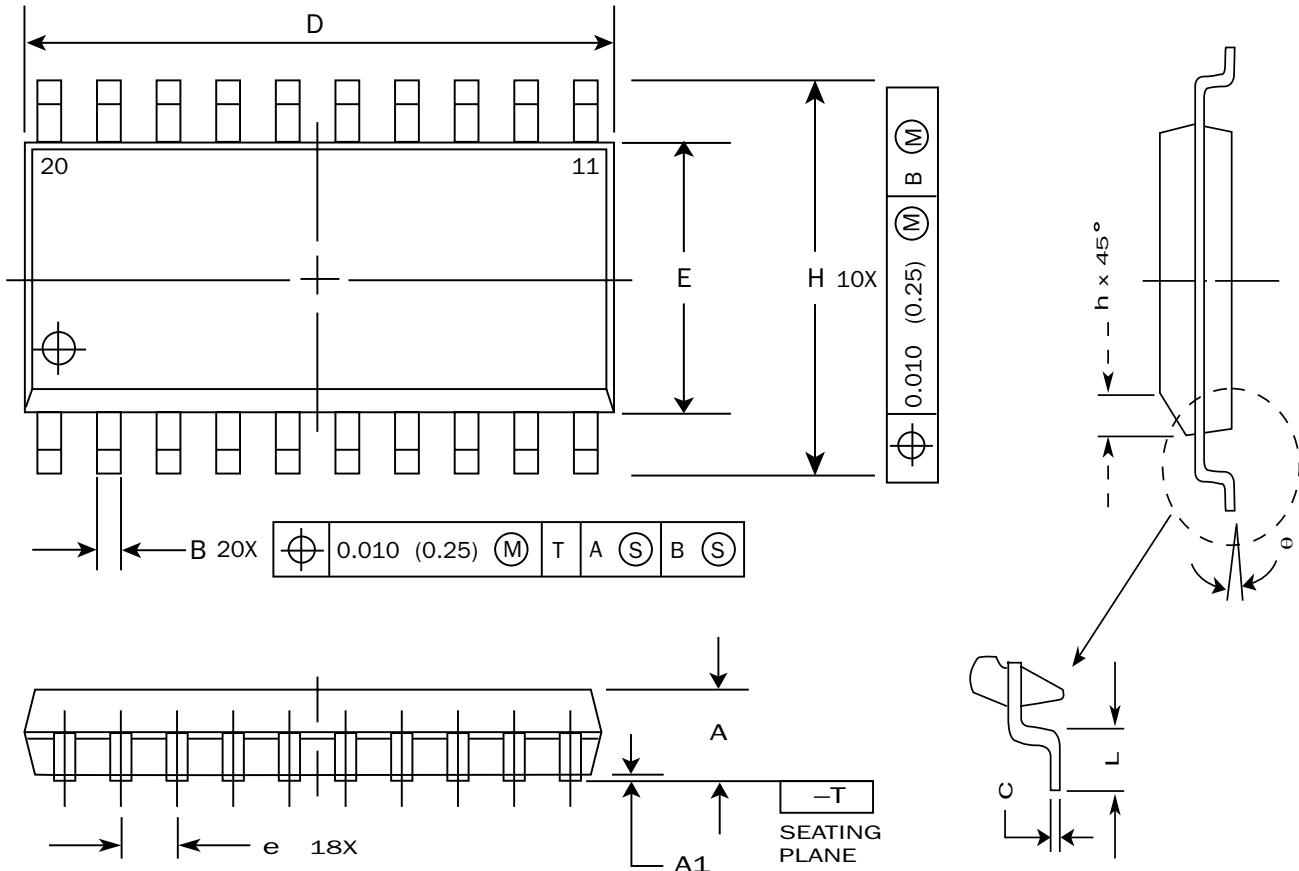
SELECT	DATA
H	A
L	B

Function Table

HIGH-PERFORMANCE PRODUCTS

Package Information

20 Pin SOIC Package



DIM	Millimeters	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

NOTES:

1. Dimensions and tolerances per ASME Y14.5M, 1994.
2. Controlling dimension: millimeters.
3. Dimensions D and E do not include mold protrusion.
4. Maximum mold protrusion 0.15 per side.
5. Dimension B does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.13 total in excess of B dimension at maximum material condition.

HIGH-PERFORMANCE PRODUCTS
DC Characteristics

SK10/100EL56W DC Electrical Characteristics (Notes 1, 2, 7)

 ($V_{CC} - V_{EE} = +3.0V$ to $+5.5V$; V_{OUT} loaded 50Ω to $V_{CC} - 2.0V$)

Symbol	Characteristic	TA = - 40°C			TA = 0°C			TA = + 25°C			TA = + 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{IN}	Input HIGH Current (Diff) (SE)	-150		150 150	-150		150 150	-150		150 150	-150		150 150	μA
I_{EE}	Power Supply current		20	29		20	29		20	29		20	29	mA
V_{BB}	Output Reference Voltage ⁶ 10EL 100EL	-1.43 -1.38		-1.30 -1.26	-1.38 -1.38		-1.27 -1.26	-1.35 -1.38		-1.25 -1.26	-1.31 -1.38		-1.19 -1.26	V V

AC Characteristics

SK10/100EL56W AC Electrical Characteristics (Notes 1, 2)

 ($V_{CC} - V_{EE} = +3.0V$ to $+5.5V$; V_{OUT} loaded 50Ω to $V_{CC} - 2.0V$)

Symbol	Characteristic	TA = - 40°C			TA = 0°C			TA = + 25°C			TA = + 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH} t_{PHL}	Input to Output Delay ³ Q, Q* (DIFF)	430	480	520	440	490	540	455	510	550	485	525	580	ps
t_{PLH} t_{PHL}	Input to Output Delay ³ Q, Q* (SE)	445	515	555	455	520	575	465	530	615	480	550	640	ps
t_{PLH} t_{PHL}	SEL/COM_SEL to Output Delay ³ Q, Q*	530	570	630	550	585	650	560	595	665	595	610	750	ps
t_{skew}	Input Skew Dn, Dn* to Q, Q*		40	80		40	80		40	80		40	80	ps
V_{PP}	Minimum Input Swing ⁴	150		1000	150		1000	150		1000	150		1000	mV
V_{CMR}	Common Mode Range ⁵	$V_{EE} + 1.4$		V_{CC}	$V_{EE} + 1.4$		V_{CC}	$V_{EE} + 1.4$		V_{CC}	$V_{EE} + 1.4$		V_{CC}	V
t_r, t_f	Output Rise/Fall Times (20% to 80%) Q, Q*	215	270	320	225	285	340	230	285	360	240	295	370	ps

Application Notes
AN1002 - Interfacing Between ECL / LVECL / PECL / LVPECL - to - TTL / LVTTTL / CMOS / LVCMOS

AN1003 - Termination Techniques for ECL / LVECL / PECL / LVPECL Devices

AN1004 - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL

AN1005 - Using ECL / LVECL Devices as PECL / LVPECL

AN1006 - Designing with 10K and 100K ECL / PECL Devices

HIGH-PERFORMANCE PRODUCTS**AC Information (continued)**

Notes:

1. 10EL circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to VCC-2.0V.
2. 100K circuits are designed to meet the DC specification shown in the table where transverse airflow greater than 500 lfpm is maintained.
3. Duty cycle skew is the difference between T_{PLH} and T_{PHL} propagation delay through a device.
4. Minimum input swing for which AC parameters guaranteed.
5. CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the high level falls within the specified range and the peak-to-peak voltage lies between $V_{PP(\min)}$ and 1V. The lower end of the CMR range varies 1:1 with VEE and is equal to $VEE + 1.4V$.
6. Voltages referenced to VCC = 0V.
7. For standard ECL DC specifications, refer to the ECL Logic Family Standard DC Specifications Data Sheet.
8. For part ordering description, see HPP Part Ordering Information Data Sheet.

Ordering Information

Ordering Code	Package ID
SK10EL56WD	20-SOIC
SK10EL56WDT	20-SOIC
SK100EL56WD	20-SOIC
SK100EL56WDT	20-SOIC
SK10EL56WU	Die
SK100EL56WU	Die

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