CALMOS™

DECEMBER 1989

CA82C84A

CLOCK GENERATOR AND DRIVER

- Pin and functional compatibility with the industry standard 8284/8284A
- Generates system clock for 80C86/88 microprocessors
- Very high speed - 5, 8 and 10 MHz
- Low power CMOS implementation
- TTL input/output compatibility
- 5V ± 10% power supply
- Provides Local READY and Multibus™ READY Synchronization
- Generates System Reset Output from Schmitt Trigger Input
- Capable of Clock Synchronization with other 8284As
- Uses a Crystal or a TTL signal for frequency source

The CA82C84A is a high performance, single chip clock generator/driver for the 8088/86 type processors, offering pin-for-pin functional compatibility with the industry standard 8284/8284A. It features a crystal-controlled oscillator, a divide-by-three counter, complete Multibus™ *Ready* synchronization, and reset logic.

The CA82C84A is manufactured using CMOS technology. Its high speed makes it ideally suited for aerospace and defense applications. Its very low power consumption also makes it suitable for portable systems and systems with low power standby modes.

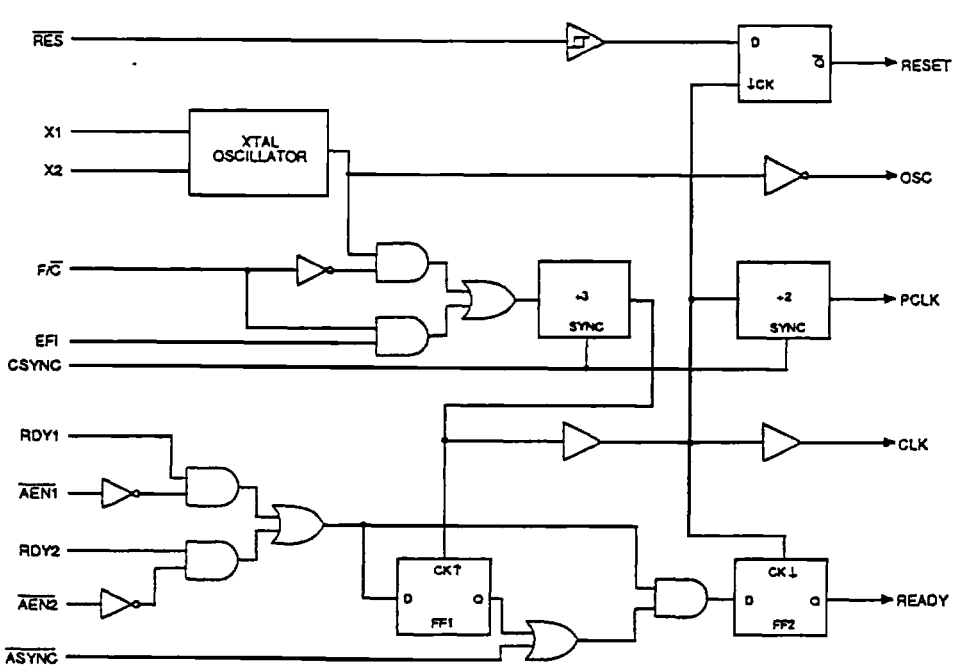


Figure 1 : CA82C84A BLOCK DIAGRAM

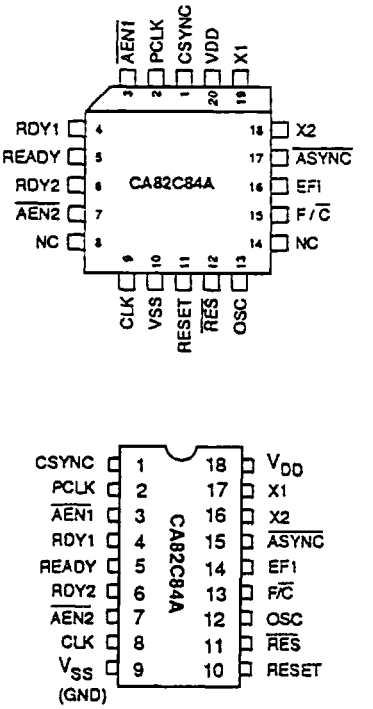


Figure 2 : PLCC and DIP PIN CONFIGURATIONS

Table 1 : PIN DESCRIPTIONS

Symbol	Pin(s)		Type	Name and Function
	PLCC	PDIP		
$\overline{AEN1}$, $\overline{AEN2}$	3, 7	3, 7	I	**Address Enable:** $\overline{AEN}$ is an active LOW signal which qualifies its respective Bus Ready Signal. $\overline{AEN1}$ validates RDY1 while $\overline{AEN2}$ validates RDY2. Two $\overline{AEN}$ signal inputs are useful in system configurations with two multi-master System Buses. In non-multi-master configurations the $\overline{AEN}$ signal inputs are tied true (LOW).
$\overline{ASYNC}$	17	15	I	**Ready Synchronization Select:** $\overline{ASYNC}$ defines the synchronization mode of the READY logic. When $\overline{ASYNC}$ is LOW, two stages of READY sync are provided. When HIGH or open a single stage of READY sync is provided (an internal pull-up is provided).
CLK	9	8	O	**Processor Clock:** CLK is used by the processor and all devices which connect directly to the processor's local bus. CLK has an output frequency of $^1/_3$ the crystal or EFI input frequency and a $^1/_3$ duty cycle. An output HIGH of 4.5 volts (V_{DD} = 5V) is provided to drive MOS devices.
CSYNC	1	1	I	**Clock Synchronization:** CSYNC is an active HIGH signal which allows multiple 8284As to be synchronized to provide clocks that are in phase. When CSYNC is HIGH the internal counters are reset. When CSYNC goes LOW the internal counters are allowed to resume counting. CSYNC *must* be externally synchronized to EFI. When using the internal oscillator, CSYNC should be hardwired to ground.
EFI	16	14	I	**External Frequency:** When F/$\overline{C}$ is strapped HIGH, CLK is generated from the input frequency appearing on this pin. The input signal is a square wave 3x the frequency of the desired CLK output.
F/$\overline{C}$	15	13	I	**Frequency/Crystal Select:** F/$\overline{C}$ is a strapping option. When strapped LOW, F/$\overline{C}$ permits the processor clock to be generated by the crystal. When strapped HIGH, CLK is generated from the EFI input.
OSC	13	12	O	**Oscillator Output:** OSC is the TTL level output of the internal oscillator circuitry. Its frequency is equal to that of the crystal.
PCLK	2	2	O	**Peripheral Clock:** PCLK is a TTL level peripheral clock signal whose output frequency is $^1/_2$ that of CLK and has a 50% duty cycle.
RDY1, RDY2	4, 6	4, 6	I	**Bus Ready:** (Transfer Complete) RDY is an active HIGH signal which indicates that data from a device located on the system data bus has been received, or is available. RDY1 is qualified by $\overline{AEN1}$ while RDY2 is qualified by $\overline{AEN2}$.
READY	5	5	O	**Ready:** READY is an active HIGH signal which is the synchronized RDY signal input. READY is cleared after the guaranteed hold time to the processor has been met.
$\overline{RES}$	12	11	I	**Reset In:** $\overline{RES}$ is an active LOW signal used to generate RESET. The CA82C84A provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration.
RESET	11	10	O	**Reset:** RESET is an active HIGH signal which is used to reset the 8086 family processors. Its timing characteristics are determined by $\overline{RES}$.
V_{DD}	20	18	-	**Power:** 5V ± 10% DC Supply
V_{SS}	10	9	-	**Ground:** 0 V
X1, X2	19, 18	17, 16	I	**Crystal In:** X1 and X2 are the pins to which a crystal is attached. The crystal frequency is 3x the desired processor clock frequency. (If no crystal is attached, then X1 should be tied to V_{DD} or V_{SS} and X2 should be left open.)

FUNCTIONAL DESCRIPTION

Oscillator

The oscillator of the CA82C84A is designed for use with an external parallel resonant, fundamental mode crystal from which the basic operating frequency is derived.

The crystal frequency should be selected to be 3x the required CPU clock frequency. X1 and X2 are the two crystal inputs. For the most stable operation of OSC, two capacitors (C1 = C2), as shown in the waveform figures, are recommended. The output of the oscillator is buffered and brought out on OSC so that other system timing signals can be derived from this stable, crystal-controlled source.

Capacitors C1, C2 are chosen such that their combined capacitance:

$$CT = \frac{C1 + C2}{C1 \cdot C2}$$ (Including stray capacitance)

matches the load capacitance as specified by the crystal manufacturer. This insures operation within the frequency tolerance specified by the crystal manufacturer.

Clock Generator

The clock generator consists of a synchronous divide-by-three counter with a special clear input that inhibits the counting. This clear input (CSYNC) allows the output clock to be synchronized with an external event (such as another CA82C84A clock). The CSYNC input is synchronized to the EFI clock externally with the use of two Schottky flip-flops. The counter output is a 33% duty cycle clock at one-third the input frequency.

The F/$\overline{C}$ input is a strapping pin that selects either the crystal oscillator or the EFI input as the clock for the ÷ 3 counter. If the EFI input is selected as the clock source, the oscillator section can be used independently for another clock source with output taken from OSC.

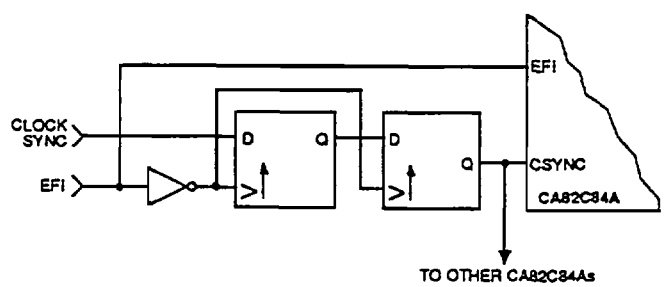


Figure 3 : CSYNC SYNCHRONIZATION

Clock Outputs

The CLK output is a 33% duty cycle clock driver designed to drive the 8088/86 processors directly. PCLK is a TTL level peripheral clock signal with a frequency of $^1/_2$ CLK, and a 50% duty cycle.

Reset Logic

The reset logic provides a Schmitt trigger input ($\overline{RES}$) and a synchronizing flip-flop to generate the reset timing. The reset signal is synchronized to the falling edge of CLK. Utilizing this function, a simple RC network can be used to provide a power-on reset.

READY Synchronization

Two READY Inputs (RDY1, RDY2) are provided to accommodate two multi-master system buses. Each input has a qualifier ($\overline{AEN1}$ and $\overline{AEN2}$, respectively). The $\overline{AEN}$ signals validate their respective RDY signals. If a multi-master system is not being used, the $\overline{AEN}$ pin should be tied LOW.

Synchronization is required for all asynchronous active-going edges of either RDY input to guarantee that the RDY setup and hold times are met. Inactive-going edges of RDY in normally ready systems do not require synchronization, but must satisfy RDY setup and hold.

The $\overline{ASYNC}$ input defines two modes of READY synchronization operation. When $\overline{ASYNC}$ is LOW, two stages of synchronization are provided for active READY input signals. Positive-going asynchronous READY inputs are first synchronized to flip-flop one at the rising edge of CLK, and then synchronized to flip-flop two at the next falling edge of CLK, after which the READY output goes active (HIGH). Negative-going async READY inputs are synchronized directly to flip-flop two at the falling edge of CLK, after which the READY output goes inactive. This mode of operation is intended for asynchronous (normally not ready) devices in the system which cannot be guaranteed by design to meet the required RDY setup timing, t_{R1VCL}, on each bus cycle.

When $\overline{ASYNC}$ is HIGH or open, the first READY flip-flop is bypassed in the READY synchronization logic. READY inputs are synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices that can be guaranteed to meet the required RDY setup time. $\overline{ASYNC}$ can change at every bus cycle to set the correct synchronization mode for each device in the system.

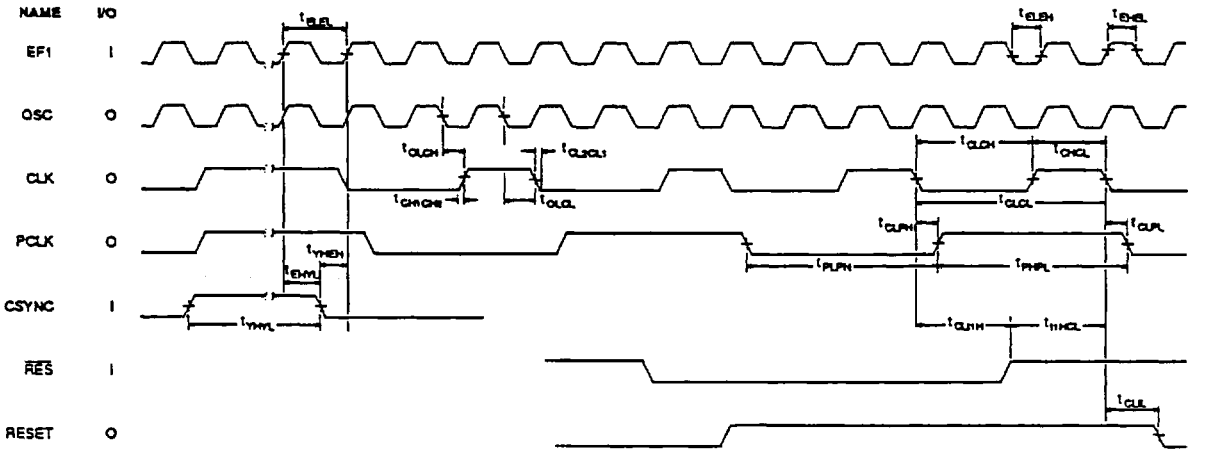
Table 2 : AC CHARACTERISTICS (T_A = –40° to +85°C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Test Conditions	Limits (5 MHz)		Limits (8 MHz)		Limits (10 MHz)		Units
			Min	Max	Min	Max	Min	Max	
t_{A1VR1V}	$\overline{AEN1, 2}$ setup to RDY1, 2		15		15		15		ns
t_{AYVCL}	$\overline{ASYNC}$ setup to CLK		50		50		50		ns
t_{CH1CH2} t_{CL2CL1}	CLK rise or fall time	1.0 V to 3.5 V		10		10		10	ns
t_{CHCL}	CLK HIGH time		$(^1/_3\ t_{CLCL})+2$		$(^1/_3\ t_{CLCL})+2$		39		ns
t_{CLA1X}	$\overline{AEN1}$, $\overline{AEN2}$ hold to CLK		0		0		0		ns
t_{CLAYX}	$\overline{ASYNC}$ hold to CLK		0		0		0		ns
t_{CLCH}	CLK LOW time		$(^2/_3\ t_{CLCL})-15$		$(^2/_3\ t_{CLCL})-15$		53		ns
t_{CLCL}	CLK cycle period		200		125		100		ns
t_{CLI1H}	$\overline{RES}$ hold to CLK	Note 2	20		10		10		ns
t_{CLIL}	CLK to reset delay			40		40		40	ns
t_{CLR1X}	RDY1, RDY2 hold to CLK		0		0		0		ns
t_{CLPH}	CLK to PCLK HIGH delay			22		22		22	ns
t_{CLPL}	CLK to PCLK LOW Delay			22		22		22	ns
t_{EHEL}	External frequency HIGH time	90%–90% V_{IN}	20		13		13		ns
t_{EHYL}	CSYNC hold to EFI		20		10		10		ns
t_{ELEH}	External frequency LOW time	10%–10% V_{IN}	20		13		13		ns
t_{ELEL}	EFI period	Note 1	66		36		33		ns
t_{I1HCL}	$\overline{RES}$ setup to CLK	Note 2	65		65		65		ns
t_{IHIL}	Input fall time	Note 1		15		15		15	ns
t_{ILIH}	Input rise time	Note 1		15		15		15	ns
t_{OLCH}	OSC to CLK HIGH delay		–5	22	–5	22	–5	22	ns
t_{OLCL}	OSC to CLK LOW display		2	35	2	35	2	35	ns
t_{OLOH}	Output rise time (except CLK)	From 0.8 – 2.0 V		15		15		15	ns
t_{OHOL}	Output fall time (except CLK)	From 2.0 – 0.8 V		15		15		15	ns
t_{PHPL}	PCLK HIGH time		t_{CLCL}–20		t_{CLCL}–20		t_{CLCL}–20		ns
t_{PLPH}	PCLK LOW time		t_{CLCL}–20		t_{CLCL}–20		t_{CLCL}–20		ns
t_{R1VCH}	RDY1, 2 active setup to CLK	$\overline{ASYNC}$ = LOW	35		35		35		ns
t_{R1VCL}	RDY1, 2 active setup to CLK (Note 5)	$\overline{ASYNC}$ = HIGH	35		35		35		ns
t_{RYHCH}	Ready active to CLK (Note 3)		$(^2/_3\ t_{CLCL})-15$		$(^2/_3\ t_{CLCL})-15$		53		ns
t_{RYLCL}	Ready inactive to CLK (Note 4)		–8		–8		–8		ns
t_{YHEH}	CSYNC setup to EFI		20		20		20		ns
t_{YHYL}	CSYNC width		$2 \cdot t_{ELEL}$		$2 \cdot t_{ELEL}$		$2 \cdot t_{ELEL}$		ns
	XTAL frequency		2.4	15	2.4	25	2.4	30	MHz

Notes : 1. Transition between V_{IL} (max) – 0.4V and V_{IH} (min) + 0.4V.
2. Setup and hold necessary only to guarantee recognition at next clock.
3. Applies only to T3 and TW states.
4. Applies only to T2 states.
5. t_{R1VCL} = 40 ns at all speeds for industrial temperature range devices.

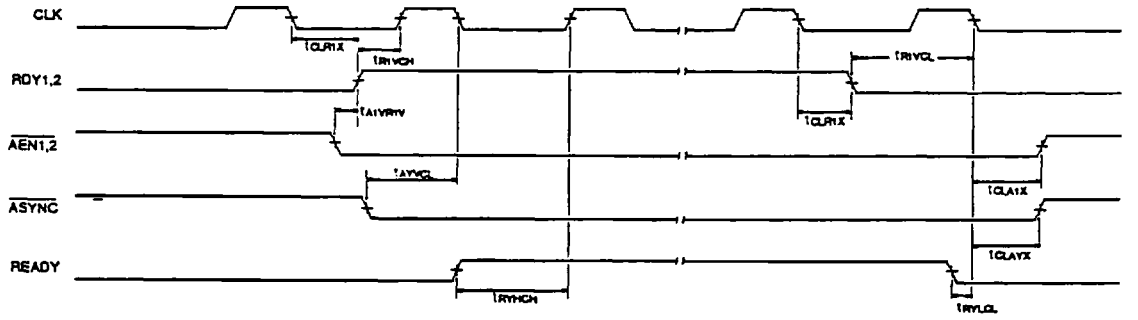
Figure 4 : TIMING DIAGRAMS

a) Clocks and Reset Signals

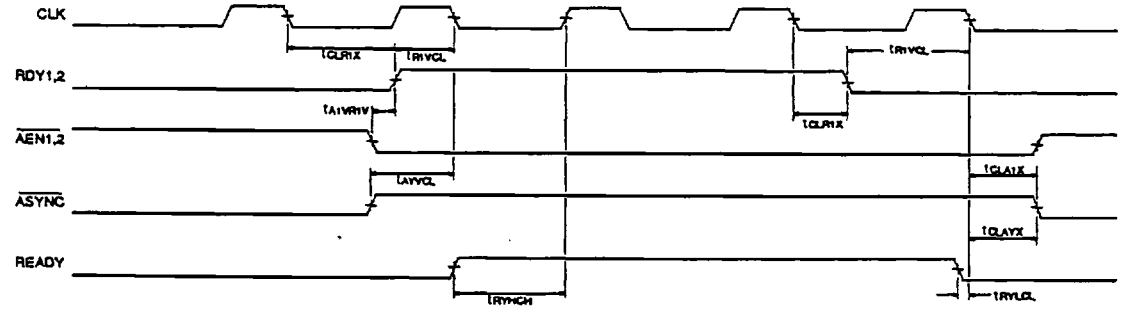


Note: All timing measurements are made at 1.5 Volts, unless otherwise noted.

b) Ready Signals (for Asynchronous Devices)

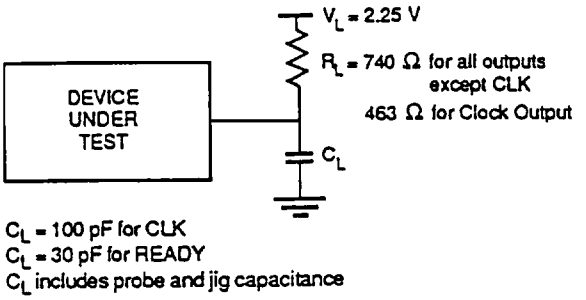


c) Ready Signals (For Synchronous Devices)



AC TESTING: All input signals must switch between 0.45V and 2.4V. T_{RISE} and T_{FALL} must be ≤ 15 ns. All timing measurements are made at 1.5V.

Figure 5: AC TESTING I/O WAVEFORM



C_L = 100 pF for CLK
C_L = 30 pF for READY
C_L includes probe and jig capacitance

Figure 6 : AC TESTING LOADING CIRCUIT

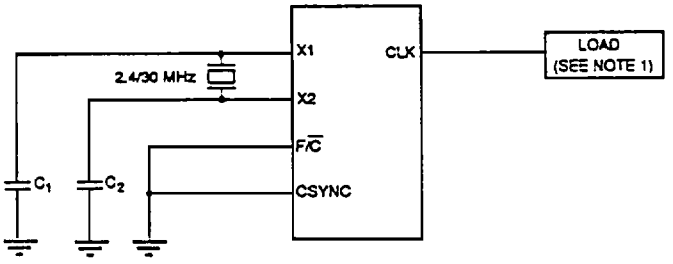


Figure 7 : CLOCK HIGH and LOW TIME (using X1, X2)

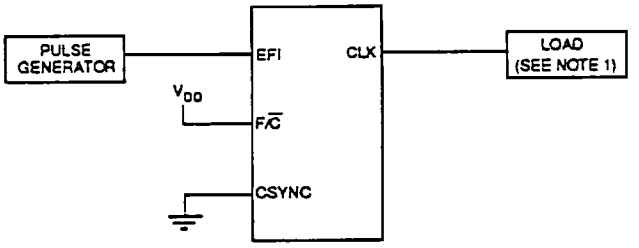


Figure 8 : CLOCK HIGH and LOW TIME (using EFI)

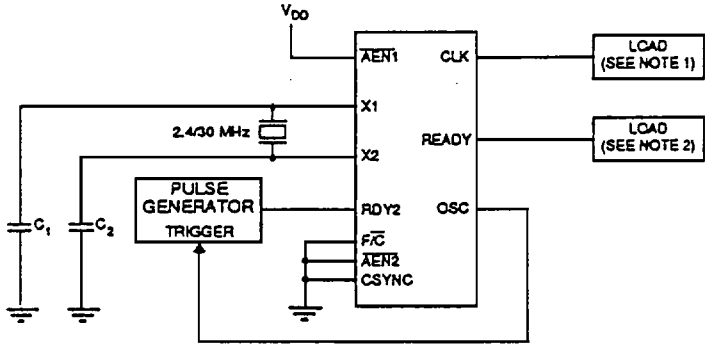


Figure 9 : READY TO CLOCK (USING X1, X2)

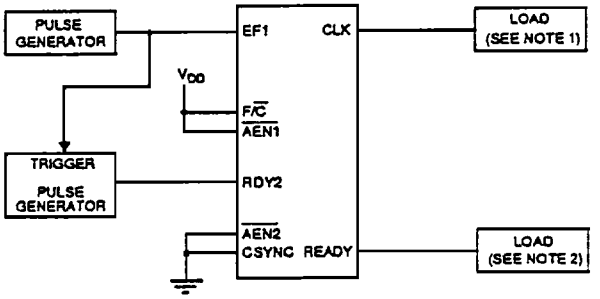


Figure 10 : READY TO CLOCK (USING EFI)

Notes: 1. C_L = 100 pF
2. C_L = 30 pF

Table 3 : DC CHARACTERISTICS (T_A = –40° to +85°C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter		Test Conditions	Limits		Units
				Min	Max	
C_{IN}	Input capacitance		Freq = 1 MHz	-	7	pF
I_{CC}	Operating supply current: 10 MHz 5 MHZ		30 MHz Xtal, C_L = 0 15 MHZ Xtal, C_L = 0	- -	40 10	mA mA
I_{CCS}	Standby supply current (Note 1)			-	100	µA
I_{LI}	Input leakage current (Note 2)	$\overline{ASYNC}$ only	$\overline{ASYNC} = V_{DD}$	-	10	µA
			$\overline{ASYNC} = V_{SS}$	-	–130	µA
		All other pins	$0V \le V_{IN} \le V_{DD}$	-	±1.0	µA
V_{IH}	Input HIGH voltage			2.2	V_{DD} + 0.5	V
V_{IHR}	Reset input HIGH voltage			0.6 V_{DD}	-	V
V_{IHR} - V_{ILR}	$\overline{RES}$ input hysteresis		CA82C84A–10	0.15	-	V
			CA82C84A–5	0.25	-	V
V_{IL}	Input LOW voltage			-	0.8	V
V_{OH}	Output HIGH voltage		CLK: I_{OH} = –4 mA Others: I_{OH} = –2.5 mA	V_{DD}–0.4	-	V
V_{OL}	Output LOW voltage		CLK: I_{OL} = 4 mA Others: I_{OL} = 2.5 mA	-	0.4	V

Table 4 : RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage		+4 V to +6 V
Operating Temperature Range	Commercial	0°C to 70°C
	Industrial	–40°C to +85°C
	Military	–55°C to +125°C

Table 5 : ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage	+7.0 V
Input, Output or I/O Voltage Applied	V_{SS} – 0.5 V to V_{DD} + 0.5 V
Storage Temperature Range	–65°C to +150°C
Maximum Package Power Dissipation	1 W

Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

MECHANICALS

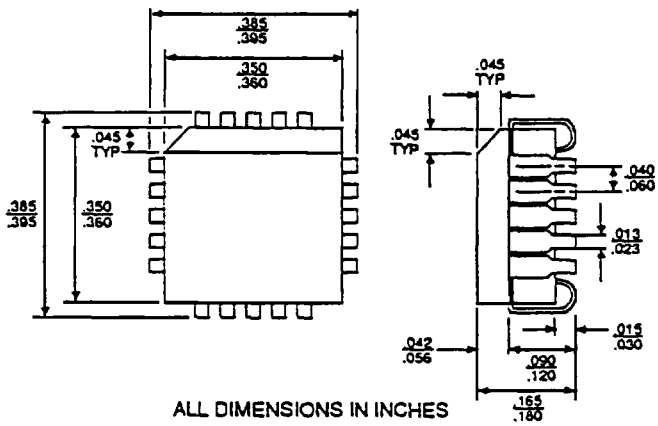


Figure 12 : PLCC PACKAGING

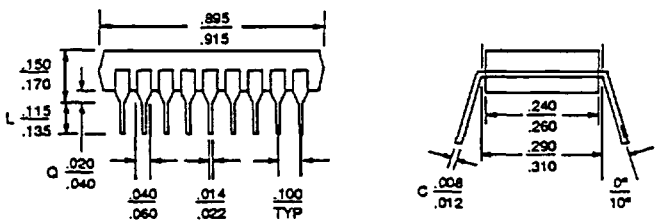


Figure 12 : PLASTIC PACKAGING

ORDERING INFORMATION and PRODUCT CODE

CA82C84A – X X X

Part Number

Speed
- -5 5 MHz
- -8 8 MHz
- -10 10 MHz

Packaging
- D - Ceramic (side-brazed)
- J - Cerdip (frit-seal)
- P - Plastic DIP
- L - Leadless Chip Carrier (Ceramic)
- N - Plastic Leaded Chip Carrier (PLCC)

Temperature

C - Commercial	(0° to + 70°C)
I - Industrial	(–40° to + 85°C)
E - Extended Temp	(–55° to +125°C)
M - Military	(–55° to +125°C)
Screened to MIL-STD-883 Equivalent	

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