Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (16K x 4-BIT)

IDT 7188S
IDT 7188L

T-46-23-10

FEATURES:

- High-speed (equal access and cycle times)
  - Military: 20/25/30/35/45/55/70/85ns (max.)
  - Commercial: 15/20/25/30/35/45ns (max.)
- Low power consumption
  - IDT7188S
    Active: 350mW (typ.)
    Standby: 100µW (typ.)
  - IDT7188L
    Active: 300mW (typ.)
    Standby: 30µW (typ.)
- Battery backup operation—2V data retention (L version only)
- Available in high-density industry standard 22-pin, 300 mil ceramic and plastic DIP, 24-pin SOIC, 24-pin Flatpack and CERPACK
- Produced with advanced CEMOS™ technology
- Single 5V (±10%) power supply
- Inputs/outputs TTL-compatible
- Three-state outputs
- Static operation: no clocks or refresh required
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7188 is a 65,536-bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for memory intensive applications.

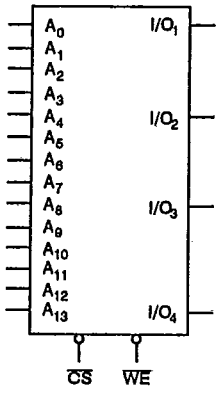
Access times as fast as 15ns are available, with typical power consumption of only 300mW. The IDT7188 offers a reduced power standby mode, I_{SB1}, which enables the designer to greatly reduce device power requirements. This capability significantly decreases system power and cooling levels, while greatly enhancing system reliability. The low-power version (L) version also offers a battery backup data retention capability where the circuit typically consumes only 30µW operating from a 2V battery.

All inputs and outputs are TTL-compatible and operate from a single 5V supply. Fully static asynchronous circuitry, along with matching access and cycle times, favor the simplified system design approach.

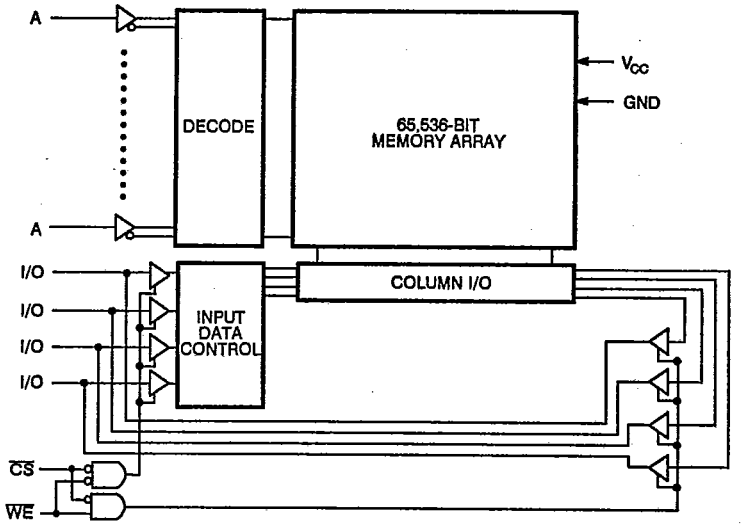
The IDT7188 is packaged in 22-pin, 300 mil ceramic and plastic DIPs, 24-pin SOICs, flatpacks and CERPACKs, providing excellent board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

LOGIC SYMBOL



FUNCTIONAL BLOCK DIAGRAM



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DSC-1026/1

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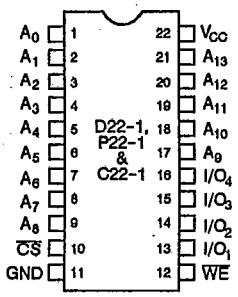
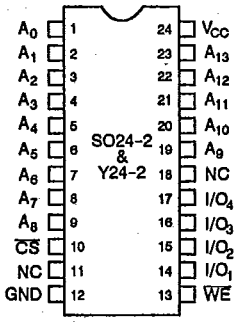
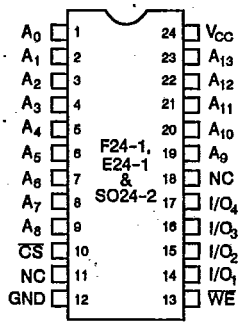
PIN CONFIGURATIONS



DIP
TOP VIEW



SOIC
TOP VIEW



FLATPACK/CERPACK/SOIC
TOP VIEW

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PIN NAMES

A_0–A_{13}	Address Inputs	I/O_1–I/O_4	Data I/O
$\overline{CS}$	Chip Select	V_{CC}	Power
$\overline{WE}$	Write Enable	GND	Ground

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

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DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITION		IDT7188S MIN.	IDT7188S TYP.(1)	IDT7188S MAX.	IDT7188L MIN.	IDT7188L TYP.(1)	IDT7188L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:

1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS (1)

V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V

SYMBOL	PARAMETER	POWER	7188S15 COM'L.	7188S15 MIL.	7188S20 COM'L.	7188S20 MIL.	7188S25 7188L25 COM'L.	7188S25 7188L25 MIL.	7188S30/35 7188L30/35 COM'L.	7188S30/35 7188L30/35 MIL.	7188S45/55(3) 7188L45/55(3) COM'L.	7188S45/55(3) 7188L45/55(3) MIL.	7188S70 7188L70 COM'L.	7188S70 7188L70 MIL.	7188S85 7188L85 COM'L.	7188S85 7188L85 MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = 0(2)	S	135	–	120	140	100	125	100	110	100	110	–	110	–	110	mA
		L	–	–	–	–	85	110	85	95	85	95	–	95	–	95	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	S	180	–	155	175	135	155	125	140	125	140	–	140	–	140	mA
		L	–	–	–	–	125	145	115/105	125/115	100	110	–	110	–	105	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open f = f_{MAX}(2)	S	75	–	60	70	55	60	50/45	55/50	45	50	–	50	–	50	mA
		L	–	–	–	–	45	50	40/35	45/40	30	35	–	35	–	35	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC} f = 0(2)	S	25	–	20	25	15	20	15	20	15	20	–	20	–	20	mA
		L	–	–	–	–	0.5	1.5	0.5	1.5	0.5	1.5	–	1.5	–	1.5	

NOTES:

1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.
3. -55°C to +125°C temperature range only.

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DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.[1] V_{CC} @ 2.0V	TYP.[1] V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	–	10	15	600	900	µA
			COM'L.	–	10	15	150	225	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	–		–		ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	–		–		ns
$\|I_{LI}\|$[3]	Input Leakage Current			–	–		2		µA

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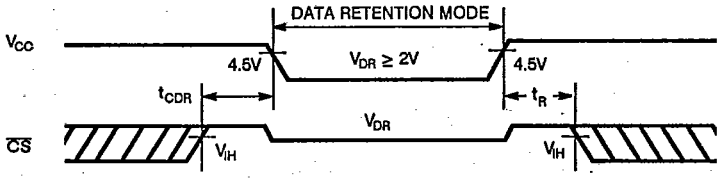
NOTES:
1. T_A = 25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

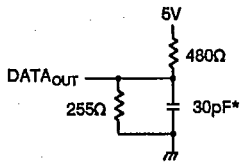


Figure 1. Output Load

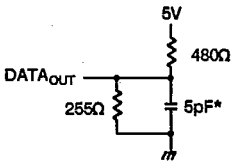


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ} and t_{OW})

* Including scope and jig.

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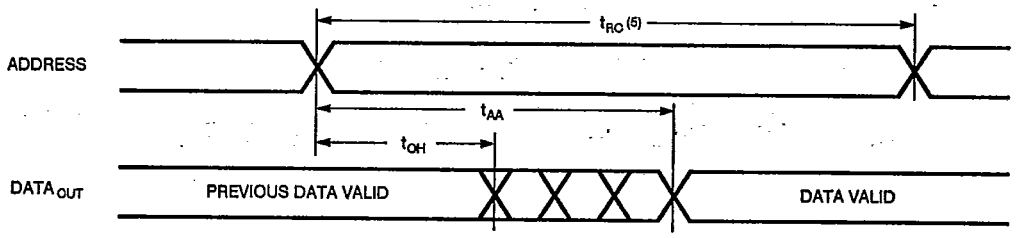
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

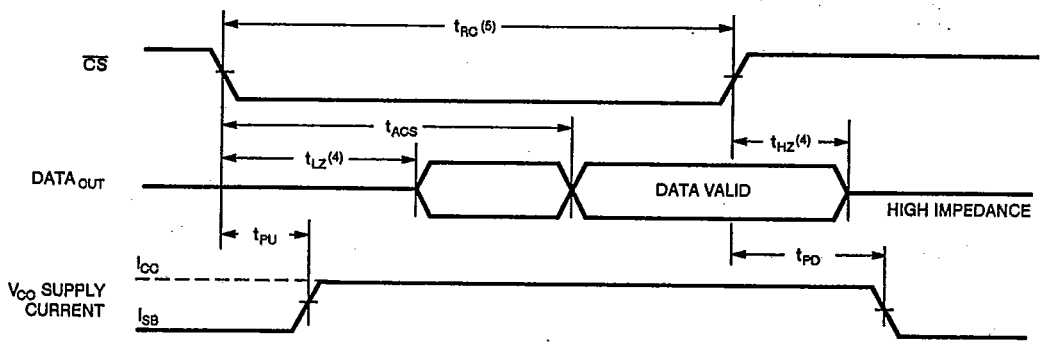
SYMBOL	PARAMETER	7188S15[1] MIN.	7188S15[1] MAX.	7188S20[4] MIN.	7188S20[4] MAX.	7188S25/30 7188L25/30 MIN.	7188S25/30 7188L25/30 MAX.	7188S35/45 7188L35/45 MIN.	7188S35/45 7188L35/45 MAX.	7188S55/70[2] 7188L55/70[2] MIN.	7188S55/70[2] 7188L55/70[2] MAX.	7188S85[2] 7188L85[2] MIN.	7188S85[2] 7188L85[2] MAX.	UNIT
READ CYCLE														
t_{RC}	Read Cycle Time	15	–	20	–	25/30	–	35/45	–	55/70	–	85	–	ns
t_{AA}	Address Access Time	–	15	–	20	–	25/30	–	35/45	–	55/70	–	85	ns
t_{ACS}	Chip Select Access Time	–	15	–	20	–	25/30	–	35/45	–	55/70	–	85	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{LZ}	Chip Selection to Output in Low Z[3]	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{HZ}	Chip Deselect to Output in High Z[3]	–	7	–	8	–	10/12	–	14	–	20/25	–	30	ns
t_{PU}	Chip Select to Power Up Time[3]	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time[3]	–	15	–	20	–	25/30	–	35/45	–	55/70	–	85	ns

NOTES:
1. 0°C to -70°C temperature range only.
2. -55°C to -125°C temperature range only.
3. This parameter is guaranteed but not tested.
4. Preliminary data only for military devices.

TIMING WAVEFORM OF READ CYCLE NO. 1[1, 2]



TIMING WAVEFORM OF READ CYCLE NO. 2[1, 3]



NOTES:
1. $\overline{WE}$ is high for READ Cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

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AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	7188S15[1] MIN.	7188S15[1] MAX.	7188S20[4] MIN.	7188S20[4] MAX.	7188S25/30 7188L25/30 MIN.	7188S25/30 7188L25/30 MAX.	7188S35/45 7188L35/45 MIN.	7188S35/45 7188L35/45 MAX.	7188S55/70[2] 7188L55/70[2] MIN.	7188S55/70[2] 7188L55/70[2] MAX.	7188S85[2] 7188L85[2] MIN.	7188S85[2] 7188L85[2] MAX.	UNIT
WRITE CYCLE														
t_{WC}	Write Cycle Time	14	—	17	—	20/22	—	30/40	—	50/60	—	75	—	ns
t_{CW}	Chip Select to End of Write	14	—	17	—	20/22	—	25/35	—	50/60	—	75	—	ns
t_{AW}	Address Valid to End of Write	14	—	17	—	20/22	—	25/35	—	50/60	—	75	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	14	—	17	—	20/22	—	25/35	—	50/60	—	75	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	8	—	10	—	13/15	—	15/20	—	25/30	—	35	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High Z[3]	0	5	—	6	—	7/10	—	10/15	—	25/30	—	40	ns
t_{OW}	Output Active from End of Write[3]	5	—	5	—	5	—	5	—	5	—	5	—	ns

NOTES:
1. 0°C to -70°C temperature range only.
2. -55°C to -125°C temperature range only.
3. This parameter is guaranteed but not tested.
4. Preliminary data only for military devices.

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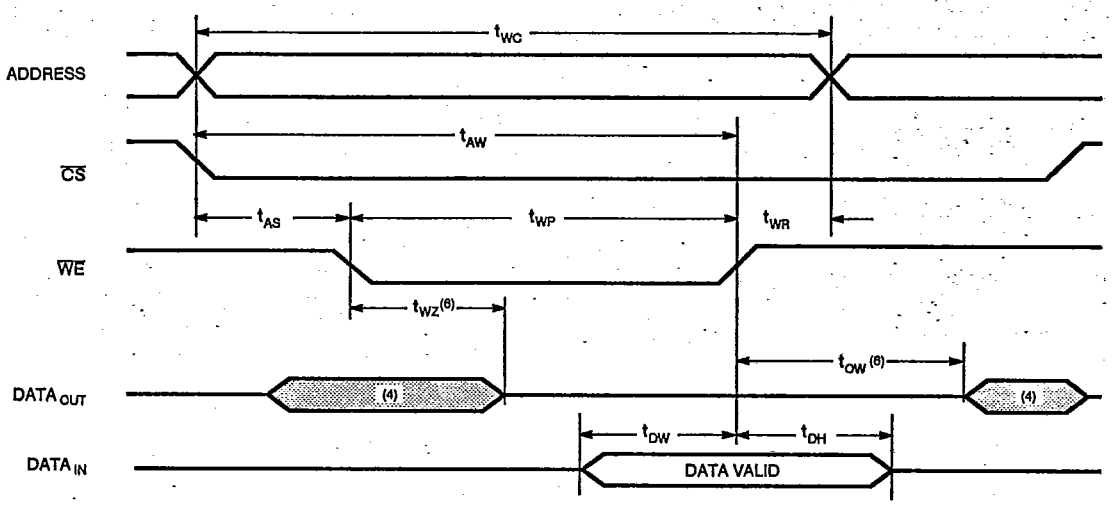
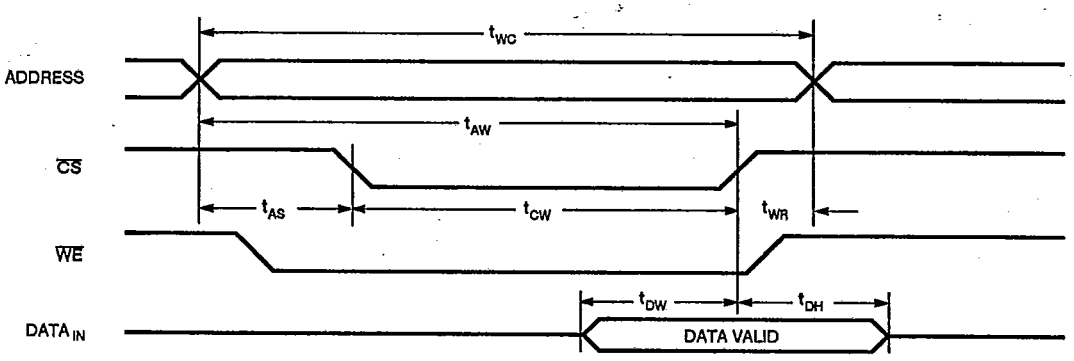
TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3]



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 3, 5]



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals should not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±200 mV from steady state.

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TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	I/O	POWER
Standby	H	X	High Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	D_{IN}	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz, V_{CO} = 0V)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	6	pF

NOTE:
1. This parameter is determined by device characterization, but is not production tested.

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ORDERING INFORMATION

IDT — XXXXX Device Type — A Power — 999 Speed — A Package — A Process/Temperature Range

Blank	Commercial (0°C to +70°C)
B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
D	Ceramic DIP
P	Plastic DIP
C	Sidebraze DIP
SO	Small Outline IC (Gull Wing)
Y	Small Outline IC (J-Bend)
F	Flatpack
E	CERPACK
Y	Small Outline (J-Bend)
15	Commercial Only
20	Speed in Nanoseconds
25	Speed in Nanoseconds
30	Speed in Nanoseconds
35	Speed in Nanoseconds
45	Speed in Nanoseconds
55	Military Only
70	Military Only
85	Military Only
S	Standard Power
L	Low Power
7188	64K (16K x 4-Bit)