

# Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

## **Quality Overview**

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.



October 1987 Revised March 2002

## **CD4027BC**

## **Dual J-K Master/Slave Flip-Flop with Set and Reset**

## **General Description**

The CD4027BC dual J-K flip-flops are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. Each flip-flop has independent J, K, set, reset, and clock inputs and buffered Q and  $\overline{\rm Q}$  outputs. These flip-flops are edge sensitive to the clock input and change state on the positive-going transition of the clock pulses. Set or reset is independent of the clock and is accomplished by a high level on the respective input.

All inputs are protected against damage due to static discharge by diode clamps to  $V_{DD}$  and  $V_{SS}$ .

## **Features**

■ Wide supply voltage range: 3.0V to 15V

■ High noise immunity: 0.45 V<sub>DD</sub> (typ.)

■ Low power TTL compatibility: Fan out of 2 driving 74L

or 1 driving 74LS

■ Low power: 50 nW (typ.)

■ Medium speed operation: 12 MHz (typ.) with 10V

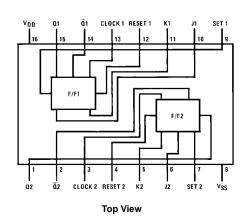
supply

## **Ordering Code:**

Order Number	Package Number	Package Description
CD4027BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4027BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## **Connection Diagram**



## **Truth Table**

Inputs t <sub>n-1</sub> (Note 1)						Outputs t <sub>n</sub> (Note 2)			
CL (Note 3)	J	K	S	R	Q	Q	Q		
~	ı	Χ	0	0	0	ı	0		
~	Χ	0	0	0	- 1	I	0		
~	0	Χ	0	0	0	0	1		
~	Χ	- 1	0	0	- 1	0	1		
~	Χ	Χ	0	0	Χ		(No Change)		
Х	Χ	Χ	I	0	Χ	I	0		
Х	Χ	Χ	0	I	Χ	0	1		
Х	X	Χ	- 1	- 1	Χ	- 1	1		

I = HIGH Level

O = LOW Level

X = Don't Care

\_ = LOW-to-HIGH

Note 1:  $t_{n-1}$  refers to the time interval prior to the positive clock pulse transition

Note 2:  $t_{\rm n}$  refers to the time intervals after the positive clock pulse transition

Note 3: Level Change

# CD4027BC Logic Diagram SLAVE

## **Absolute Maximum Ratings**(Note 4)

(Note 5)

 $\begin{array}{ll} \text{DC Supply Voltage (V}_{\text{DD}}) & -0.5 \text{ V}_{\text{DC}} \text{ to +18 V}_{\text{DC}} \\ \text{Input Voltage (V}_{\text{IN}}) & -0.5 \text{V to V}_{\text{DD}} +0.5 \text{ V}_{\text{DC}} \\ \text{Storage Temperature Range (T}_{\text{S}}) & -65^{\circ}\text{C to +150}^{\circ}\text{C} \end{array}$ 

Power Dissipation (P<sub>D</sub>)

 Dual-In-Line
 700 mW

 Small Outline
 500 mW

Lead Temperature (T<sub>L</sub>)

(Soldering, 10 seconds) 260°C

# Recommended Operating Conditions (Note 5)

DC Supply Voltage ( $V_{DD}$ ) 3V to 15  $V_{DC}$ Input Voltage ( $V_{IN}$ ) 0V to  $V_{DD}$   $V_{DC}$ Operating Temperature Range ( $T_A$ ) -55°C to +125°C

Note 4: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 5:  $V_{SS} = 0V$  unless otherwise specified.

## DC Electrical Characteristics (Note 6)

Parameter	Conditions	-55	–55°C		+25°C			+125°C	
Parameter	Conditions	Min	Max	Min	Тур	Max	Min	Max	Units
Quiescent Device Current	$V_{DD} = 5V$ , $V_{IN} = V_{DD}$ or $V_{SS}$		1			1		30	
	$V_{DD}$ = 10V, $V_{IN}$ = $V_{DD}$ or $V_{SS}$		2			2		60	μΑ
	$V_{DD} = 15V$ , $V_{IN} = V_{DD}$ or $V_{SS}$		4			4		120	
LOW Level	I <sub>O</sub>   < 1 μA								
Output Voltage	$V_{DD} = 5V$		0.05		0	0.05		0.05	
	$V_{DD} = 10V$		0.05		0	0.05		0.05	V
	V <sub>DD</sub> = 15V		0.05		0	0.05		0.05	
HIGH Level	I <sub>O</sub>   < 1 μA								
Output Voltage	$V_{DD} = 5V$	4.95		4.95	5		4.95		
	$V_{DD} = 10V$	9.95		9.95	10		9.95		V
	V <sub>DD</sub> = 15V	14.95		14.95	15		14.95		
LOW Level	$V_{DD} = 5V$ , $V_{O} = 0.5V$ or 4.5V		1.5			1.5		1.5	
Input Voltage	$V_{DD} = 10V, V_{O} = 1V \text{ or } 9V$		3.0			3.0		3.0	V
	$V_{DD} = 15V$ , $V_{O} = 1.5V$ or $13.5V$		4.0			4.0		4.0	
HIGH Level	$V_{DD} = 5V, V_{O} = 0.5V \text{ or } 4.5V$	3.5		3.5			3.5		
Input Voltage	$V_{DD} = 10V, V_{O} = 1V \text{ or } 9V$	7.0		7.0			7.0		V
	$V_{DD} = 15V$ , $V_{O} = 1.5V$ or $13.5V$	11.0		11.0			11.0		
LOW Level Output	$V_{DD} = 5V, V_{O} = 0.4V$	0.64		0.51	0.88		0.36		
Current (Note 7)	$V_{DD} = 10V, V_{O} = 0.5V$	1.6		1.3	2.25		0.9		mA
	$V_{DD} = 15V, V_{O} = 1.5V$	4.2		3.4	8.8		2.4		
HIGH Level Output	$V_{DD} = 5V, V_{O} = 4.6V$	-0.64		-0.51	-0.88		-0.36		
Current (Note 7)	$V_{DD} = 10V, V_{O} = 9.5V$	-1.6		-1.3	-2.25		-0.9		mA
	$V_{DD} = 15V, V_{O} = 13.5V$	-4.2		-3.4	-8.8		-2.4		
Input Current	V <sub>DD</sub> = 15V, V <sub>IN</sub> = 0V		-0.1		-10 <sup>-5</sup>	-0.1		-1.0	
	$V_{DD}=15V,\ V_{IN}=15V$		0.1		10 <sup>-5</sup>	0.1		1.0	μА
	LOW Level Output Voltage  HIGH Level Output Voltage  LOW Level Input Voltage  HIGH Level Input Voltage  LOW Level Output Current (Note 7)  HIGH Level Output Current (Note 7)	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Parameter   Conditions   Min	Parameter   Conditions   Min   Max	Parameter   Conditions   Min   Max   Min	Parameter   Conditions   Min   Max   Min   Typ	Parameter   Conditions   Min   Max   Min   Typ   Max	Conditions         Min         Max         Min         Typ         Max         Min           Quiescent Device Current         V <sub>DD</sub> = 5V, V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub> V <sub>DD</sub> = 15V, V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub> 1         1         1         2         2         2         2         2         4	Parameter   Conditions   Min   Max   Min   Typ   Max   Min   Max

Note 6: V<sub>SS</sub> = 0V unless otherwise specified.

Note 7:  $I_{OH}$  and  $I_{OL}$  are tested one output at a time.

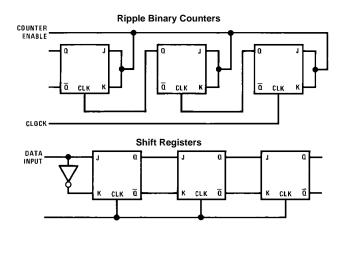
# AC Electrical Characteristics (Note 8) ${\rm T_A=25^{\circ}C,\ C_L=50\ pF,\ t_{rCL}=t_{fCL}=20\ ns,\ unless\ otherwise\ specified}$

Symbol	Parameter	Conditions	Min	Тур	Max	Units
t <sub>PHL</sub> or t <sub>PLH</sub>	Propagation Delay Time	V <sub>DD</sub> = 5V		200	400	
	from Clock to Q or Q	$V_{DD} = 10V$		80	160	ns
		$V_{DD} = 15V$		65	130	
t <sub>PHL</sub> or t <sub>PLH</sub>	Propagation Delay Time	$V_{DD} = 5V$		170	340	
	from Set to Q or Reset to Q	$V_{DD} = 10V$		70	140	ns
		$V_{DD} = 15V$		55	110	
t <sub>PHL</sub> or t <sub>PLH</sub>	Propagation Delay Time	$V_{DD} = 5V$		110	220	
	from Set to Q or	$V_{DD} = 10V$		50	100	ns
	Reset to Q	$V_{DD} = 15V$		40	80	
t <sub>S</sub>	Minimum Data Setup Time	$V_{DD} = 5V$		135	270	
		$V_{DD} = 10V$		55	110	ns
		$V_{DD} = 15V$		45	90	
t <sub>THL</sub> or t <sub>TLH</sub>	Transition Time	$V_{DD} = 5V$		100	200	
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	
f <sub>CL</sub>	Maximum Clock Frequency	V <sub>DD</sub> = 5V	2.5	5		
	(Toggle Mode)	$V_{DD} = 10V$	6.2	12.5		MHz
		$V_{DD} = 15V$	7.6	15.5		
t <sub>rCL</sub> or t <sub>fCL</sub>	Maximum Clock Rise	$V_{DD} = 5V$	15			
	and Fall Time	$V_{DD} = 10V$	10			μs
		$V_{DD} = 15V$	5			
t <sub>W</sub>	Minimum Clock Pulse	$V_{DD} = 5V$		100	200	
	Width (t <sub>WH</sub> = t <sub>WL</sub> )	$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		32	65	
t <sub>WH</sub>	Minimum Set and	V <sub>DD</sub> = 5V		80	160	
	Reset Pulse Width	$V_{DD} = 10V$		30	60	ns
		$V_{DD} = 15V$		25	50	
C <sub>IN</sub>	Average Input Capacitance	Any Input		5	7.5	pF
C <sub>PD</sub>	Power Dissipation Capacity	Per Flip-Flop		35		pF
		(Note 9)				

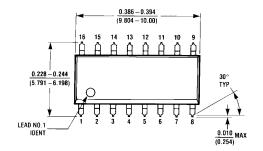
Note 8: AC Parameters are guaranteed by DC correlated testing.

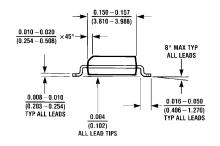
Note 9: C<sub>PD</sub> determines the no load AC power consumption of any CMOS device. For complete explanation, see 74C Family Characteristics application

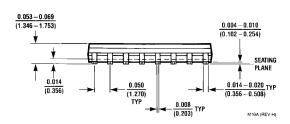
## **Typical Applications**



## Physical Dimensions inches (millimeters) unless otherwise noted







16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A

### Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.090 (18.80 - 19.81)(2.286)**16 15 14 13 12 11 10 9** 16 15 INDEX AREA 0.250 ± 0.010 $\overline{(6.350 \pm 0.254)}$ PIN NO. 1 PIN NO. 1 1 2 3 4 5 6 7 8 1 2 OPTION 01 OPTION 02 0.065 $\frac{0.130 \pm 0.005}{(3.302 \pm 0.127)}$ $\frac{0.060}{(1.524)}$ TYP 4° TYP OPTIONAL 0.300 - 0.320(1.651)(7.620 - 8.128) 0.145 - 0.200 (3.683 - 5.080)95°±5° 0.008 = 0.016 (0.203 = 0.406) TYP $\frac{0.280}{(7.112)}$ (0.508)0.125 - 0.150 (3.175 - 3.810) $0.030 \pm 0.015$ MIN $(0.762 \pm 0.381)$ 0.014 = 0.023 (0.356 = 0.584) 0.100 ± 0.010 (0.325 +0.040 -0.015 $(2.540 \pm 0.254)$

16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

0.050 ± 0.010

(1.270 ± 0.254)

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

## LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- 1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- 2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com

N16E (REV F)