



# Series 54/74

**DM7280/DM8280(S8280/N8280) presetable decade counter**  
**DM7281/DM8281(S8281/N8281) presetable binary counter**  
**DM7288/DM8288(S8288/N8288) presetable  $\div 12$  counter**

## general description

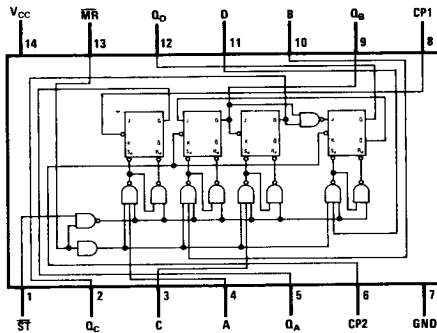
The counters in this series are four-bit monolithic subsystems containing a divide-by-two counter with one clock input and a second counter with a second clock input. The two clock inputs and the other logic functions provided will implement a wide variety of counter and storage register functions.

## features

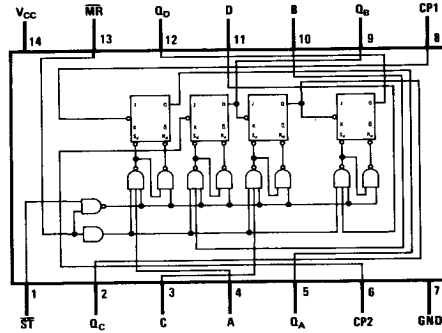
- Series 54/74 compatible

- Two clock inputs for additional flexibility
- Strobed parallel-entry capability
- Reset inputs common to all stages
- Typical toggle rates to 45 MHz
- Typical power dissipation of 130 mW
- Direct-coupled stages
- Available in cavity or molded DIP

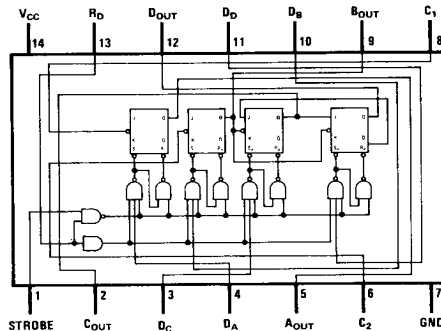
## connection diagrams (Dual-In-Line Packages)



DM7280/DM8280  
(DM54176/DM74176)



DM7281/DM8281  
(DM54177/DM74177)



DM7288/DM8288

### absolute maximum ratings

Supply Voltage	7V
Input Voltage	5.5V
Operating Temperature Range	
DM7280, DM7281, DM7288	-55°C to +125°C
DM8280, DM8281, DM8288	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

### electrical characteristics (Notes 1, 2)

CHARACTERISTICS	LIMITS				TEMP	V <sub>CC</sub>	DATA STROBE	DATA INPUTS	RESET	CLOCK 1	CLOCK 2	OUTPUTS
	MIN	TYP	MAX	UNITS								
"1" Output Voltage <sup>(3)(4)</sup>	2.6			V	0°C	4.75V	0.8V	2.0V	2.0V			Output A
	2.8			V	+25°C	5.0V	0.8V	2.0V	2.0V			Output A
	2.6			V	+75°C	4.75V	0.8V	2.0V	2.0V			Output A
"0" Output Voltage <sup>(3)(5)</sup>			0.4	V	0°C	4.75V	0.8V	0.8V	0.8V			Output A
			0.4	V	+25°C	5.0V	0.8V	0.8V	0.8V			Output A
			0.4	V	+75°C	4.75V	0.8V	0.8V	0.8V			Output A
"0" Input Current												
Data Strobe	-0.1		-1.6	mA	+25°C	5.25V	0.4V					
Data Inputs	-0.1		-1.2	mA	+25°C	5.25V		0.4V				
Reset (DM8280, DM8281)	-0.1		-3.0	mA	+25°C	5.25V			0.4V			
Reset (DM8288)	-0.1		-2.8	mA	+25°C	5.25V			0.4V			
Clock <sub>1</sub> (DM8280, DM8281)	-0.1		-3.2	mA	+25°C	5.25V				0.4V		
Clock <sub>1</sub> (DM8288)	-0.1		-1.6	mA	+25°C	5.25V				0.4V		
Clock <sub>2</sub> (DM8280)	-0.1		-3.2	mA	+25°C	5.25V					0.4V	
Clock <sub>2</sub> (DM8281, DM8288)	-0.1		-1.6	mA	+25°C	5.25V					0.4V	
"1" Input Current												
Data Strobe			25	μA	+75°C	5.0V	4.5V					
Data Input			25	μA	+75°C	5.0V		4.5V				
Reset (DM8280, DM8281)			75	μA	+75°C	5.0V			4.5V			
Reset (DM8288)			50	μA	+75°C	5.0V			4.5V			
Clock <sub>1</sub>			75	μA	+75°C	5.0V				4.5V		
Clock <sub>2</sub>			75	μA	+75°C	5.0V					4.5V	
Clock Mode T <sub>ON</sub> Delay												
Bit A			25	ns	+25°C	5.0V						6.4 mA
Bit B, C, D			25	ns	+25°C	5.0V						
Clock Mode T <sub>OFF</sub> Delay												
Bit A			25	ns	+25°C	5.0V						6.4 mA
Bit B, C, D			25	ns	+25°C	5.0V						
Data/Strobe T <sub>ON</sub> Delay												
Bit A, B, C, D			35	ns	+25°C	5.0V						6.4 mA
Data/Strobe T <sub>OFF</sub> Delay												
Bit A, B, C, D			45	ns	+25°C	5.0V						6.4 mA
Toggle Rate	20	45		MHz	+25°C	5.0V						6.4 mA
		35		MHz	+25°C	5.0V						6.4 mA
Clock Mode Switching Test <sup>(6)</sup>			∞	ns	+25°C	5.0V				Pulse	Pulse	
Output Fall Time			50	nA	+25°C	4.75V						100 pF
Power Consumption		130	194	mW	+25°C	5.25V			0V	0V	0V	
Input Voltage Rating												
Data Strobe	5.5			V	+25°C	5.0V	10 mA					
Data Inputs	5.5			V	+25°C	5.0V		10 mA				
Reset	5.5			V	+25°C	5.0V			10 mA			
Output Short Circuit												
Current	-10		-60	mA	+25°C	5.0V	0V				0V	
Input Capacitance			3.0	pF	+25°C	5.0V						
Strobe Memory Holding												
Time with "1" to "0"		17	35	ns	+25°C	5.0V		0.8V	2.0V	2.0V		Output A
Clock or Output												
Transition												
With no "1" to "0"		17	35	ns	+25°C	5.0V		2.0V	2.0V	2.0V		Output A
Clock or Output												
Transition												
Strobe Pulse Width	25			ns	+25°C	5.0V		0.8V	2.0V	2.0V		Output A
Reset Pulse Width	30			ns	+25°C	5.0V	2.0V	0.8V		2.0V		Output A

**Note 1:** All voltage and capacitance measurements are referenced to the ground terminal. Terminals that are not specifically referenced are left electrically open.

**Note 2:** Positive current flow is defined as the current into the referenced terminal.

**Note 3:** Measurements of each output and the associated data input apply independently.

**Note 4:** Output source current is supplied through a resistor to ground.

**Note 5:** Output sink current is supplied through a resistor to V<sub>CC</sub>.

**Note 6:** The unit will tolerate any fall time on the clock due to the DC design.

## general description (cont.)

The DM7280/DM8280 counter operates as a divide-by-two and divide-by-five counter with no external connections. When the A output is connected to the Clock 2 input, it counts in the familiar BCD mode. The bi-quinary mode is obtained by connecting the D output to the Clock 1 input while applying the clock to the Clock 2 input. This produces a square-wave output at  $f/10$  on the A output that is particularly useful in frequency synthesizers.

The DM7281/DM8281 is a 2,2,4,8 counter when operated with two clock inputs and no external connections. It is a 2,4,8,16 counter when the A output is connected to the Clock 2 input. Thus, it may be used as a divide-by-two, -eight, or -sixteen counter.

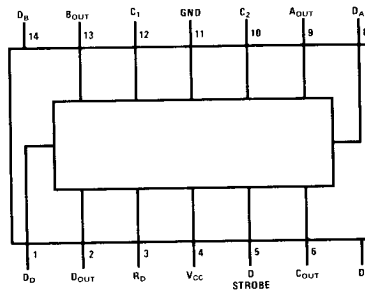
The DM7288/DM8288 consists of divide-by-two and divide-by-six counters. For divide-by-twelve operation, output A is connected to the Clock 2 input.

Counting is performed on the negative-going edge of the clock pulse in all three types. The divide-by-two stages may be toggled at up to 45 MHz, typical, approximately twice the maximum frequency of the Clock 2 input.

All three have parallel inputs which may be used to set the corresponding outputs to desired states. The parallel input logic levels are transferred to the outputs when the strobe line is placed at the logical "0" level. A "0" on the reset line will place all four outputs in the "0" state.

The register-storage function can be obtained by using the strobed parallel-entry capability. Data to be stored is entered by the method indicated above and retained on the outputs holding both clock inputs at logical "1" ( $V_{CC}$ ). The register may be reloaded with a new parallel entry and strobe operation or cleared by the reset line.

## connection diagram (Flat Package)



DM7280/DM8280, DM7281/DM8281, DM7288/DM8288  
(Not applicable to DM54176W or DM54177W)