TC74LCX157F/FN/FS

PRELIMINARY

Low-Voltage Quad 2-CHANNEL MULTIPLEXER with 5V Tolerant Inputs and Outputs

The TC74LCX157 is a high performance CMOS 2-CHANNEL MULTIPLEXER. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaning the CMOS low power dissipation.

The device is designed for low voltage (3.3V) V_{CC} applications, but it could be used to interface to 5V supply environment for inputs.

This device consists of four 2-input digital multiplexers with common select and strobe inputs.

When the $\overline{STROBE}$ input is held "H" level, selection of data is inhibited and all outputs become "L" level.

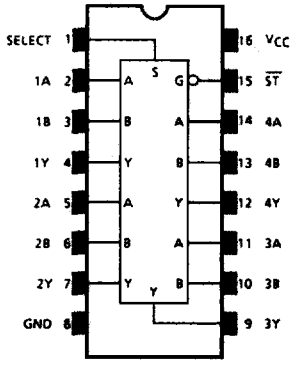
The SELECT decoding determines whether the A or B inputs get routed to their corresponding Y outputs.

All inputs are equipped with protection circuits against static discharge.

Features

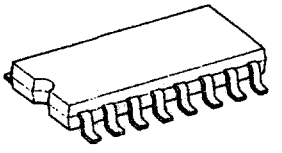
- Low Voltage Operation: V_{CC} = 2.0 ~ 3.6V
- High Speed: t_{pd} = 6.0ns (Max.) (V_{CC} = 3.0 ~ 3.6V)
- Output Current: $|I_{OH}|/I_{OL}$ = 24mA (Min.) (V_{CC} = 3.0V)
- Latch up Performance: ±500mA
- Available in JEDEC SOP, EIAJ SOP and SSOP
- Power down protection is provided on all inputs and outputs
- Pin and Function Compatible with 74 series
  - (74AC/VHC/HC/F/ALS/LS, etc.) 157 type

Pin Connection



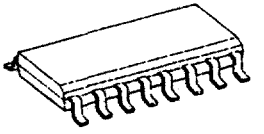
(TOP VIEW)

TC74LCX157F



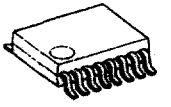
SOP16-P-300

TC74LCX157FN



SOL16-P-150

TC74LCX157FS

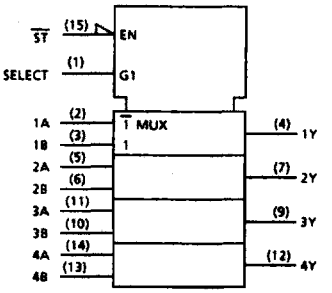


SSOP16-P-225B

Weight SOP16-P-300 : 0.18g (Typ.)
SOL16-P-150 : 0.12g (Typ.)
SSOP16-P-225B : 0.07g (Typ.)

Pin Assignment

IEC Logic Symbol

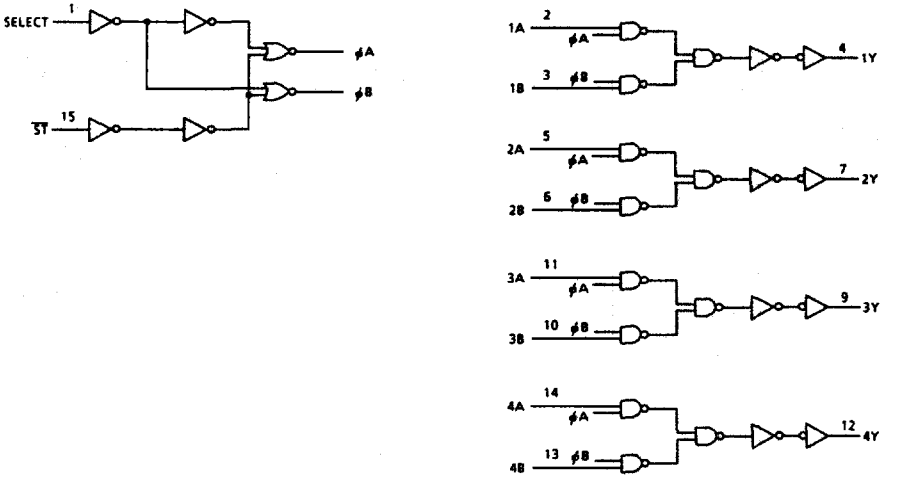


Truth Table

Inputs				Outputs
$\overline{ST}$	Select	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

X: Don't Care

System Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	-0.5 ~ 7.0	V
DC Input Voltage	V_{IN}	-0.5 ~ 7.0	V
DC Output Voltage	V_{OUT}	-0.5 ~ 7.0 (Note 1)	V
		-0.5 ~ V_{CC} + 0.5 (Note 2)	
Input Diode Current	I_{IK}	-50	mA
Output Diode Current	I_{OK}	±50 (Note 3)	mA
DC Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	180	mW
DC V_{CC}/Ground Current	I_{CC}/I_{GND}	±100	mA
Storage Temperature	T_{stg}	-65 ~ 150	°C

(Note 1) Off-State
(Note 2) High or Low State. I_{OUT} absolute maximum rating must be observed.
(Note 3) V_{OUT} < GND, V_{OUT} > V_{CC}

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	2.0 ~ 3.6	V
		1.5 ~ 3.6 (Note 4)	
Input Voltage	V_{IN}	0 ~ 5.5	V
Bus Output Voltage	V_{OUT}	0 ~ 5.5 (Note 5)	V
		0 ~ V_{CC} (Note 6)	
Output Current	I_{OH}/I_{OL}	±24 (Note 7)	mA
		±12 (Note 8)	
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	dt/dv	0 ~ 10 (Note 9)	ns/V

(Note 4) Data Retension Only
(Note 5) Off-State
(Note 6) High or Low State
(Note 7) V_{CC} = 3.0 ~ 3.6V
(Note 8) V_{CC} = 2.7 ~ 3.0V
(Note 9) V_{IN} = 0.8 ~ 2.0V, V_{CC} = 3.0V

Electrical Characteristics

DC Characteristics (Ta = -40 ~ 85°C)

Parameter		Symbol	Test Condition		V_{CC} (V)	Min.	Max.	Unit
Input Voltage	"H" Level	V_{IH}	–		2.7 ~ 3.6	2.0	–	V
	"L" Level	V_{IL}	–		2.7 ~ 3.6	–	0.8	V
Output Voltage	"H" Level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -100μA	2.7 ~ 3.6	V_{CC} - 0.2	–	V
				I_{OH} = -12mA	2.7	2.2	–	
				I_{OH} = -18mA	3.0	2.4	–	
				I_{OH} = -24mA	3.0	2.2	–	
	"L" Level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = 100μA	2.7 ~ 3.6	–	0.2	V
				I_{OL} = 12mA	2.7	–	0.4	
				I_{OL} = 16mA	3.0	–	0.4	
				I_{OH} = 24mA	3.0	–	0.55	
Input Leakage Current		I_{IN}	V_{IN} = 0 ~ 5.5V		2.7 ~ 3.6	–	±5.0	μA
Power Off Leakage Current		I_{OFF}	V_{IN}/V_{OUT} = 5.5V		0	–	10.0	μA
Quiescent Supply Current		I_{CC}	V_{IN} = V_{CC} or GND		2.7 ~ 3.6	–	10.0	μA
			V_{IN}/V_{OUT} = 3.6 ~ 5.5V		2.7 ~ 3.6	–	±10.0	
Increase in I_{CC} per Input		ΔI_{CC}	V_{IH} = V_{CC} - 0.6V		2.7 ~ 3.6	–	500	μA

AC Characteristics (Ta = -40 ~ 85°C)

Parameter	Symbol	Test Condition	V_{CC} (V)	Min.	Max.	Unit
Propagation Delay Time (A, B-Y)	t_{pLH} t_{pHL}	(Fig. 1, 2)	2.7	–	6.5	ns
			3.3 ± 0.3	1.5	6.0	
Propagation Delay Time (SELECT-Y)	t_{pLH} t_{pHL}	(Fig. 1, 2)	2.7	–	8.0	ns
			3.3 ± 0.3	1.5	7.0	
Propagation Delay Time ($\overline{ST}$-Y)	t_{pLH} t_{pHL}	(Fig. 1, 2)	2.7	–	7.0	ns
			3.3 ± 0.3	1.5	8.0	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 10)	2.7	–	–	ns
			3.3 ± 0.3	–	1.0	

(Note 10) Parameter guaranteed by design. $t_{osLH} = (| t_{pLHm} - t_{pLHn} |, t_{osHL} = | t_{pHLm} - t_{pHLn} |)$

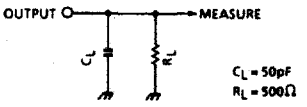
Capacitive Characteristics (Ta = 25°C)

Parameter	Symbol	Test Condition	V_{CC} (V)	Typical	Unit
Input Capacitance	C_{IN}	–	3.3	TBD	pF
Output Capacitance	C_{OUT}	–	3.3	TBD	pF
Power Dissipation Capacitance	C_{PD}	f_{IN} = 10MHz (Note 11)	3.3	TBD	pF

(Note 11) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = $C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}$

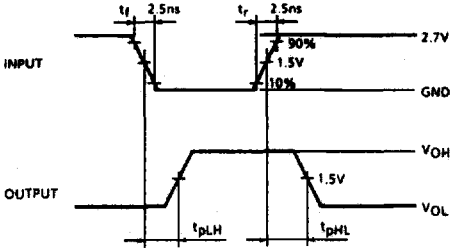
TEST CIRCUIT

Fig.1



AC WAVEFORM

Fig.2 t_{pLH}, t_{pHL}



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