32K x 8 RADIATION-HARDENED STATIC RAM HC6856

FEATURES

RADIATION

- Fabricated with RICMOS™ IV Bulk 0.8 μm Process
- Total Dose Hardness through $1x10^6$ rad(SiO_2)
- Neutron Hardness through $1x10^{14}$ cm^{-2}
- Dynamic and Static Transient Upset Hardness through $1x10^9$ rad(Si)/s
- Soft Error Rate of $<1x10^{-10}$ upsets/bit-day
- Dose Rate Survivability through $1x10^{12}$ rad(Si)/s
- Latchup Free

OTHER

- Read/Write Cycle Times ≤ 40 ns (-55 to 125°C)
- Standby Current of 20 μA (typical)
- Asynchronous Operation
- CMOS or TTL Compatible I/O
- Single 5 V ± 10% Power Supply
- Low Operating Power
- Packaging Options
  - 36-Lead Flat Pack (0.630 in. x 0.650 in.)
  - 28-Lead DIP (Std. 0.600 in. x 1.400 in.)

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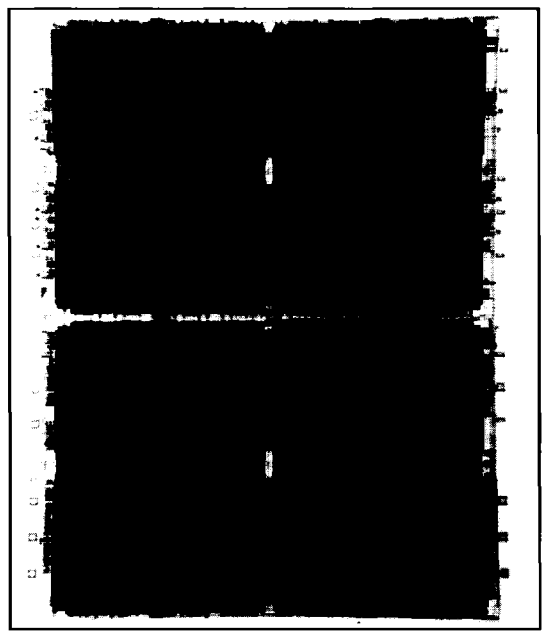
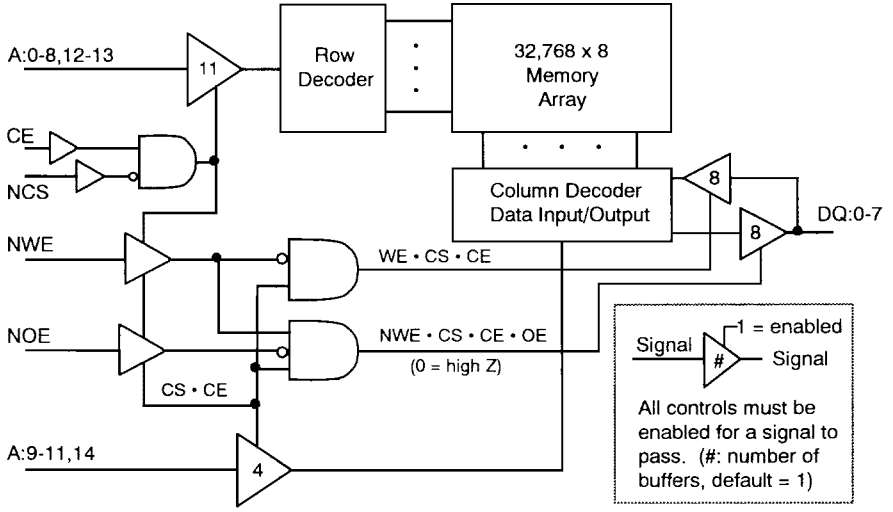
GENERAL DESCRIPTION

The 32K x 8 Radiation-Hardened Static RAM is a high performance 32,768 x 8-bit static random access memory with industry-standard functionality. It is fabricated with Honeywell's radiation-hardened technology, and is designed for use in systems operating in radiation environments. The RAM operates over the full military temperature range and requires only a single 5 V ± 10% power supply. The RAM is available with either TTL or CMOS compatible I/O. Power consumption is typically less than 50 mW/MHz in operation, and less than 5 mW/MHz in the low power disabled mode. The RAM read operation is fully asynchronous, with an associated typical access time of 20 ns.

Honeywell's enhanced RICMOS™IV (Radiation Insensitive CMOS) technology is radiation hardened through the use of advanced and proprietary design, layout, and process hardening techniques. The RICMOS™ IV process is a 5-volt, twin-well CMOS technology with a 170 Å gate oxide and a minimum feature size of 0.8 μm. Additional features include a three layer interconnect metalization and a lightly doped drain (LDD) structure for improved short channel reliability. High resistivity cross-coupled polysilicon resistors have been incorporated for single event upset hardening.



FUNCTIONAL DIAGRAM



SIGNAL DEFINITIONS

A: 0-14 Address input pins (A) which select a particular eight-bit word within the memory array.

DQ: 0-7 Bidirectional data pins which serve as data outputs during a read operation and as data inputs during a write operation.

NCS Negative chip select, when at a low level allows normal read or write operation. When at a high level it forces the SRAM to a precharge condition, holds the data output drivers in a high impedance state and disables all the input buffers. If this signal is not used it must be connected to VSS.

NWE Negative write enable, when at a low level activates a write operation and holds the data output drivers in a high impedance state. When at a high level it allows normal read operation.

NOE Negative output enable, when at a high level holds the data output drivers in a high impedance state. When at a low level, the data output driver state is defined by NCS, NWE and CE. If this signal is not used it must be connected to VSS.

CE Chip enable, when at a high level allows normal operation. When at a low level it forces the SRAM to a precharge condition, holds the data output drivers in a high impedance state and disables all the input buffers. If this signal is not used it must be connected to VDD.

TRUTH TABLE

NCS	CE	NWE	NOE	MODE	DQ
L	H	H	L	Read	Data Out
L	H	L	X	Write	Data In
H	X	XX	XX	Deselected	High Z
X	L	XX	XX	Disabled	High Z

Notes:
X: VI=VIH or VIL
XX: VSS≤VI≤VDD
NOE=H: High Z output state maintained for NCS=X, CE=X, NWE=X

RADIATION CHARACTERISTICS

Total Ionizing Radiation Dose

The RAM will meet all stated functional and electrical specifications over the entire operating temperature range after a total ionizing radiation dose of $1x10^6$ rad(SiO_2). All electrical and timing performance parameters will remain within specifications after rebound at VDD = 5.5 V and T =125°C extrapolated to ten years of operation. Total dose hardness is assured by wafer level testing of process monitor transistors and RAM product using 10 keV X-ray radiation. Transistor gate threshold shift correlations have been made between 10 keV X-rays applied at a dose rate of $1x10^5$ rad(SiO_2)/min at T = 25°C and gamma rays (Cobalt 60 source) to ensure that wafer level X-ray testing is consistent with standard military radiation test environments.

Transient Pulse Ionizing Radiation

The RAM is capable of writing, reading, and retaining stored data during and after exposure to a transient ionizing radiation pulse of ≤1 μs duration up to $1x10^9$ rad(Si)/s, when applied under recommended operating conditions. To ensure validity of all specified performance parameters before, during, and after radiation (timing degradation during transient pulse radiation is ≤10%), it is suggested that a minimum of 0.8 μF per part of stiffening capacitance be placed between the package (chip) VDD and VSS, with a maximum inductance between the package (chip) and stiffening capacitance of 0.7 nH per part. If there are no operate-through or valid stored data requirements, the capacitance specification can be reduced to a minimum of 0.1 μF per part.

The RAM will meet any functional or electrical specification after exposure to a radiation pulse of ≤ 50 ns duration up to $1x10^{12}$ rad(Si)/s, when applied under recommended operating conditions. Note that the current conducted during the pulse by the RAM inputs, outputs, and power supply may significantly exceed the normal operating levels. The application design must accommodate these effects.

Neutron Radiation

The RAM will meet any functional or timing specification after a total neutron fluence of up to $1x10^{14}$ cm^{-2} applied under recommended operating or storage conditions. This assumes an equivalent neutron energy of 1 MeV.

Soft Error Rate

The RAM is capable of soft error rate (SER) performance of $<1x10^{-10}$ upsets/bit-day, under recommended operating conditions. This hardness level is defined by the Adams 10% worst case cosmic ray environment.

Latchup

The RAM will not latch up due to any of the above radiation exposure conditions when applied under recommended operating conditions. Fabrication with the RICMOS™ p-epi on p+ substrate process and use of proven design techniques, such as double guardbanding, ensure latchup immunity.

RADIATION-HARDNESS RATINGS (1)

Parameter	Limits (2)	Units	Test Conditions
Total Dose	$\geq 1x10^6$	rad(SiO_2)	TA=25°C
Transient Dose Rate Upset (3)	$\geq 1x10^9$	rad(Si)/s	Pulse width≤1 μs
Transient Dose Rate Survivability	$\geq 1x10^{12}$	rad(Si)/s	Pulse width≤50 ns, X-ray, VDD=6.6 V, TA=25°C
Soft Error Rate: Level A	$<1x10^{-9}$ (4)	upsets/bit-day	Adams 10% worst case environment
Level Z	$<1x10^{-10}$		
Neutron Fluence	$\geq 1x10^{14}$	N/cm²	1 MeV equivalent energy, Unbiased, TA=25°C

(1) Device will not latch up due to any of the specified radiation exposure conditions.

(2) Operating conditions (unless otherwise specified): VDD=4.5 V to 5.5 V, TA=-55°C to 125°C.

(3) Suggested stiffening capacitance specifications for optimum expected dose rate upset performance is stated above in the text.

(4) SER $<1x10^{-10}$ u/b-d from -55 to 80°C.

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter		Rating Min	Rating Max	Units
VDD	Positive Supply Voltage (2)		-0.5	7.0	V
VPIN	Voltage on Any Pin (2)		-0.5	VDD+0.5	V
TSTORE	Storage Temperature (Zero Bias)		-65	150	°C
TSOLDER	Soldering Temperature • Time			270•5	°C•s
PD	Total Package Power Dissipation (3)			2.5	W
IOUT	DC or Average Output Current			25	mA
VPROT	ESD Input Protection Voltage (4)		2000		V
ΘJC	Thermal Resistance (Junction-to-Case)	36 FP		2	°C/W
		28 DIP		10	°C/W
TJ	Junction Temperature			175	°C

(1) Stresses in excess of those listed above may result in permanent damage. These are stress ratings only, and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.
(2) Voltage referenced to VSS.
(3) RAM power dissipation (IDDSB + IDDOP) plus RAM output driver power dissipation due to external loading must not exceed this specification.
(4) Class 2 electrostatic discharge (ESD) input protection. Tested per MIL-STD-883, Method 3015 by DESC certified lab.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Description Min	Description Typ	Description Max	Units
VDD	Supply Voltage (referenced to VSS)	4.5	5.0	5.5	V
TA	Ambient Temperature	-55	25	125	°C
VPIN	Voltage on Any Pin (referenced to VSS)	-0.3		VDD+0.3	V

CAPACITANCE (1)

Symbol	Parameter	Typical	Worst Case Min	Worst Case Max	Units	Test Conditions
CI	Input Capacitance	4		6	pF	VI=VDD or VSS, f=1 MHz
CO	Output Capacitance	6.5		8	pF	VIO=VDD or VSS, f=1 MHz

(1) This parameter is tested during initial design characterization only.

DATA RETENTION CHARACTERISTICS

Symbol	Parameter (2)	Typical (1)	Worst Case Min	Worst Case Max	Units	Test Conditions
VDR	Data Retention Voltage (3)	2.0	2.5		V	NCS=VDR VI=VDR or VSS
IDR	Data Retention Current	150		400	µA	NCS=VDD=VDR VI=VDR or VSS

(1) Typical operating conditions: TA= 25°C, pre-radiation.
(2) Worst case operating conditions: TA= -55°C to +125°C, total dose through $1x10^6$ rad(SiO_2) at 25°C.
(3) To maintain valid data storage during transient radiation, VDD must be held within the recommended operating range.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Typical (1)	Worst Case (2) Min	Worst Case (2) Max	Units	Test Conditions (3)
IDDSB1	Static Supply Current		0.02		1.2	mA	VIH=VDD IO=0 VIL=VSS Inputs Stable
IDDSB2	Static Supply Current with Chip Disabled		0.02		1.2	mA	CE=VSS or NCS=VDD IO=0, VSS≤ VI≤VDD (4)
IDDSEIL	Static Supply Current per Enabled Input*-Low		6		30	µA	VDD=5.5V, VIL=0.5V (4)
IDDSEIH	Static Supply Current per Enabled Input*-High		6		30	µA	VDD=5.5V, VIH=VDD-0.5V (4)
IDDOPW	Dynamic Supply Current, Selected (Write)		5.5		7.5	mA	f=1 MHz, IO=0, CE=VIH=VDD NCS=VIL=VSS (5)
IDDOPR	Dynamic Supply Current, Selected (Read)		4.5		6.5	mA	f=1 MHz, IO=0, CE=VIH=VDD NCS=VIL=VSS (5)
IDDOP1	Dynamic Supply Current, Deselected		5		20	µA	f=1 MHz, IO=0, VIL=VSS NCS=CE=VIH=VDD (5)
IDDOP2	Dynamic Supply Current, Disabled		5		20	µA	f=1 MHz, IO=0, VIH=VDD NCS=CE=VIL=VSS (5)
II	Input Leakage Current		±0.05	-5	+5	µA	VSS≤VI≤VDD
IOZ	Output Leakage Current		±0.1	-10	10	µA	VSS≤VIO≤VDD Output=high Z
VIL	Low-Level InputVoltage	CMOS TTL	1.9 1.3		1.5 0.8	V V	VDD=4.5V VDD=4.5V
VIH	High-Level Input Voltage	CMOS TTL	3.0 1.7	3.5 2.2		V V	VDD=5.5V VDD=5.5V
VOL	Low-Level Output Voltage		0.2		0.4 0.05	V V	VDD=4.5V, IOL=10 mA VDD=4.5V, IOL=200 µA
VOH	High-Level Output Voltage		4.8	4.2 VDD-0.05		V V	VDD=4.5V, IOH=-5 mA VDD=4.5V, IOH=-200 µA

(1) Typical operating conditions: VDD= 5.0 V,TA=25°C, pre-radiation.

(2) Worst case operating conditions: VDD=4.5 V to 5.5 V, TA=-55°C to +125°C, total dose through $1x10^6$ rad(SiO_2) at 25°C.

(3) Input high = VIH ≥ VDD-0.3V, input low =VIL ≤ 0.3V

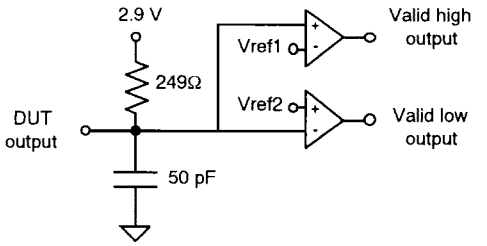
(4) Guaranteed but not tested.

(5) All inputs switching. DC average current.

* ENABLED INPUT PINS TRUTH TABLE

CE	NCS	NWE	# of enabled input pins
H	L	L	27
H	L	H	19
X	H	X	2
L	X	X	2

X: VI = VIH OR VIL

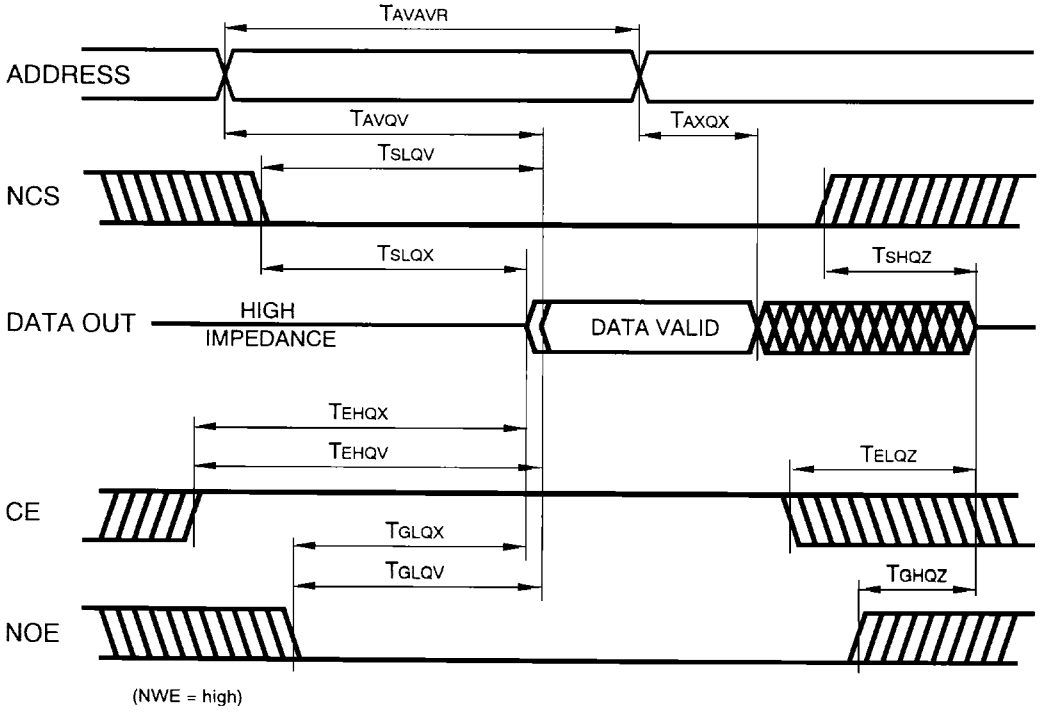


Tester Equivalent Load Circuit

READ CYCLE AC TIMING CHARACTERISTICS (1)

Symbol	Parameter	Typical (2)	Worst Case (3) -55 to 125°C Min	Worst Case (3) -55 to 125°C Max	Units
TAVAVR	Address Read Cycle Time	18	40		ns
TAVQV	Address Access Time	18		40	ns
TAXQX	Address Change to Output Invalid Time	15	5		ns
TSLQV	Chip Select Access Time	20		40	ns
TSLQX	Chip Select Output Enable Time	20	5		ns
TSHQZ	Chip Select Output Disable Time	6		15	ns
TEHQV	Chip Enable Access Time	20		40	ns
TEHQX	Chip Enable Output Enable Time	20	5		ns
TELQZ	Chip Enable Output Disable Time	6		15	ns
TGLQV	Output Enable Access Time	4		10	ns
TGLQX	Output Enable Output Enable Time	3	0		ns
TGHQZ	Output Enable Output Disable Time	4		10	ns

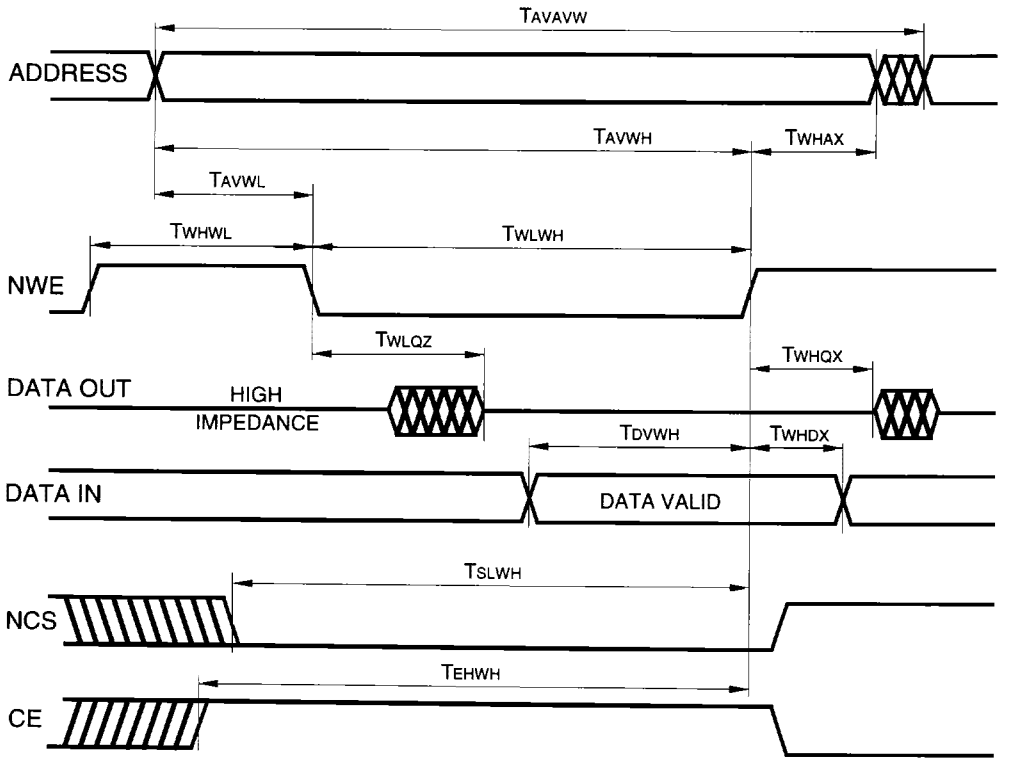
(1) Test conditions: input switching levels VIL/VIH=0.5V/VDD-0.5V (CMOS), VIL/VIH=0V/3V (TTL), input rise and fall times <5 ns, input and output timing reference levels shown in the Tester AC Timing Characteristics table, capacitive output loading C_L=50 pF. For C_L >50 pF, derate access times by 0.02 ns/pF (typical).
(2) Typical operating conditions: VDD=5.0 V, TA=25°C, pre-radiation.
(3) Worst case operating conditions: VDD=4.5 V to 5.5 V, total dose through 1x10^6 rad(SiO_2) at 25°C.



WRITE CYCLE AC TIMING CHARACTERISTICS (1)

Symbol	Parameter	Typical	Worst Case (3)				Units
			SER <1E-9 (4)		SER <1E-10		
		(2)	Min	Max	Min	Max	
TAVAVW	Write Cycle Time (5)	30	40		60		ns
TWLWH	Write Enable Write Pulse Width	25	35		55		ns
TSLWH	Chip Select to End of Write Time	25	35		55		ns
TDVWH	Data Valid to End of Write Time	20	30		50		ns
TAVWH	Address Valid to End of Write Time	25	35		55		ns
TWHDX	Data Hold Time after End of Write Time	0	0		0		ns
TAVWL	Address Valid Setup to Start of Write Time	0	0		0		ns
TWHAX	Address Valid Hold after End of Write Time	0	0		0		ns
TWLQZ	Write Enable to Output Disable Time	5	0	10	0	10	ns
TWHQX	Write Disable to Output Enable Time	15	5		5		ns
TWHWL	Write Disable to Write Enable Pulse Width	4	5		5		ns
TEHWH	Chip Enable to End of Write Time	25	35		55		ns

(1) Test conditions: input switching levels VIL/VIH=0.5V/VDD-0.5V (CMOS), VIL/VIH=0V/3V (TTL), input rise and fall times <5 ns, input and output timing reference levels shown in the Tester AC Timing Characteristics table, capacitive output loading=50 pF.
(2) Typical operating conditions: VDD=5.0 V, TA=25°C, pre-radiation.
(3) Worst case operating conditions: VDD=4.5 V to 5.5 V, -55 to 125°C, total dose through $1x10^6$ rad(SiO_2) at 25°C.
(4) SER ≤1E-10 u/b-d from -55 to 80°C.
(5) TAVAV = TWLWH + TWHWL



DYNAMIC ELECTRICAL CHARACTERISTICS

Read Cycle

The RAM is asynchronous in operation, allowing the read cycle to be controlled by address, chip select (NCS), or chip enable (CE) (refer to Read Cycle timing diagram). To perform a valid read operation, both chip select and output enable (NOE) must be low and chip enable and write enable (NWE) must be high. The output drivers can be controlled independently by the NOE signal. Consecutive read cycles can be executed with NCS held continuously low, and with CE held continuously high.

For an address activated read cycle, NCS and CE must be valid prior to or coincident with the activating address edge transition(s). Any amount of toggling or skew between address edge transitions is permissible; however, data outputs will become valid TAVQV time following the latest occurring address edge transition. The minimum address activated read cycle time is TAVAV. When the RAM is operated at the minimum address activated read cycle time, the data outputs will remain valid on the RAM I/O until TAXQX time following the next sequential address transition.

To control a read cycle with NCS, all addresses and CE must be valid prior to or coincident with the enabling NCS edge transition. Address or CE edge transitions can occur later than the specified setup times to NCS, however, the valid data access time will be delayed. Any address edge transition, which occurs during the time when NCS is low, will initiate a new read access, and data outputs will not become valid until TAVQV time following the address edge transition. Data outputs will enter a high impedance state TSHQZ time following a disabling NCS edge transition.

To control a read cycle with CE, all addresses and NCS must be valid prior to or coincident with the enabling CE edge transition. Address or NCS edge transitions can occur later than the specified setup times to CE; however, the valid data access time will be delayed. Any address edge transition which occurs during the time when CE is high will initiate a new read access, and data outputs will not become valid until TAVQV time following the address edge transition. Data outputs will enter a high impedance state TELQZ time following a disabling CE edge transition.

Write Cycle

The write operation is synchronous with respect to the address bits, and control is governed by write enable (NWE), chip select (NCS), or chip enable (CE) edge transitions (refer to Write Cycle timing diagrams). To perform a write operation, both NWE and NCS must be low, and CE must be high. Consecutive write cycles can be performed with NWE or NCS held continuously low, or CE held continuously high. At least one of the control signals must transition to the opposite state between consecutive write operations.

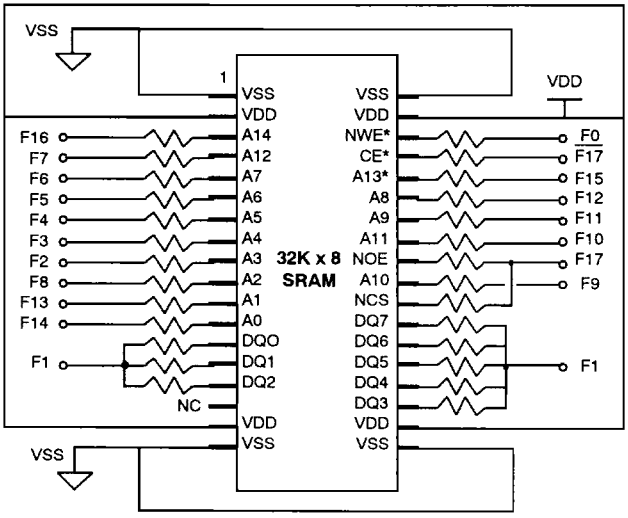
The write mode can be controlled via three different control signals: NWE, NCS, and CE. All three modes of control are similar except the NCS and CE controlled modes actually disable the RAM during the write recovery pulse. Only the NWE controlled mode is shown in the table and diagram on the previous page for simplicity. However, each mode of control provides the same write cycle timing characteristics. Thus, some of the parameter names referenced below are not shown in the write cycle table or diagram, but indicate which control pin is in control as it switches high or low.

To write data into the RAM, NWE and NCS must be held low and CE must be held high for at least TWLWH/TSLSH/TEHEL time. Any amount of edge skew between the signals can be tolerated, and any one of the control signals can initiate or terminate the write operation. For consecutive write operations, write pulses must be separated by the minimum specified TWHWL/TSHSL/TELEH time. Address inputs must be valid at least TAVWL/TAVSL/TAVEH time before the enabling NWE/NCS/CE edge transition, and must remain valid during the entire write time. A valid data overlap of write pulse width time of TDVWH/TDVSH/TDVEL, and an address valid to end of write time of TAVWH/TAVSH/TAVEL also must be provided for during the write operation. Hold times for address inputs and data inputs with respect to the disabling NWE/NCS/CE edge transition must be a minimum of TWHAX/TSHAX/TELAX time and TWHDX/TSHDX/TELDX time, respectively. The minimum write cycle time is TAVAV.

TESTER AC TIMING CHARACTERISTICS

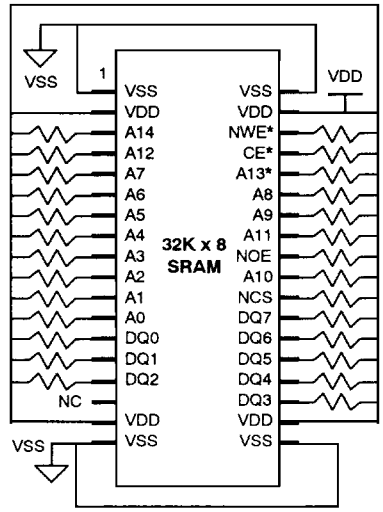
	TTL I/O Configuration	CMOS I/O Configuration
Input Levels*	3 V, 0 V, 1.5 V	VDD-0.5 V, 0.5 V, VDD/2
Output Sense Levels	1.5 V VDD-0.4V, 0.4 V, High Z High Z, 3.4 V, 2.4 V High Z = 2.9V	VDD/2 VDD-0.4V, 0.4 V, High Z High Z, 3.4 V, 2.4 V High Z = 2.9V

* Input rise and fall times <5 ns



DYNAMIC BURN-IN DIAGRAM

VDD = 5.5V, R ≤ 10 KΩ, VIH = VDD, VIL = VSS
Ambient Temperature ≥ 125 °C, F0 ≥ 100 KHz Sq Wave
Frequency of F1 = F0/2, F2 = F0/4, F3 = F0/8, etc.



STATIC BURN-IN DIAGRAM

VDD = 5.5V, R ≤ 10 KΩ
Ambient Temperature ≥ 125 °C

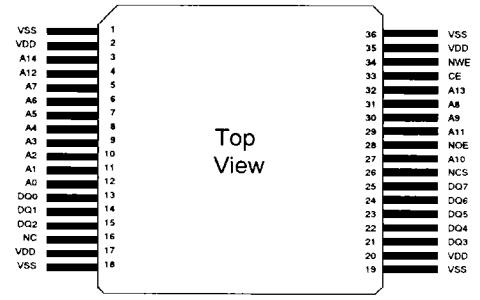
NOTE - Package pinout option dependent
(28-Lead DIP diagrams not shown but have similar connections)

PACKAGING

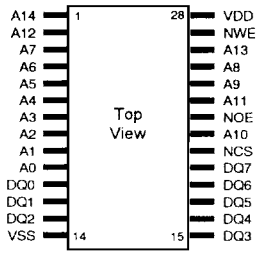
The 32K x 8 SOI SRAM is offered in a custom 36-lead flat pack or standard 28-lead DIP. Both packages are constructed of multilayer ceramic (Al_2O_3) and feature internal power and ground planes. The 36-lead FP also features a non-conductive ceramic tie bar on the lead frame. The purpose of the tie bar is to allow electrical testing of the device, while preserving the lead integrity during shipping and handling, up to the point of lead forming and insertion.

Optional capacitors can be mounted to the package to maximize supply noise decoupling and increase board packing density. These capacitors attach directly to the internal package power and ground planes. This design minimizes resistance and inductance of the bond wire and package, both of which are critical in a transient radiation environment. All NC pins must be connected to either VDD, VSS or an active driver to prevent charge build up in the radiation environment. (NC = no connect)

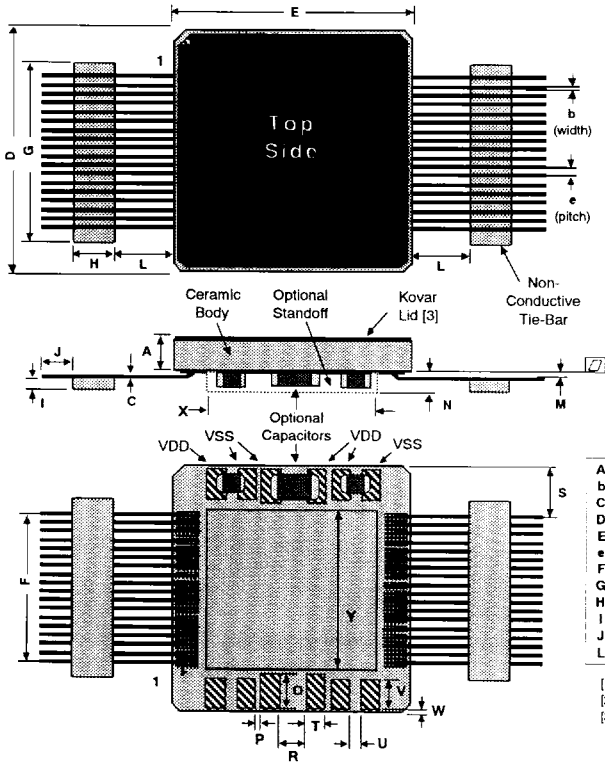
36-LEAD FLAT PACK PINOUT



28-LEAD DIP PINOUT



36-LEAD FLAT PACK

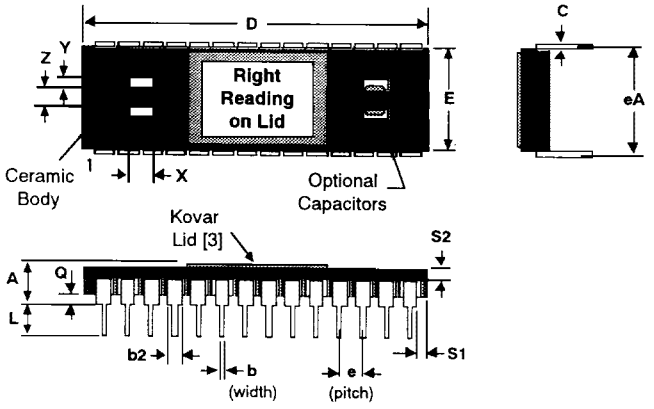


All dimensions are in inches [1]

A	0.095 ± 0.010	M	0.008 ± 0.003
b	0.008 ± 0.002	N	0.050 ± 0.010
C	0.005 to 0.0075	O	0.090 ref
D	0.650 ± 0.010	P	0.015 ref
E	0.630 ± 0.007	R	0.075 ref
e	0.025 ± 0.002 [2]	S	0.113 ± 0.010
F	0.425 ± 0.005 [2]	T	0.050 ref
G	0.525 ± 0.005	U	0.030 ref
H	0.135 ± 0.005	V	0.080 ref
I	0.030 ± 0.005	W	0.005 ref
J	0.080 typ.	X	0.450 ref
L	0.285 ± 0.015	Y	0.400 ref

[1] Parts delivered with leads unformed
[2] At tie bar
[3] Lid tied to VSS

28-LEAD DUAL IN-LINE PACKAGE (DIP)



All dimensions in inches [1]

A	0.175 (max)	L	0.125 to 0.200
b	0.020 ± 0.006	Q	0.015 to 0.060
b2	0.055 ± 0.010	S1	0.005 (min)
c	0.009 to 0.012	S2	0.005 (min)
D	1.400 ± 0.020	X	0.100 ref
E	0.595 ± 0.015	Y	0.050 ref
e	0.100 BSC [2]	Z	0.075 ref
eA	0.600 BSC [2]		

[1] Dimensions meet MIL-STD-1835, Config. C, D-10
[2] BSC - Basic lead Spacing between Centers
[3] Lid tied to VSS

3

ORDERING INFORMATION

H — **SOURCE**
H=HONEYWELL

C — **PROCESS**
C=CMOS

6856/1 — **PART NUMBER**
Pinout options (2)

X — **PACKAGE DESIGNATION**
W=36-Lead Flat Pack, without standoff, without capacitors
X=36-Lead Flat Pack, with standoff, without capacitors
Y=36-Lead Flat Pack, with standoff, with capacitors
R=28-Lead DIP without capacitors
S=28-Lead DIP with capacitors
- = Bare Die (No Package) (4)

S — **SCREEN LEVEL**
C=Brass Board
S=Modified Class S (1)

H — **RADIATION HARDNESS**
H=1x10^{6} rad(SiO$_2$)
R=2x10^{5} rad(SiO$_2$)

Z — **SOFT ERROR RATE**
Z <1x10^{-10} upsets/bit-day
A <1x10^{-9} upsets/bit-day (3)
- = SER is N/A (Brassboard)

C — **INPUT BUFFER TYPE**
C=CMOS Level
T=TTL Level

(1) Refer to Assembly and Screening Procedure section for Honeywell's screening procedures.
(2) Pinout options:

	pin 32	pin 33	pin 34
HC6856/1	A13	CE	NWE
HC6856/2	CE	NWE	A13

(3) SER <1E-10 u/b-d from -55 to 80°C.
(4) Contact factory for information regarding die sales.

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