Description

The GM76FV28 / GM76FU28 / GM76FS28 / GM76FR28 is a 2,097,152 bits static random access memory organized as 262,144 words by 8 bits. Using an advanced Full CMOS technology and it provides high speed operation with minimum cycle time of 55/70ns. The device is placed in a low power standby mode with $\overline{CS1}$ high or CS2 low and the output enable ($\overline{OE}$) allows fast memory access. Thus it is suitable for high speed and low super power applications, especially where battery back-up is required.

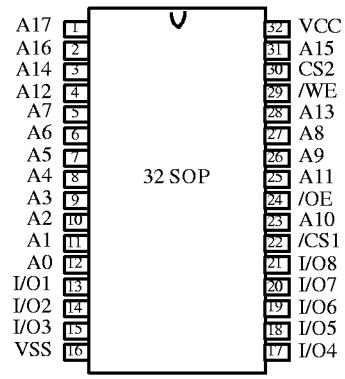
Features

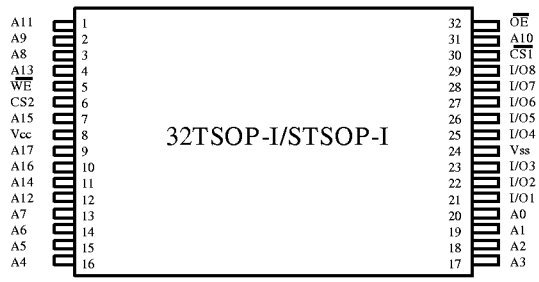
- Fast Speed : 55/70ns
- Power Supply /Speed
  GM76FV28 : 3.3V ± 0.3V / *55/70ns
  GM76FU28 : 3.0V ± 0.3V / *55/70ns
  GM76FS28 : 2.5V ± 0.2V / *70/85ns
  GM76FR28 : 2.0V ± 0.2V / *100/120ns
  * The parameter is measured with 30pF test load.
- Low Power Standby
  10uA(LL) / 2uA(SL)
- Completely Static RAM : No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- TTL compatible inputs and outputs
- Capability of Battery Back-up Operation
- Standard 32SOP and TSOP-I,STSOP-I
- Temperature Range
  Commercial (0 70°C)
  Industrial (-40 ~ 85°C)

Pin Description

Pin	Function
A0-A17	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS1}$, CS2	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O1-I/O8	Data Inputs/Outputs
Vcc	Power Supply (1.8V ~3.6V)
Vss	Ground
NC	No Connection

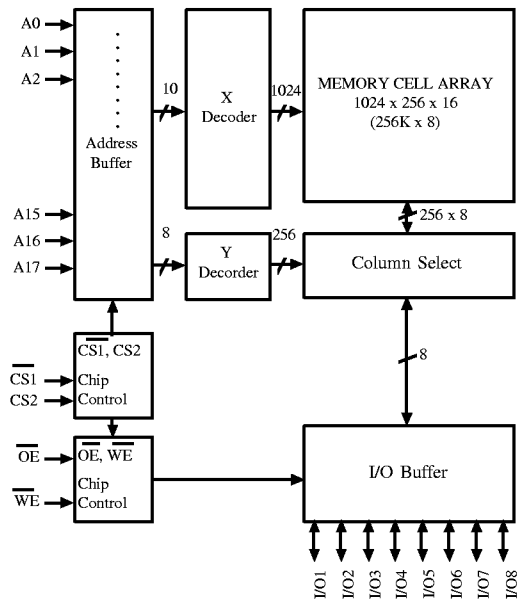
Pin Configuration





(Top View)

Block Diagram



Absolute Maximum Ratings*

Symbol	Parameter		Rating	Unit
T_A	Ambient Temperature under Bias	GM76FV28 GM76FU28 GM76FS28 GM76FR28	0 ~ 70	°C
		GM76FV28-I GM76FU28-I GM76FS28-I GM76FR28-I	-40 ~ 85	
T_{STG}	Storage Temperature		-55 ~ 150	°C
T_{SOL}	Soldering Temperature and Time		260, 10 (at lead)	°C, S
V_{CC}	Supply Voltage		-0.2 ~ 4.0**	V
V_{IN}	Input Voltage		-0.2 ~ 3.6 ***	V
$V_{I/O}$	Input and Output Voltage		-0.2 ~ 3.6 ***	V
P_D	Power Dissipation		1	W

*: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

** : Maximum Vcc = -0.2 to 4.6V for GM76FV28 -(I)

*** : $V_{IN}/V_{I/O}$ = -0.2 to 3.9V for GM76FV28 - (I)

Recommended DC Operating Conditions*

Symbol	Parameter	Product	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	GM76FV28 -(I) GM76FU28 -(I) GM76FS28 -(I) GM76FR28 -(I)	3.0 2.7 2.3 1.8	3.3 3.0 2.5 2.0	3.6 3.3 2.7 2.2	V
V_{IH}	Input High Voltage	GM76FV28 -(I) GM76FU28 -(I) GM76FS28 -(I) GM76FR28 -(I)	2.2 2.2 2.0 1.6	-	Vcc+ 0.2	V
V_{IL}	Input Low Voltage	All Product	-0.2**	-	0.4	V

* 1) Commercial Product : Ta = 0 ~ 70 °C, unless otherwise specified
2) Industrial Product : Ta = -40 ~ 85 °C, unless otherwise specified

** V_{IL}(min) = -1.5V for ≤ 30ns pulse

Truth Table

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	A0 to A17	DATA I/O	MODE
L	H	L	H	Stable	Output Data	Read
L	H	X	L	Stable	Input Data	Write
L	H	H	H	Stable	Hi-Z	Output Disable
H	X	X	X	-	Hi-Z	Standby
X	L	X	X	-	Hi-Z	

*Note: X means don't care(Must be high or low states)

Capacitance (f = 1MHz, T_A = 25 °C)

Symbol	Parameter	Test Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	V_I = 0V	-	8	pF
$C_{I/O}$	Output Capacitance	V_O = 0V	-	10	pF

*Note: This parameter is sampled and not 100% tested.

AC Operating Characteristics

Test Conditions (Commercial Product :Ta = 0 ~ 70 °C, Industrial Product : Ta = -40 ~ 85 °C)

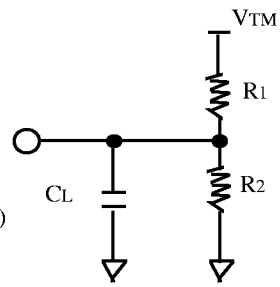
Parameter	Value
Input Pulse Level	0.4 to 2.2V for Vcc=3.3V,3.0V,2.5V 0.4 to 1.8V for Vcc=2.0V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	1.5V for Vcc=3.3V,3.0V 1.1V for Vcc=2.5V 0.9V for Vcc=2.0V
Output Load	C_L = 100pF + 1TTL Load or 30 pF + 1TTL Load

DC Operating Characteristics

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
$I_{I(L)}$	Input Leakage Current	V_{IN} =Vss to V_{CC}			-1	-	1	uA
$I_{O(L)}$	Output Leakage Current	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} $\overline{OE}$ = V_{IH}, V_{SS}<V_{OUT}< V_{CC}			-1	-	1	uA
V_{OH}	High Level Output Voltage	I_{OH}	-1.0mA at Vcc=3.3V -1.0mA at Vcc=3.0V -0.5mA at Vcc=2.5V -0.44mA at Vcc=2.0V		2.4 2.2 2.0 1.6	-	-	V
V_{OL}	Low Level Output Voltage	I_{OL}	2.1mA at Vcc=3.0/3.3V 0.5mA at Vcc=2.5V 0.33mA at Vcc=2.0V		-	-	0.4	V
I_{CC}	Operating Supply Current	$\overline{CS1}$ = V_{IL} and CS2 = V_{IH}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA			-	-	10	mA
I_{CC1}	Average Operating Current	$\overline{CS1}$ = V_{IL} and CS2 = V_{IH} V_{IN} = V_{IH} or V_{IL} , I_{OUT} = 0mA tcycle = Min, cycle	Vcc=3.3V@55ns		-	-	45	mA
			Vcc=3.0V@55ns		-	-	35	
			Vcc=2.5V@70ns		-	-	25	
			Vcc=2.0V@100ns		-	-	20	
I_{CC2}		$\overline{CS1}$ = 0.2V, CS2 = V_{CC}-0.2V V_{IN} = V_{CC} - 0.2V or 0.2V I_{OUT} = 0mA, tcycle = 1μs			-	-	10	mA
I_{CCS1}	Standby Current(TTL)	$\overline{CS1}$ = V_{IH}, CS2 = V_{IL}			-	-	0.3	mA
I_{CCS2}	Standby Current(CMOS)	$\overline{CS1}$ = V_{CC}-0.2V,CS2 = 0.2V		SL	-	-	2	uA
				LL	-	-	10	

AC Test Load Conditions.

1. Including scope and jig capacitance
2. R1=3070 Ω , R2=3150 Ω
3. V_{TM}=2.8V for Vcc=3.0V/3.3V
   V_{TM}=2.3V for Vcc=2.5V
   V_{TM}=1.8V for Vcc=2.0V
4. CL= 100pF + 1TTL (70ns @3.3/3.0V, 85ns @2.5V,120ns @2.0V)
   30pF + 1TTL (55ns @3.3/3.0V, 70ns @2.5V, 100ns @2.0V)
   5pF + 1TTL (For tCLZ1,tCLZ2,tOLZ,tCHZ1
   tCHZ2,tOHZ,tWHZ,tOW)



AC Operating Characteristics

Read Cycle

(Commercial Product :Ta = 0 ~ 70 °C, Industrial Product : Ta = -40 ~ 85 °C)

Symbol	Parameter	55ns		70ns		85ns		Unit
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	55	-	70	-	85	-	ns
t_{AA}	Address Access Time	-	55	-	70	-	85	ns
t_{ACS1}	Chip Select 1 Access Time	-	55	-	70	-	85	ns
t_{ACS2}	Chip Select 2 Access Time	-	55	-	70	-	85	ns
t_{OE}	Output Enable Access Time	-	30	-	35	-	45	ns
t_{CLZ1}	Chip Select 1 Output Setup Time	5	-	5	-	10	-	ns
t_{CHZ1}	Chip Select 1 Output Floating	0	20	0	25	0	30	ns
t_{CLZ2}	Chip Select 2 Output Setup Time	5	-	5	-	10	-	ns
t_{CHZ2}	Chip Select 2 Output Floating	0	20	0	25	0	30	ns
t_{OLZ}	Output Enable Output Setup Time	5	-	5	-	5	-	ns
t_{OHZ}	Output Enable Output Floating	0	20	0	25	0	30	ns
t_{OH}	Output Hold Time	5	-	10	-	10	-	ns

Write Cycle

Symbol	Parameter	55ns		70ns		85ns		Unit
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	55	-	70	-	85	-	ns
t_{CW1}	Chip Select Time 1	50	-	65	-	75	-	ns
t_{CW2}	Chip Select Time 2	50	-	65	-	75	-	ns
t_{AW}	Address Enable Time	50	-	60	-	70	-	ns
t_{AS}	Address Setup Time	0	-	0	-	0	-	ns
t_{WP}	Write Pulse Width	45	-	50	-	60	-	ns
t_{WR}	Write Recovery Time	0	-	0	-	0	-	ns
t_{DW}	Input Data Setup Time	25	-	30	-	35	-	ns
t_{DH}	Input Data Hold Time	0	-	0	-	0	-	ns
t_{WHZ}	Write to Output in High-Z	0	20	0	25	0	30	ns
t_{OW}	Output Active from End of Write	5	-	5	-	5	-	ns

AC Operating Characteristics

Read Cycle

(Commercial Product :Ta = 0 ~ 70 °C, Industrial Product : Ta = -40 ~ 85 °C)

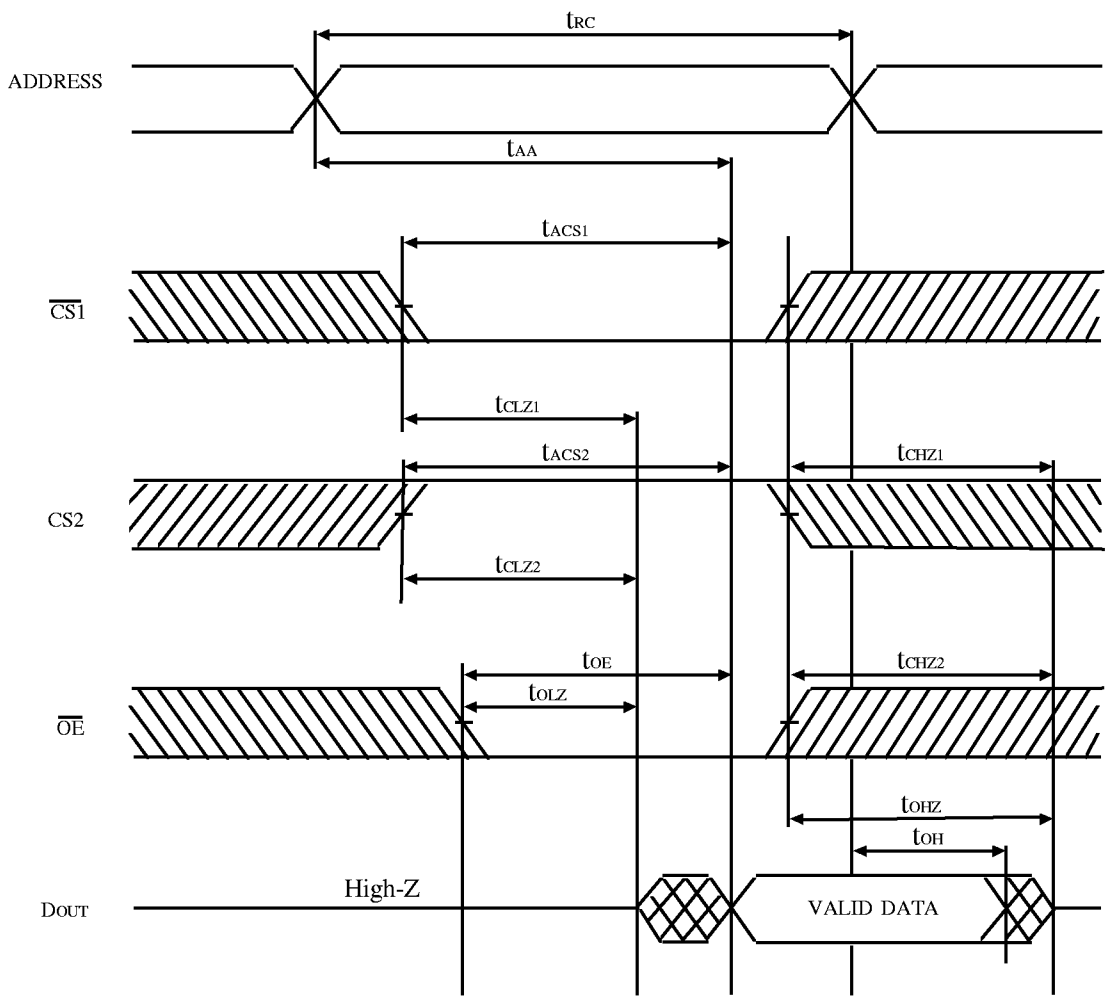
Symbol	Parameter	100ns		120ns		Unit
		Min	Max	Min	Max	
t_{RC}	Read Cycle Time	100	-	120	-	ns
t_{AA}	Address Access Time	-	100	-	120	ns
t_{ACS1}	Chip Select 1 Access Time	-	100	-	120	ns
t_{ACS2}	Chip Select 2 Access Time	-	100	-	120	ns
t_{OE}	Output Enable Access Time	-	50	-	60	ns
t_{CLZ1}	Chip Select 1 Output Setup Time	10	-	10	-	ns
t_{CHZ1}	Chip Select 1 Output Floating	0	35	0	35	ns
t_{CLZ2}	Chip Select 2 Output Setup Time	10	-	10	-	ns
t_{CHZ2}	Chip Select 2 Output Floating	0	35	0	35	ns
t_{OLZ}	Output Enable Output Setup Time	5	-	5	-	ns
t_{OHZ}	Output Enable Output Floating	0	35	0	35	ns
t_{OH}	Output Hold Time	15	-	15	-	ns

Write Cycle

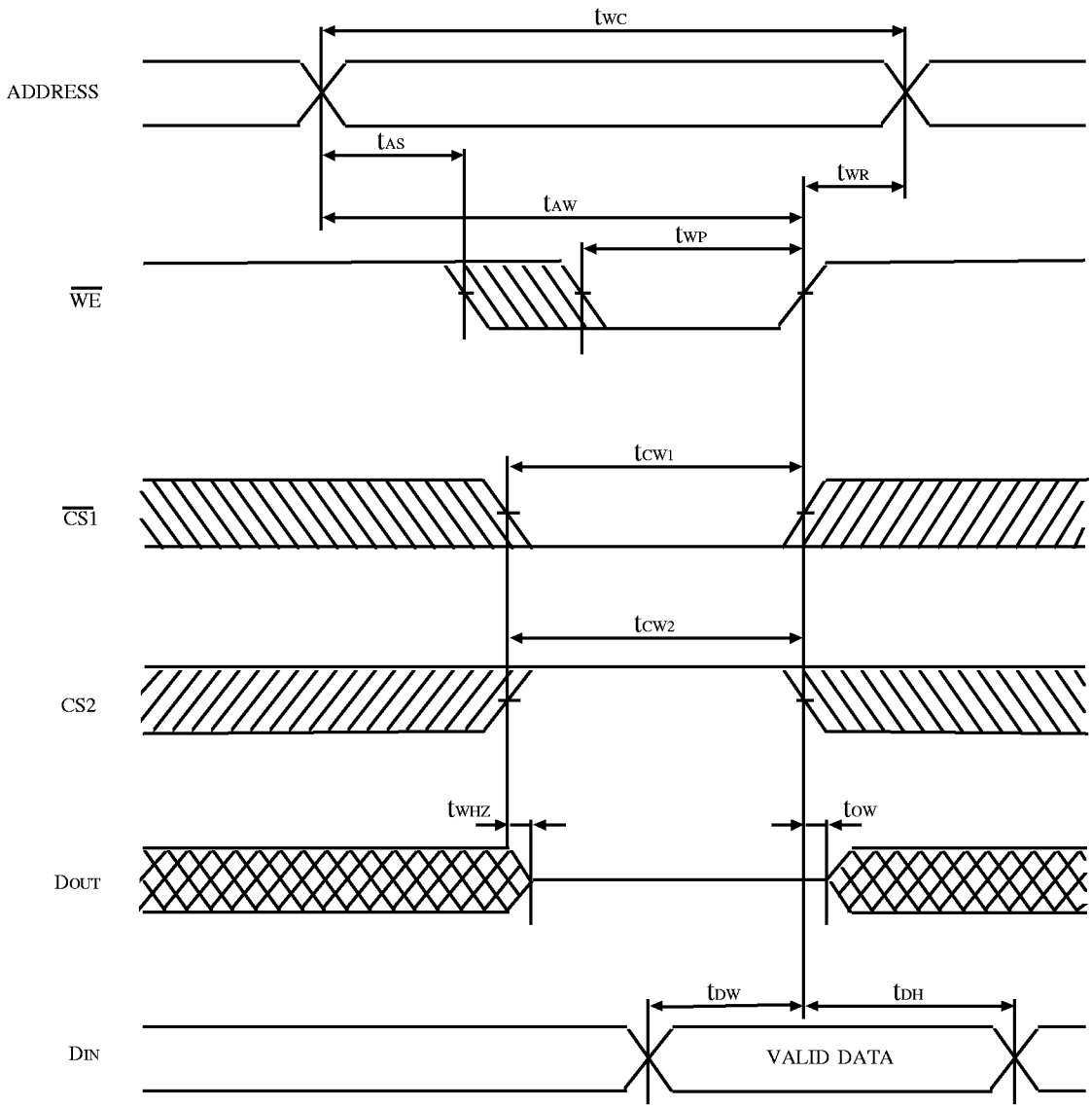
Symbol	Parameter	100ns		120ns		Unit
		Min	Max	Min	Max	
t_{WC}	Write Cycle Time	100	-	120	-	ns
t_{CW1}	Chip Select Time 1	80	-	100	-	ns
t_{CW2}	Chip Select Time 2	80	-	100	-	ns
t_{AW}	Address Enable Time	80	-	100	-	ns
t_{AS}	Address Setup Time	0	-	0	-	ns
t_{WP}	Write Pulse Width	70	-	80	-	ns
t_{WR}	Write Recovery Time	0	-	0	-	ns
t_{DW}	Input Data Setup Time	40	-	50	-	ns
t_{DH}	Input Data Hold Time	0	-	0	-	ns
t_{WHZ}	Write to Output in High-Z	0	30	0	35	ns
t_{OW}	Output Active from End of Write	10	-	10	-	ns

Timing Waveforms

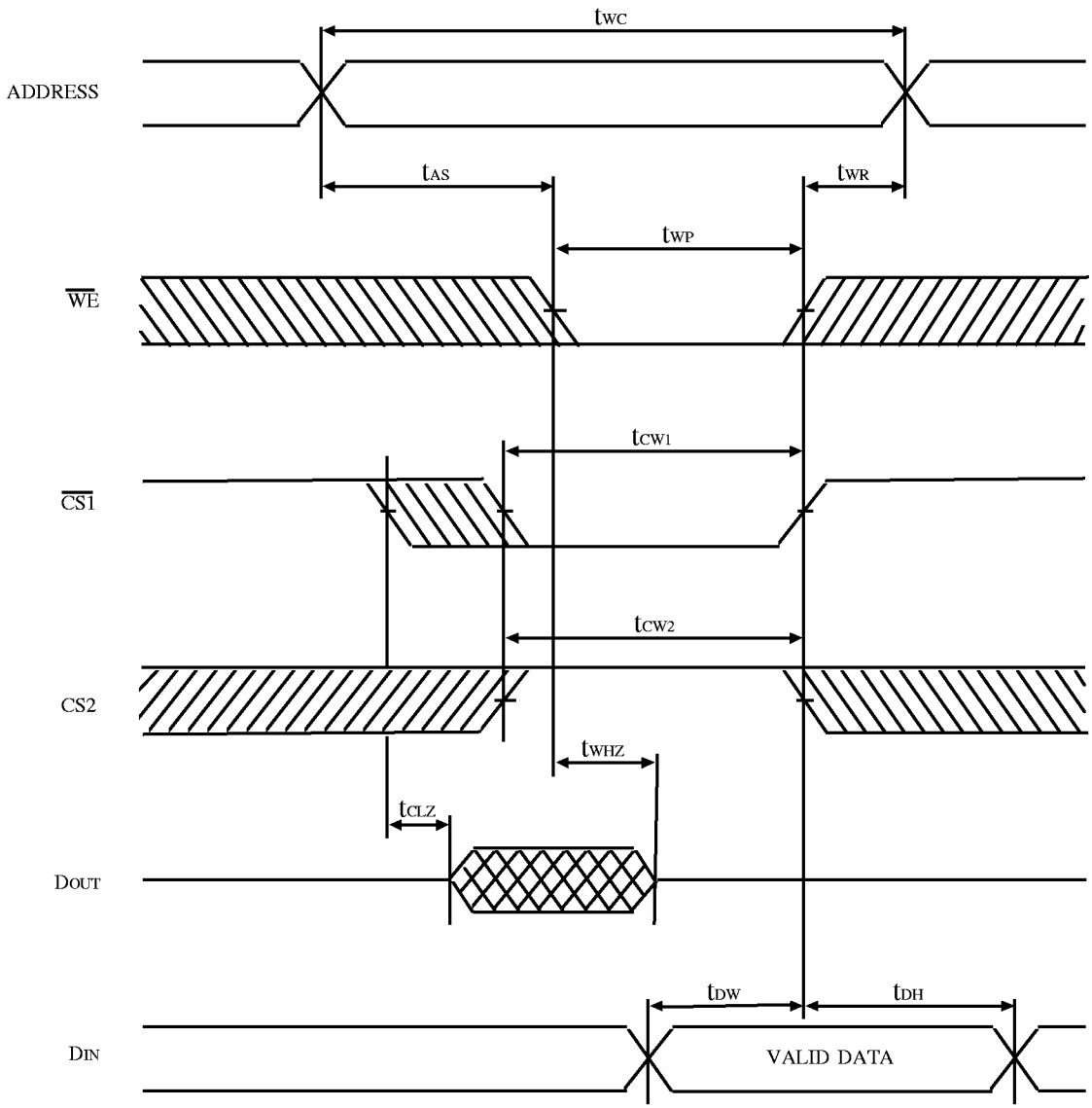
Read Cycle (Note 1)



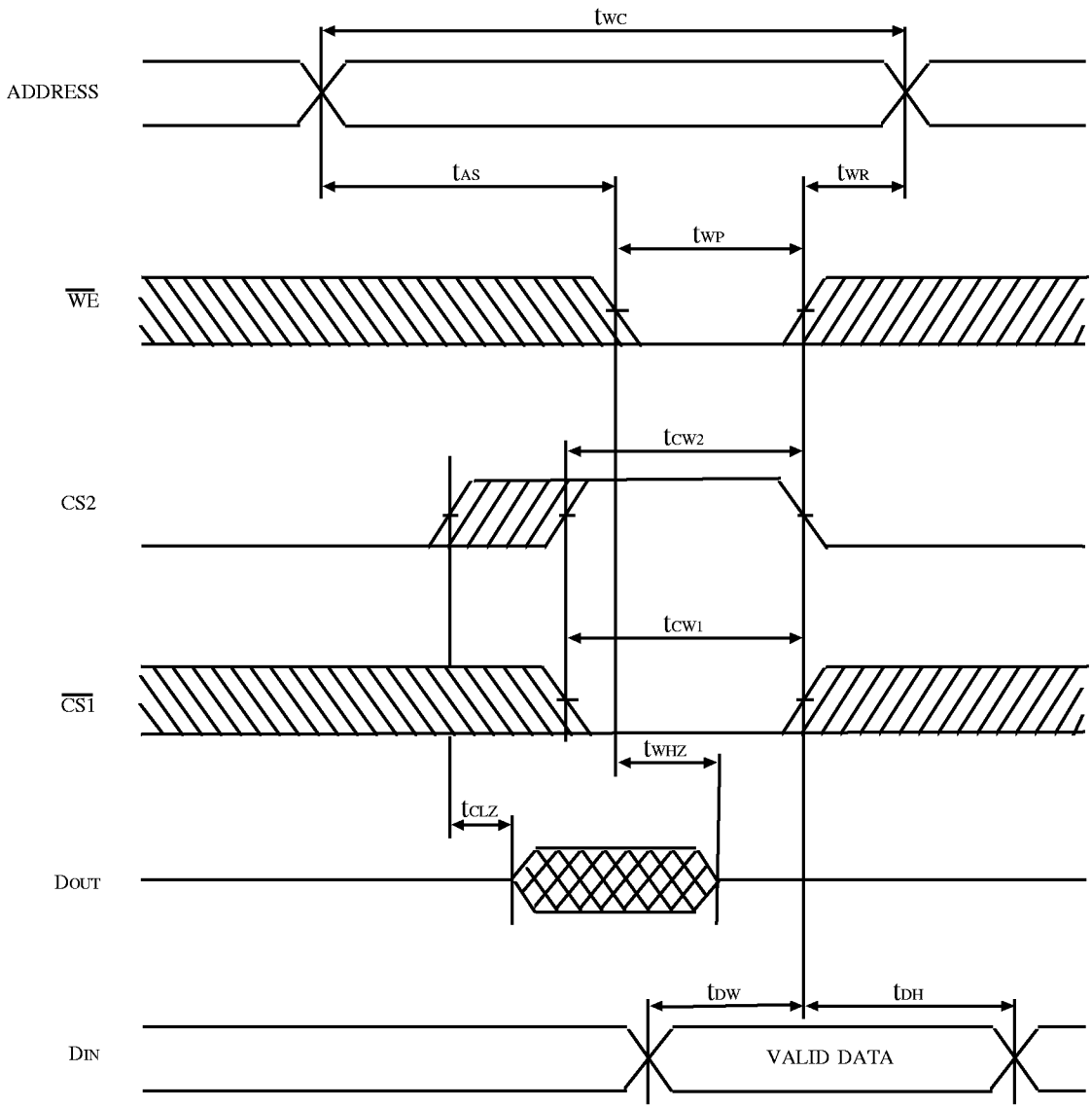
Write Cycle (1) ($\overline{WE}$ Controlled) (Notes 2, 3, 4)



Write Cycle (2) ($\overline{CS1}$ Controlled) (Notes 4)



Write Cycle (3) (CS2 Controlled) (Notes 4)



Notes:
1. $\overline{WE}$ is High for Read Cycle.
2. Assuming that $\overline{CS1}$ Low transition or CS2 High transition occurs coincident with or after $\overline{WE}$ Low transition. Outputs remain in a high impedance state.
3. Assuming that $\overline{CS1}$ High transition or CS2 Low transition occurs coincident with or prior to $\overline{WE}$ High transition. Outputs remain in a high impedance state.
4. Assuming that $\overline{OE}$ is high for write cycle. Outputs are in a high impedance state during this period.

Data Retention Characteristics

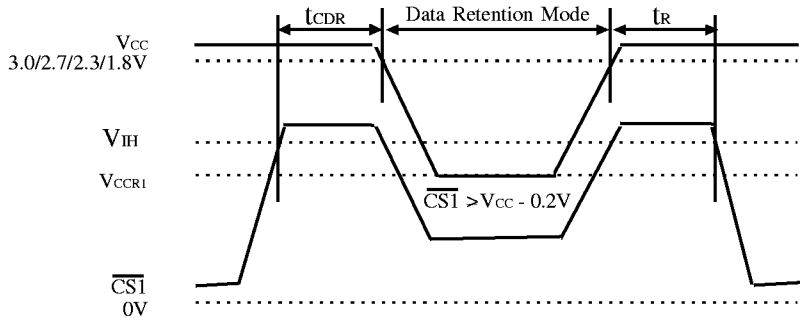
Symbol	Item	Test Condition		Min	Typ	Max	Unit
V_{CCR}	Data Retention Supply Voltage	$\overline{CS1}$ ≥Vcc -0.2V[1]		1.5	-	3.6	V
I_{CCR}	Data Retention Current	Vcc=2.0V, $\overline{CS1}$ ≥ Vcc-0.2V[1]	LL SL	- -	- -	10 2	uA
t_{CDR}	Chip Select to Data Retentiom Time	See data retention waveform		0	-	-	ns
t_R	Operation Recovery Time			t_{RC}[2]	-	-	ns

1) $\overline{CS1}$ ¡Ý Vcc - 0.2V, CS2 ¡Ý Vcc - 0.2V ($\overline{CS1}$ controlled) or CS2 ¡Ü 0.2V (CS2 Controlled)

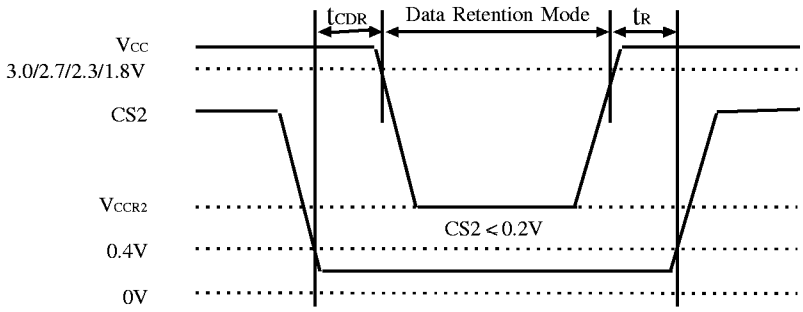
2) t_{RC} = Read cycle time

• Data Retention Waveform

(1) $\overline{CS1}$ Controlled



(2) CS2 Controlled

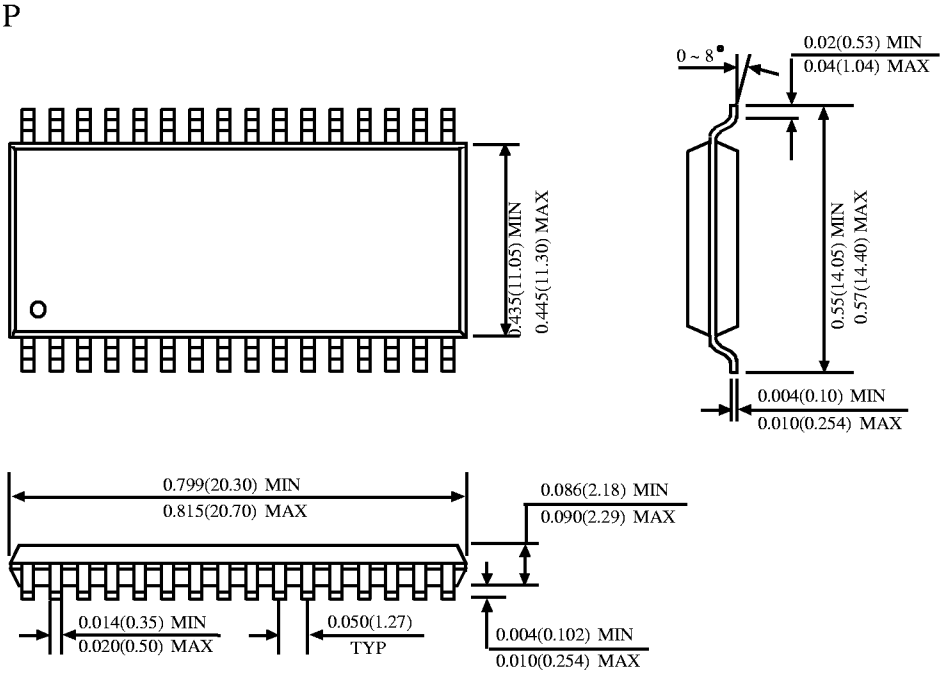


Notes: In Data Retention Mode, CS2 controls the Address, $\overline{WE}$, $\overline{CS1}$, $\overline{OE}$ and D_{IN} buffer. If CS2 controls data retention mode, V_{IN} for these inputs can be in the high impedance state. If $\overline{CS1}$ controls the data retention mode, CS2 must satisfy either CS2>V_{CC} - 0.2V or CS2<0.2V. The other input levels (Address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

Package Dimensions

Unit: Inches (mm)

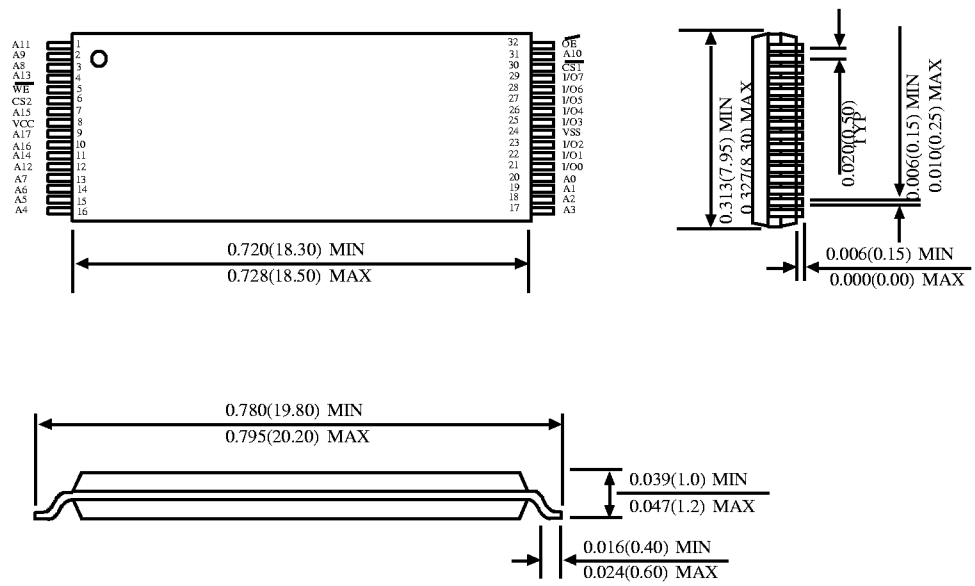
32 SOP



Package Dimensions

Unit: Inches (mm)

32 TSOP I (8 x 20 mm)



32 Small TSOP I (8 x 13.4 mm)