LINEAR SYSTEMS

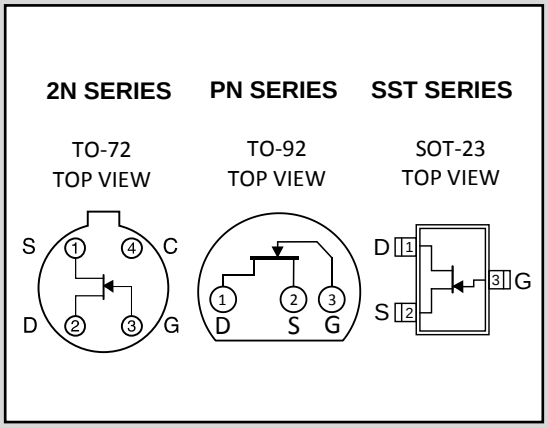
Over Three Decades of Quality Through Innovation

2N/PN/SST 4117, 4118, 4119

ULTRA-HIGH INPUT IMPEDANCE N-CHANNEL JFET AMPLIFIER

FEATURES	
LOW POWER	I_{DSS}<600 µA (2N4117A)
MINIMUM CIRCUIT LOADING	I_{GSS}<1 pA (2N4117A Series)

ABSOLUTE MAXIMUM RATINGS (NOTE 3) @ 25°C (unless otherwise noted)	
Gate-Source or Gate-Drain Voltage	-40V
Gate-Current	50mA
Total Device Dissipation (Derate 2mW/ºC above 25ºC)	300mW
Storage Temperature Range	-55ºC to+150ºC
Lead Temperature (1/16" from case for 10 seconds)	300ºC



ELECTRICAL CHARACTERISTICS @ 25ºC (unless otherwise noted)

SYMBOL	CHARACTERISTIC	4117 MIN	4117 MAX	4118 MIN	4118 MAX	4119 MIN	4119 MAX	UNITS	CONDITIONS	
BV_{GSS}	Gate-Source Breakdown Voltage	-40	--	-40	--	-40	--	V	I_G =-1µA V_{DS}=0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.6	-1.8	-1	-3	-2	-6	V	V_{DS} =10V I_D=1nA	
I_{DSS}	Saturation Drain Current (NOTE 2)	0.03	0.60	0.08	0.60	0.20	0.80	mA	V_{DS} =10V V_{GS}=0	
I_{GSS}	Gate Reverse Current 2N4117A, 2N4118A, 2N4119A	--	-1	--	-1	--	-1	pA	V_{GS} =-20V V_{DS}=0	
		--	-2.5	--	-2.5	--	-2.5	nA		150ºC
	PN4117, PN4118, PN4119 SST4117, SST4118, SST4119	--	-10	--	-10	--	-10	pA	V_{GS} =-10V V_{DS}=0	
		--	-25	--	-25	--	-25	nA		150ºC
g_{fs}	Common-Source Forward Transconductance	70	450	80	650	100	700	µS	V_{DS} =10V V_{GS}=0	f=1kHz
g_{os}	Common-Source Output Conductance	--	3	--	5	--	10	µS		f=1kHz
C_{iss}	Common-Source Input Capacitance (NOTE 4)	--	3	--	3	--	3	pF		f=1MHz
C_{rss}	Common-Source Reverse Transfer Capacitance (NOTE 4)	--	1.5	--	1.5	--	1.5	pF		f=1MHz

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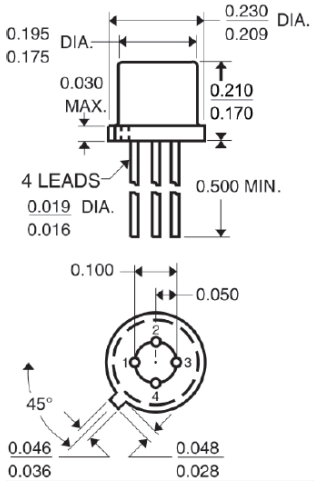
Doc 201135 11/09/17 Rev#A10 ECN# 2N & SST 4117 4118 4119

STANDARD PACKAGE DIMENSIONS:

2N4117A, 2N4118A, 2N4119A

TO-72

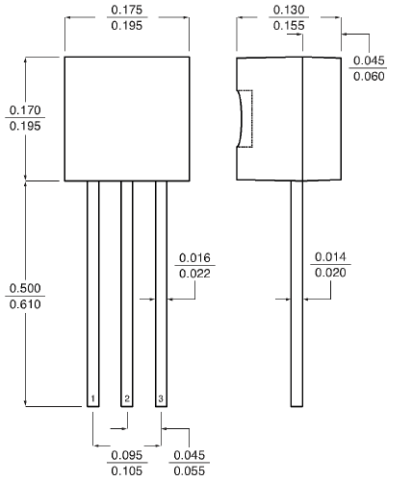
Four Lead



*Dimensions in inches

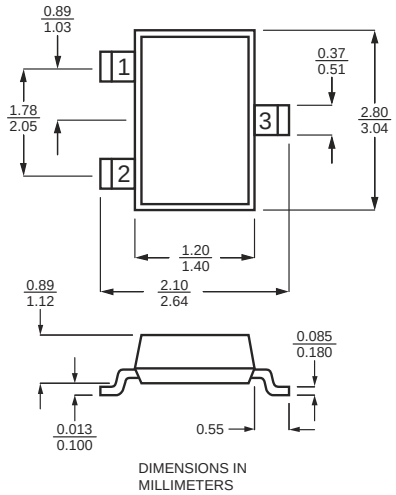
PN4117, PN4118, PN4119

TO-92



SST4117, SST4118, SST4119

SOT-23



NOTES:

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. This parameter is measured during a 2 ms interval 100 ms after power is applied. (Not a JEDEC condition.)
3. Absolute maximum ratings are limiting values above which serviceability may be impaired.
4. Not production tested, guaranteed by design.

Linear Integrated Systems (LIS), established in 1987, is a third-generation precision semiconductor company providing high-quality discrete components. Expertise brought to LIS is based on processes and products developed at Amelco, Union Carbide, Intersil and Micro Power Systems by company Founder John H. Hall. Hall, a protégé of Silicon Valley legend Dr. Jean Hoerni, was the director of IC Development at Union Carbide, Co-Founder and Vice President of R&D at Intersil, and Founder/President of Micro Power Systems.

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