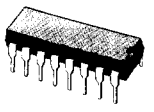
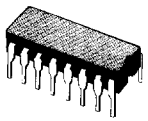
HC192 - SYNCHRONOUS UP/DOWN DECADE COUNTER
HC193 - SYNCHRONOUS UP/DOWN BINARY COUNTER

- HIGH SPEED
  f_{MAX} = 54 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS192-193



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

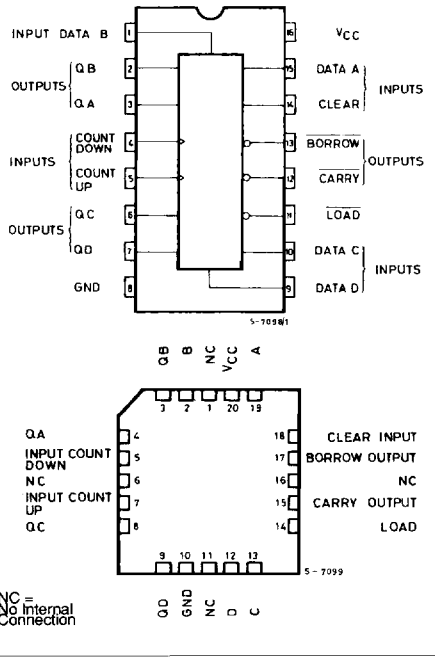
ORDER CODES :

M54HCXXXF1R M74HCXXXM1R
M74HCXXXB1R M74HCXXXC1R

DESCRIPTION

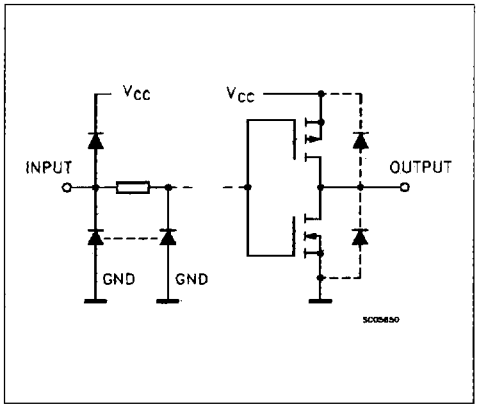
The M54/74HC192/193 are a high speed CMOS SYNCHRONOUS UP/DOWN DECADE COUNTERS fabricated in silicon gate C^2MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption. The counter has two separate clock inputs, an UP COUNT input and a DOWN COUNT input. All outputs of the flip-flop are simultaneously triggered on the low to high transition of either clock while the other input is held high. The direction of counting is determined by which input is clocked. This counter may be preset by entering the desired data on the DATA A, DATA B, DATA C, and DATA D input. When the LOAD input is taken low the data is loaded independently of either clock input. This feature allows the counters to be used as divide-by-n counters by modifying the count length with the preset inputs. In addition the counter can also be cleared. This is accomplished by inputting a high on the CLEAR input. All 4 internal stages are set to low independently of either COUNT input. Both a BORROW and CARRY output are provided to enable cascading of both up and down counting functions. The BORROW output produces a negative going pulse when the counter underflows and the CARRY outputs a pulse when the counter overflows. The counter can be cascaded by connecting the CARRY and BORROW outputs of one device to the COUNT UP and COUNT DOWN inputs, respectively, of the next device. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)



NC = No Internal Connection

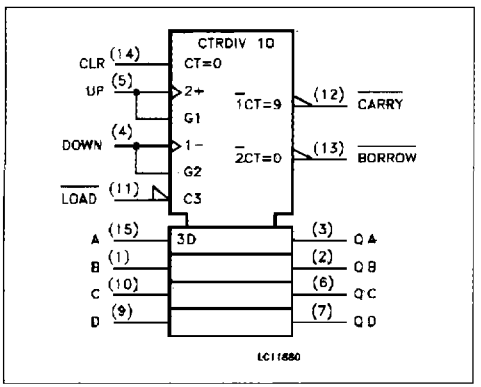
INPUT AND OUTPUT EQUIVALENT CIRCUIT



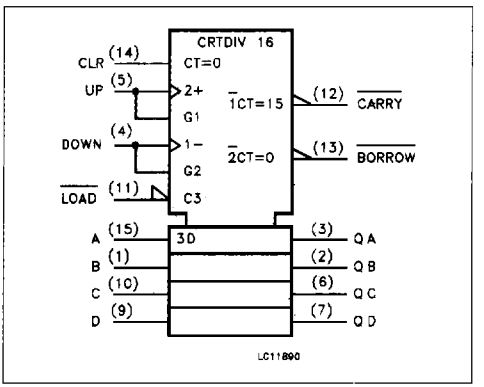
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
3, 2, 6, 7	QA to QD	Flip-Flop Outputs
4	CP_D	Count Down Clock Input
5	CP_U	Count Up Clock Input
11	$\overline{LOAD}$	Asynchronous Parallel Load Input (Active LOW)
12	$\overline{CARRY}$	Count Up (Carry) Output (Active LOW)
13	$\overline{BORROW}$	Count Down (Borrow) Output (Active LOW)
14	CLEAR	Asynchronous Reset Input (Active HIGH)
15, 1, 10, 9	DA to DD	Data Inputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL (HC191)



IEC LOGIC SYMBOL (HC193)

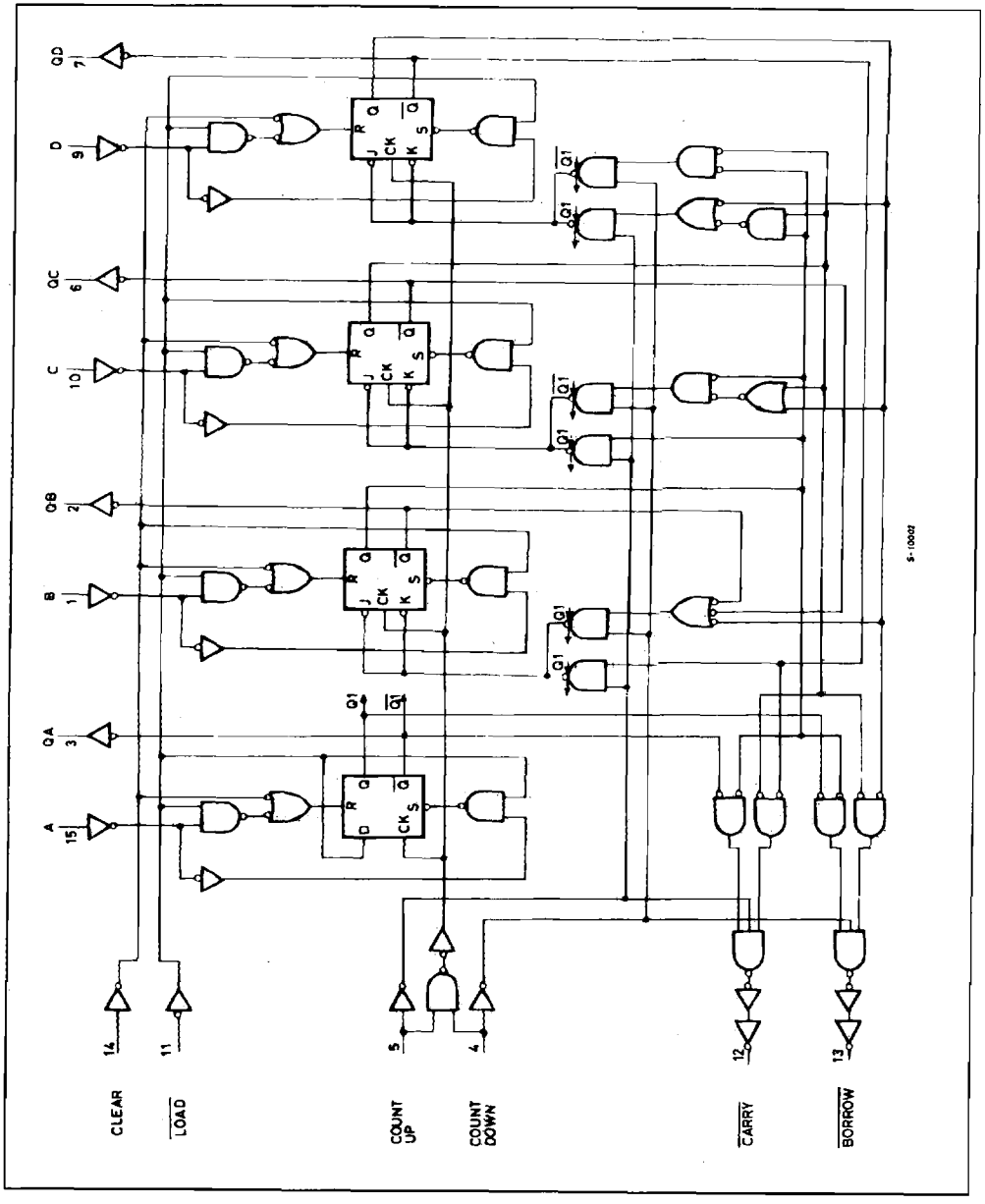


TRUTH TABLE

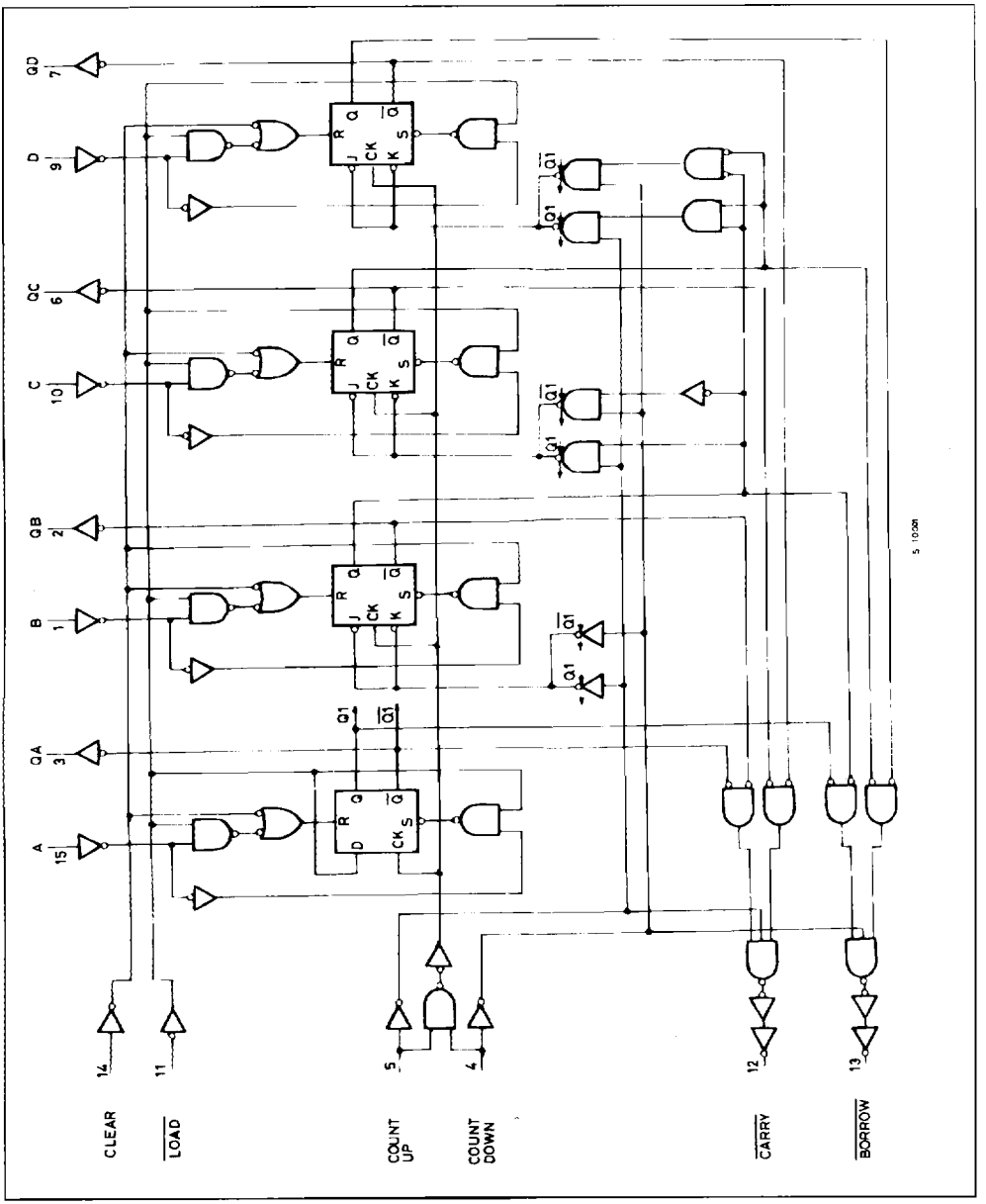
COUNT UP	COUNT DOWN	$\overline{LOAD}$	CLEAR	FUNCTION
⌐	H	H	L	COUNT UP
¬	H	H	L	NO COUNT
H	⌐	H	L	COUNT DOWN
H	¬	H	L	NO COUNT
X	X	L	L	PRESET
X	X	X	H	RESET

X: Don't Care

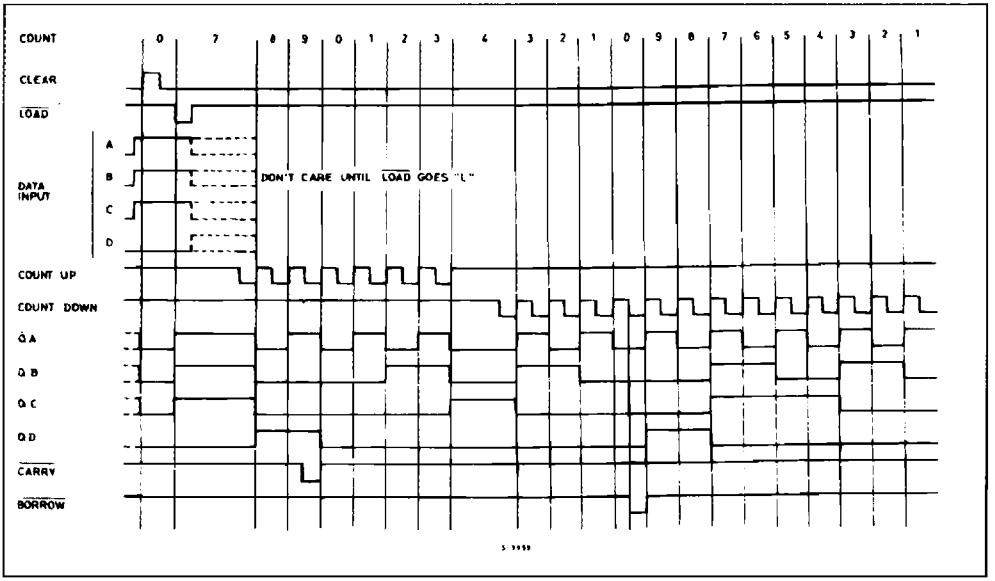
LOGIC DIAGAM (HC192)



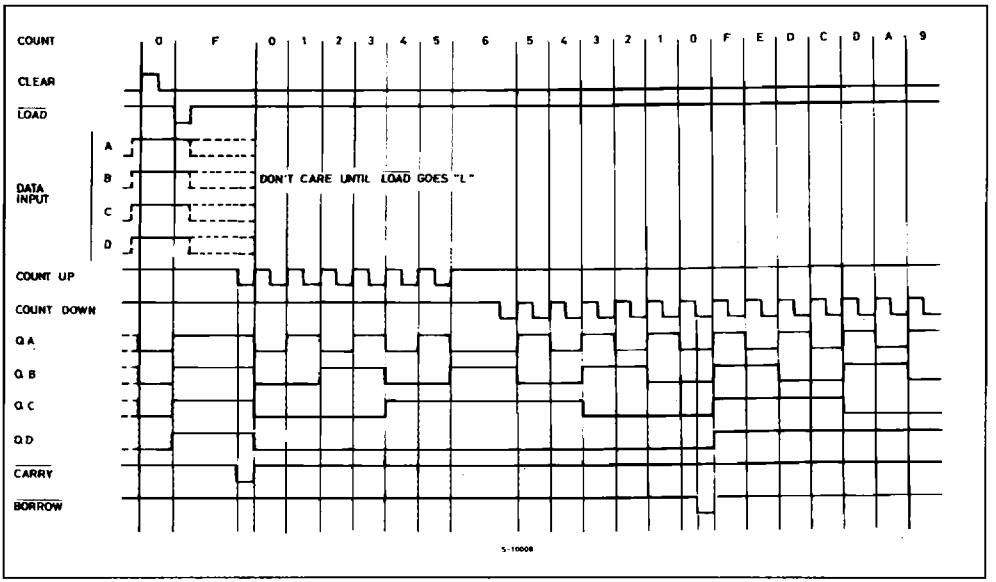
LOGIC DIAGAM (HC193)



TIMING DIAGRAM (HC192)



TIMING DIAGRAM (HC193)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

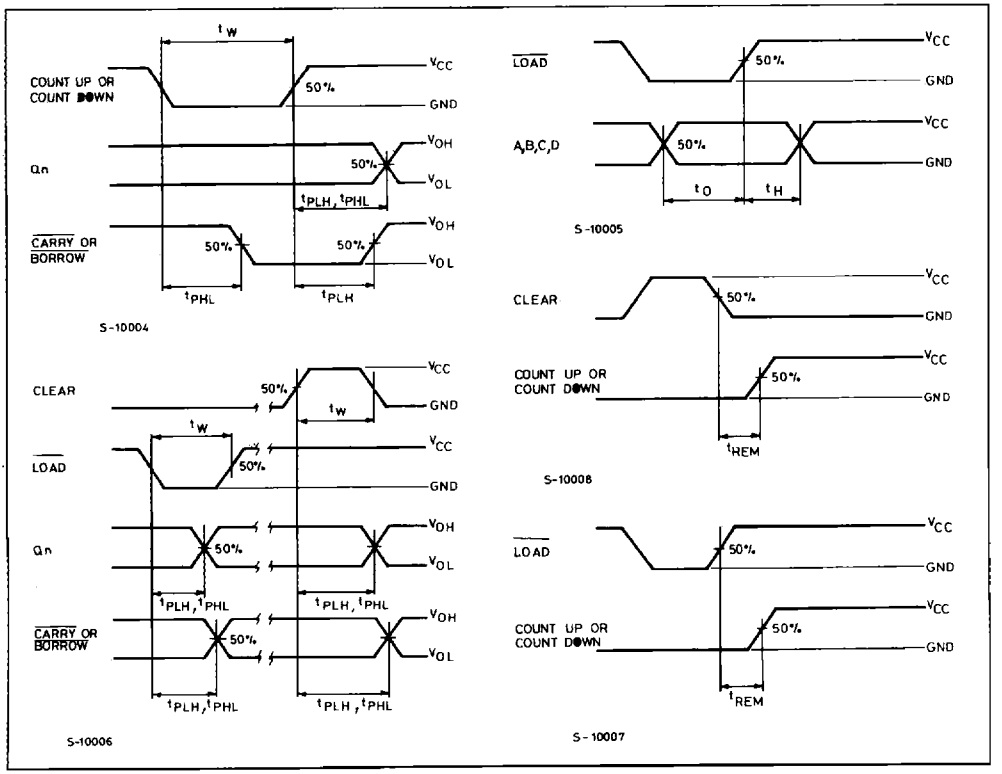
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (UP, DOWN - Q)	2.0			65	190		240		285	ns
		4.5			20	38		48		57	
		6.0			16	32		41		48	
t_{PLH} t_{PHL}	Propagation Delay Time (UP - $\overline{CARRY}$)	2.0			40	130		165		195	ns
		4.5			13	26		33		39	
		6.0			11	22		28		33	
t_{PLH} t_{PHL}	Propagation Delay Time (DOWN - BORROW)	2.0			40	130		165		195	ns
		4.5			13	26		33		39	
		6.0			11	22		28		33	
t_{PLH} t_{PHL}	Propagation Delay Time (LOAD - Q)	2.0			85	220		275		330	ns
		4.5			25	44		55		66	
		6.0			20	37		47		56	
t_{PLH} t_{PHL}	Propagation Delay Time (LOAD - $\overline{CARRY}$)	2.0			110	250		315		375	ns
		4.5			30	50		63		75	
		6.0			25	43		54		64	
t_{PLH} t_{PHL}	Propagation Delay Time (LOAD - BORROW)	2.0			110	250		315		375	ns
		4.5			31	50		63		75	
		6.0			25	43		54		64	
t_{PLH} t_{PHL}	Propagation Delay Time (DATA - Q)	2.0			80	190		240		285	ns
		4.5			25	38		48		57	
		6.0			20	32		41		48	
t_{PLH} t_{PHL}	Propagation Delay Time (DATA - $\overline{CARRY}$)	2.0			120	250		315		375	ns
		4.5			34	50		63		75	
		6.0			28	43		54		64	
t_{PLH} t_{PHL}	Propagation Delay Time (DATA - $\overline{BORROW}$)	2.0			110	250		315		375	ns
		4.5			30	50		63		75	
		6.0			25	43		54		64	
t_{PHL}	Propagation Delay Time (CLEAR - Q)	2.0			100	225		280		340	ns
		4.5			30	45		56		68	
		6.0			25	38		48		58	
t_{PLH}	Propagation Delay Time (CLEAR - $\overline{CARRY}$)	2.0			120	250		315		375	ns
		4.5			35	50		63		75	
		6.0			29	43		54		64	
t_{PHL}	Propagation Delay Time (CLEAR - $\overline{BORROW}$)	2.0			120	250		315		375	ns
		4.5			35	50		63		75	
		6.0			29	43		54		64	
f_{MAX}	Maximum Clock Frequency	2.0		5	12		4		3.4		MHz
		4.5		25	48		20		17		
		6.0		30	55		24		20		

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

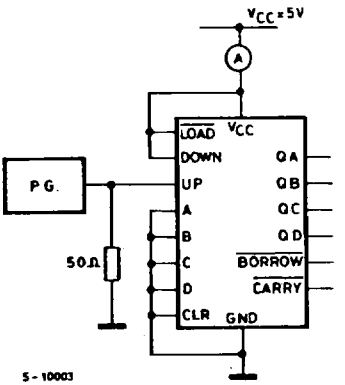
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (COUNT UP/DOWN)	2.0			34	100		125		150	ns
		4.5			9	20		25		30	
		6.0			7	17		21		26	
$t_{W(L)}$	Minimum Pulse Width ($\overline{LOAD}$)	2.0			34	75		95		110	ns
		4.5			9	15		19		22	
		6.0			7	13		16		19	
$t_{W(H)}$	Minimum Pulse Width (CLEAR)	2.0			40	100		125		150	ns
		4.5			12	20		25		30	
		6.0			10	17		21		26	
t_s	Minimum Set-up Time (DATA - $\overline{LOAD}$)	2.0			30	75		95		110	ns
		4.5			9	15		19		22	
		6.0			7	13		16		19	
t_h	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t_{REM}	Minimum Removal Time ($\overline{LOAD}$)	2.0			6	50		65		75	ns
		4.5			2	10		13		15	
		6.0			2	9		11		13	
t_{REM}	Minimum Removal Time (CLEAR)	2.0			14	50		65		75	ns
		4.5			4	10		13		15	
		6.0			3	9		11		13	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance		for HC192		68						pF
			for HC193		67						

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT Icc (Opr.)



TRANSITION TIME OF INPUT WAVEFORMS IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.