National Semiconductor

74VHC153
Dual 4-Input Multiplexer

General Description

The VHC153 is an advanced high-speed CMOS device fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The VHC153 is a high-speed dual 4-input multiplexer with common select inputs and individual enable inputs for each section. It can select two lines of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the VHC153 can act as a function generator and generate any two functions of three variables. An input protection circuit insures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back-up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

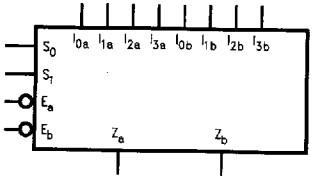
- Low power dissipation:
  I_{CC} = 4 μA (max) at T_A = 25°C
- High noise immunity: V_{NIH} = V_{NIL} = 28% V_{CC} (min)
- All inputs are equipped with a power down protection function
- Balanced propagation delays: $t_{PLH} \cong t_{PHL}$
- Pin and function compatible with 74HC153

Ordering Code: See Section 6

Commercial	Package Number	Package Description
74VHC153M	M16A	16-Lead Molded JEDEC SOIC
74VHC153SJ	M16D	16-Lead Molded EIAJ SOIC
74VHC153MTC	MTC16	16-Lead Molded JEDEC Type 1 TSSOP
74VHC153N	N16E	16-Lead Molded DIP

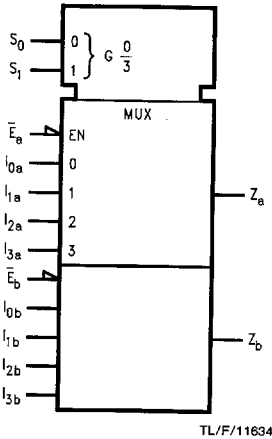
Note: Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



TL/F/11634–1

IEEE/IEC

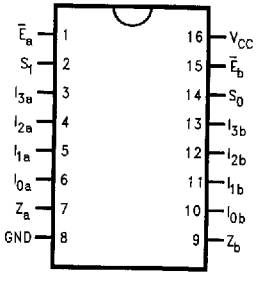


TL/F/11634–2

Pin Names	Description
I_{0a}–I_{3a}	Side A Data Inputs
I_{0b}–I_{3b}	Side B Data Inputs
S_0, S_1	Common Select Inputs
$\overline{E}_a$	Side A Enable Input
$\overline{E}_b$	Side B Enable Input
Z_a	Side A Output
Z_b	Side B Output

Connection Diagram

Pin Assignment for DIP, TSSOP and SOIC



TL/F/11634–3

Functional Description

The VHC153 is a dual 4-input multiplexer. It can select two bits of data from up to four sources under the control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active-LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs indepedently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs (Z_a, Z_b) are forced LOW. The VHC153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the Select inputs. The logic equations for the outputs are shown below.

$$Z_a = \overline{E}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet S_0 + I_{3a} \bullet S_1 \bullet S_0)$$

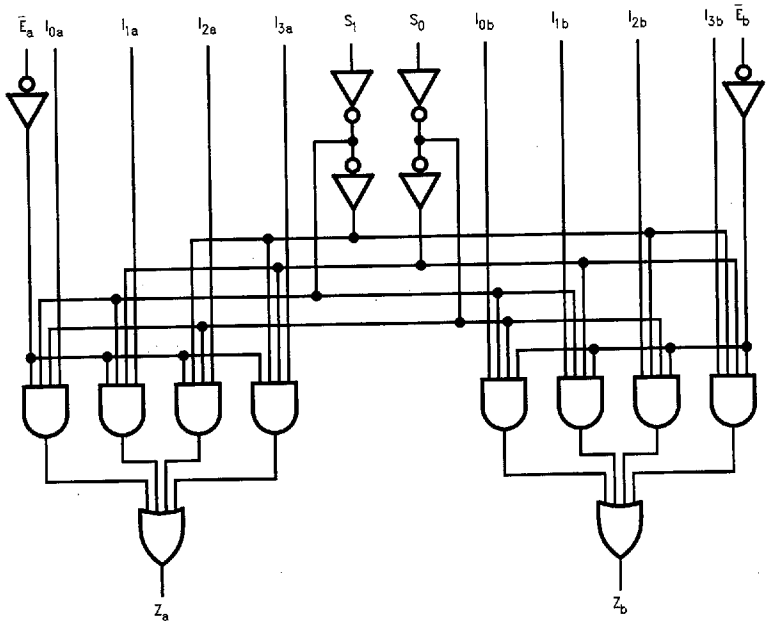
$$Z_b = \overline{E}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet S_0 + I_{3b} \bullet S_1 \bullet S_0)$$

Truth Table

Select Inputs		Inputs (a or b)					Output
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	Z
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



TL/F/11634–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to + 7.0V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Input Diode Current (I_{IK})	−20 mA
Output Diode Current (I_{OK})	±20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Note 1: *Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation outside databook specifications.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 5.5V
Input Voltage (V_{IN})	0V to +5.5
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 3.3V ±0.3V	0~100 ns/V
V_{CC} = 5.0V ±0.5V	0~20 ns/V

DC Characteristics for 'VHC Family Devices

Symbol	Parameter	V_{CC} (V)	74VHC					Units	Conditions	
			T_A = 25°C			T_A = −40°C to +85°C				
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0 3.0–5.5	1.50 0.7 V_{CC}			1.50 0.7 V_{CC}		V		
V_{IL}	Low Level Input Voltage	2.0 3.0–5.5			0.50 0.3 V_{CC}		0.50 0.3 V_{CC}	V		
V_{OH}	High Level Output Voltage	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA
		3.0 4.5	2.58 3.94			2.48 3.80		V		I_{OH} = −4 mA I_{OH} = −8 mA
V_{OL}	Low Level Output Voltage	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA
		3.0 4.5			0.36 0.36		0.44 0.44	V		I_{OL} = 4 mA I_{OL} = 8 mA
I_{IN}	Input Leakage Current	0–5.5			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	5.5			4.0		40.0	μA	V_{IN} = V_{CC} or GND	

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC} (V)	74VHC $T_A = 25°C$			74VHC $T_A = -40°C$ to $+85°C$		Units	Conditions	Fig. No.
			Min	Typ	Max	Min	Max			
t_{PLH}, t_{PHL}	Propagation Delay I_n to Z_n	3.3 ±0.3		7.7	11.9	1.0	14.0	ns	C_L = 15 pF	2-5
				10.2	15.4	1.0	17.5		C_L = 50 pF	2-5
		5.0 ±0.5		5.0	7.7	1.0	9.0	ns	C_L = 15 pF	2-5
				6.5	9.7	1.0	11.0		C_L = 50 pF	2-5
t_{PLH}, t_{PHL}	Propagation Delay S_n to Z_n	3.3 ±0.3		10.8	16.7	1.0	19.5	ns	C_L = 15 pF	2-6
				13.3	20.2	1.0	23.0		C_L = 50 pF	2-6
		5.0 ±0.5		6.8	9.9	1.0	11.5	ns	C_L = 15 pF	2-6
				8.3	11.9	1.0	13.5		C_L = 50 pF	2-6
t_{PLH}, t_{PHL}	Propagation Delay $\overline{E}_n$ to Z_n	3.3 ±0.3		6.3	10.1	1.0	12.0	ns	C_L = 15 pF	2-6
				8.8	13.6	1.0	15.5		C_L = 50 pF	2-6
		5.0 ±0.5		4.4	6.4	1.0	7.5	ns	C_L = 15 pF	2-6
				5.9	8.4	1.0	9.5		C_L = 50 pF	2-6
C_{IN}	Input Capacitance			4	10		10	pF	V_{CC} = Open	
C_{PD}	Power Dissipation Capacitance			20				pF	(Note 1)	

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = C_{PD} * V_{CC} * f_{IN} + I_{CC}.