P54/74FCT833A/B(P54/74PCT833A/B)
FAST CMOS PARITY BUS TRANSCEIVER

FEATURES

- Function, Pinout, and Drive Compatible with the FCT and F Logic
- FCT-B speed at 7.0ns max. (Com'l)
  FCT-A speed at 10.0ns max. (Com'l)
- CMOS V_{OH} Levels for Low Power Consumption
  — Typically 1/3 of FAST Bipolar Logic
- Edge-rate Control Circuitry for Significantly Improved Noise Characteristics
- ESD protection exceeds 2000V
- Inputs and Outputs Interface Directly with TTL, NMOS, and CMOS Devices
- Outputs Meet Levels Required for CMOS Static RAM Low Power Standby Mode
- 64 mA Sink Current (Com'l), 48 mA (Mil)
  24 mA Source Current (Com'l), 15 mA (Mil)
- Buffered Direction Tri-State Output
- High Speed Bidirectional Bus Transceiver for Processor Organized Devices
- Error Flag with Open-Drain Output
- Manufactured in 0.8 micron PACE Technology™

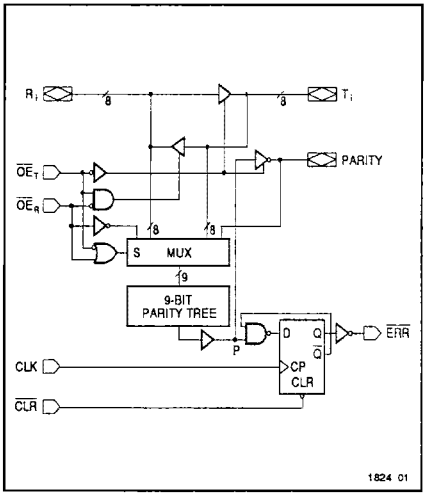
DESCRIPTION

The 'FCT833 is a high-performance bus transceiver designed for two-way communications. It contains an 8-bit data path from the R (port) to the T (port), an 8-bit data path from the T (port) to the R (port), and a 9-bit parity checker/generator. The fault register allows the error flag to be clocked and stored in the register and read at the $\overline{ERR}$ open drain output. The clear ($\overline{CLR}$) input is used to clear the error flag register. The output enable $\overline{OE}_T$ and $\overline{OE}_R$ are used to force the port outputs to the high impedance state so that the device can drive bus lines directly. In addition, $\overline{OE}_T$ and $\overline{OE}_R$ can be used to force a parity error by enabling both lines simultaneously. This transmission of inverting parity gives the designer more system diagnostic capability. The data presented at the output is non-inverted.

The 'FCT833 is manufacturered using PACE Technology™ which is Performance Advanced CMOS Engineered to use 0.8 micron effective channel lengths resulting in 500 picoseconds loaded* internal gate delays. PACE Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection and single event upset protection, and is supported by a Class 1 environment volume production facility.

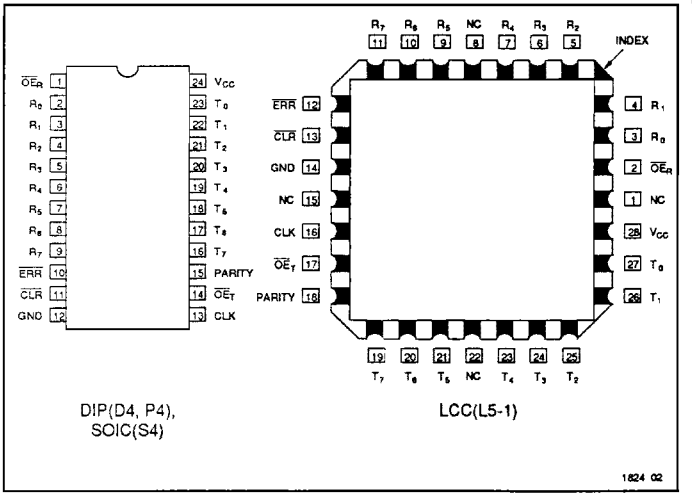
* For a fan-in/fan-out of 4 at 85°C junction temperature and 5.0 V supply. For a fan-in/fan-out of 1, the internal gate delay is 200 picoseconds at room temperature.

FUNCTIONAL BLOCK DIAGRAM



1824 01

PIN CONFIGURATIONS



DIP(D4, P4),
SOIC(S4)

LCC(L5-1)

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ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
I_{IN}	Input Current	–30 to +5.0	mA

1824 Tbl 01

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to V_{CC} + 0.5	V
V_{OUT}	Voltage Applied to Output	–0.5 to V_{CC} + 0.5	V

1824 Tbl 02

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1824 Tbl 03

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1824 Tbl 04

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.35		V		All inputs
V_{CD}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output High Voltage (Except $\overline{ERR}$)	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} – 0.2V	V_{CC} – 0.2	V_{CC}		V		I_{OH} = –32µA
		Military/Commercial (CMOS)	V_{CC} – 0.2	V_{CC}		V	MIN	I_{OH} = –300µA
		Military (TTL)	2.4	4.3		V	MIN	I_{OH} = –15mA
		Commercial (TTL)	2.4	4.3		V	MIN	I_{OH} = –24mA
V_{OL}	Output Low Voltage	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} – 0.2V		GND	0.2	V		I_{OL} = 300µA
		Military/Commercial (CMOS)		GND	0.2	V	MIN	I_{OL} = 300µA
		Military (TTL)		0.3	0.5	V	MIN	I_{OL} = 32mA
		Commercial (TTL)		0.3	0.5	V	MIN	I_{OL} = 48mA
		Commercial (TTL)		0.3	0.5	V	MIN	I_{OL} = 64mA
I_{IH}	Input HIGH Current (Except I/O Pins)				5	µA	MAX	V_{IN} = V_{CC}
I_{IL}	Input LOW Current (Except I/O Pins)				–5	µA	MAX	V_{IN} = GND
I_{IH}	Input HIGH Current[3] (Except I/O Pins)				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current[3] (Except I/O Pins)				–5	µA	MAX	V_{IN} = 0.5V
I_{IH}	Input HIGH Current (I/O Pins only)				15	µA	MAX	V_{IN} = V_{CC}
I_{IL}	Input LOW Current (I/O Pins only)				–15	µA	MAX	V_{IN} = GND
I_{IH}	Input HIGH Current[3] (I/O Pins only)				15	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current[3] (I/O Pins only)				–15	µA	MAX	V_{IN} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120		mA	MAX	V_{OUT} = 0.0V
C_{IN}	Input Capacitance[3]			5	10	pF		All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF		All outputs

1824 Tbl 05

Notes:

1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{os} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
I_{CC}	Quiescent Power Supply Current (CMOS inputs)	0.003	0.5	mA	V_{CC} = MAX, f_1 = 0, Outputs Open, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ mHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}_T$ = GND, $\overline{OE}_R$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$,
I_C	Total Power Supply Current[5]	1.4	3.4	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling, f_0 = 10MHz, $\overline{OE}_T$ = GND, $\overline{OE}_R$ = V_{CC}, f_1 = 2.5MHz, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC}$ -0.2V
		1.9	5.4	mA	V_{CC} = MAX 50% Duty Cycle, Outputs Open, One Bit Toggling, f_0 = 10MHz, $\overline{OE}_T$ = GND, $\overline{OE}_R$ = V_{CC}, f_1 = 2.5MHz, V_{IN} = 3.4V or V_{IN} = GND
		4.0	7.8[4]	mA	V_{CC} = MAX 50% Duty Cycle, Outputs Open, Eight Bits Toggling, f_0 = 10MHz, $\overline{OE}_T$ = GND, $\overline{OE}_R$ = V_{CC}, f_1 = 2.5MHz, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		6.2	16.8[4]	mA	V_{CC} = MAX 50% Duty Cycle, Outputs Open, Eight Bits Toggling, f_0 = 10MHz, $\overline{OE}_T$ = GND, $\overline{OE}_R$ = V_{CC}, f_1 = 2.5MHz, V_{IN} = 3.4V or V_{IN} GND

1824 Tbl 06

Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1

All currents are in milliamps and all frequencies are in megahertz.

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AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	'FCT833A				'FCT833B				Units	Fig. No.
			MIL		COM'L		MIL		COM'L			
			Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max		
t_{PLH} t_{PHL}	Propagation Delay R_i to T_i, T_i to R_i	C_L = 50pF	– –	14.0 14.0	– –	10.0 10.0	– –	10.0 10.0	– –	7.0 7.0	ns ns	1 5
t_{PLH} t_{PHL}	Propagation Delay R_i to T_i, T_i to R_i	C_L = 300pF[2]	– –	21.5 21.5	– –	17.5 17.5	– –	17.5 17.5	– –	14.5 14.5	ns ns	1 5
t_{PLH} t_{PHL}	Propagation Delay R_i to PARITY	C_L = 50pF	– –	20.0 20.0	– –	15.0 15.0	– –	14.0 14.0	– –	10.5 10.5	ns ns	1 5
t_{PLH} t_{PHL}	Propagation Delay R_i to PARITY	C_L = 300pF[2]	– –	27.5 27.5	– –	22.5 22.5	– –	21.5 21.5	– –	18.0 18.0	ns ns	1 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{OE}_R$ to Parity	C_L = 50pF	– –	20.0 20.0	– –	15.0 15.0	– –	14.0 14.0	– –	10.5 10.5	ns ns	1 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{OE}_R$ to PARITY	C_L = 300pF[2]	– –	27.5 27.5	– –	22.5 22.5	– –	21.5 21.5	– –	18.0 18.0	ns ns	1 5
t_{PHL}	Propagation Delay CLK to $\overline{ERR}$	C_L = 50pF	–	16.0	–	12.0	–	11.0	–	8.5	ns	1 5
t_{PLH}	Propagation Delay $\overline{CLR}$ to $\overline{ERR}$	C_L = 50pF	–	16.0	–	12.0	–	11.0	–	8.5	ns	1 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}_R$, $\overline{OE}_T$ to R_i,T_i	C_L = 50pF	– –	16.0 16.0	– –	12.0 12.0	– –	11.0 11.0	– –	8.5 8.5	ns ns	1, 7, 8
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}_R$, $\overline{OE}_T$ to R_i,T_i	C_L = 300pF[2]	– –	23.5 23.5	– –	19.5 19.5	– –	18.5 18.5	– –	16.0 16.0	ns ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}_R$, $\overline{OE}_T$ to R_i,T_i	C_L = 50pF	– –	16.0 16.0	– –	12.0 12.0	– –	11.0 11.0	– –	8.5 8.5	ns ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}_R$, $\overline{OE}_T$ to R_i,T_i	C_L = 5pF[2]	– –	14.7 14.7	– –	10.7 10.7	– –	9.8 9.8	– –	7.2 7.2	ns ns	1, 7, 8

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AC OPERATING REQUIREMENTS

Symbol	Parameter	Test Conditions	'FCT833A				'FCT833B				Units	Fig. No.
			MIL		COM'L		MIL		COM'L			
			Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max		
t_{SU}	T_i PARITY to CLK Set-up Time	C_L = 50pF	16.0	–	12.0	–	11.0	–	8.5	–	ns	4
t_{SU}	Clear Recovery Time $\overline{CLR}$ to CLK		–	20.0	–	15.0	–	14.0	–	10.5	ns	4
t_H	T_i PARITY to CLK Hold Time		0	–	0	–	0	–	0	–	ns	4
t_w(H) t_w(L)	Clock Pulse Width HIGH or LOW		9.5 9.5	– –	7.0 7.0	– –	7.0 7.0		5.5 5.5		ns ns	5
t_w(L)	Clear Pulse Width LOW		9.5		7.0		7.0		5.5		ns	5

Notes:

1624 Tbl 08

1. Minimum limits are guaranteed but not tested on Propagation Delays.
2. These parameters are guaranteed but not tested.

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
I_{IN}	Input Current	–30 to +5.0	mA

1822 Tbl 01

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to V_{CC} + 0.5	V
V_{OUT}	Voltage Applied to Output	–0.5 to V_{CC} + 0.5	V

1822 Tbl 02

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1822 Tbl 03

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1822 Tbl 04

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.35		V		All inputs
V_{CD}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} – 0.2V	V_{CC} – 0.2	V_{CC}		V		I_{OH} = –32µA
		Military/Commercial (CMOS)	V_{CC} – 0.2	V_{CC}		V	MIN	I_{OH} = –300µA
		Military (TTL)	2.4	4.3		V	MIN	I_{OH} = –12mA
		Commercial (TTL)	2.4	4.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} – 0.2V		GND	0.2	V		I_{OL} = 300µA
		Military/Commercial (CMOS)		GND	0.2	V	MIN	I_{OL} = 300µA
		Military (TTL)		0.3	0.5	V	MIN	I_{OL} = 32mA
		Commercial (TTL)		0.3	0.5	V	MIN	I_{OL} = 48mA
		Commercial (TTL)		0.3	0.5	V	MIN	I_{OL} = 64mA
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = V_{CC}
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = GND
I_{IH}	Input HIGH Current[3]				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current[3]				–5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current				10	µA	MAX	V_{OUT} = V_{CC}
I_{OZL}	Off State I_{OUT} LOW-Level Output Current				–10	µA	MAX	V_{OUT} = GND
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current[3]				10	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Output Current[3]				–10	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF	MAX	All outputs

1822 Tbl 05

Notes:

1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{os} tests should be performed last.
3. This parameter is guaranteed but not tested.

P54/74FCT11374 (P54/74PCT11374)
OCTAL D FLIP-FLOPS WITH 3-STATE OUTPUTS

FEATURES

- Function, Pinout, and Drive Compatible with the FCT, F Logic and P54/74ACT11374
- FCT speed at 4.5ns max. (Com'l)
- CMOS V_{OH} Levels for Low Power Consumption — Typically 1/3 of FAST Bipolar Logic
- Edge-rate Control Circuitry for Significantly Improved Noise Characteristics
- ESD protection exceeds 2000V
- Inputs and Outputs Interface Directly with TTL, NMOS, and CMOS Devices
- Outputs Meet Levels Required for CMOS Static RAM Low Power Standby Mode
- 64 mA Sink Current (Com'l), 48 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)
- 5.0V ± 10% (Mil), 5.0V ± 5% (Commercial)
- Multiple Center Power and Ground Pins
- Edge Triggered D Type Inputs
- 250MHz Typical Toggle Rate
- Buffered Positive Edge Trigered Clock
- Input Clamp Diode to Limit Bus Reflections
- Significantly Improved Switching Characteristics
- Manufactured in 0.8 micron PACE Technology™

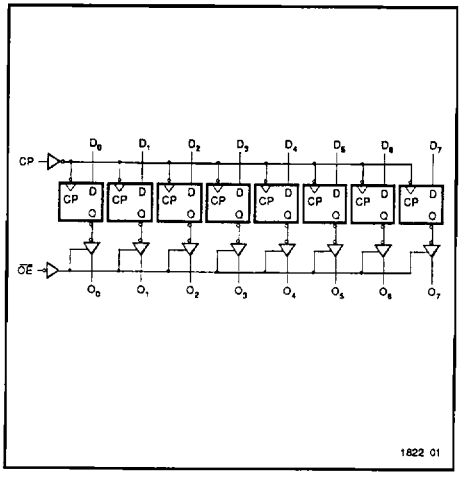
DESCRIPTION

The 'FCT11374 are high-speed low power octal D-type flip-flops featuring separate D-type inputs for each flip-flop. Both devices have 3-state outputs for bus oriented applications. A buffered clock (CP) and output enable ($\overline{OE}$) are common to all flip-flops. The eight flip-flops contained in the 'FCT11374 will store the state of their individual D inputs that meet the setup and hold time requirements on the low-to-high clock (CP) transition. When $\overline{OE}$ is LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs will be in the high impedance state. The state of output enable does not affect the state of the flip-flops.

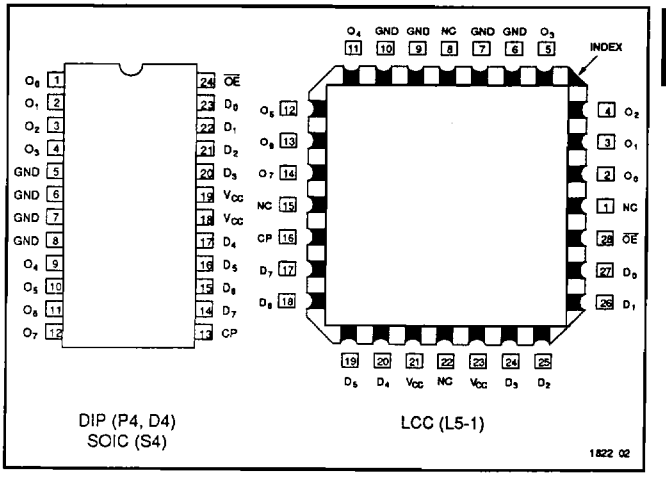
The 'FCT11374 is manufactured with PACE II Technology™ which is Performance Advanced CMOS Engineered with two-level metal and epitaxial substrates to use 0.7 micron effective channel lengths giving 400 picosecond loaded* internal gate delays. This product incorporates the (lower inductance) multiple center power and ground pinout, hence significantly improving switching noise characteristics. This pinout is compatible with 54/74ACT11374.

*For a fan-in/fan-out of 4 at 85°C junction temperature and 5V supply.

LOGIC DIAGRAMS



PIN CONFIGURATION



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