FEMTOCLOCKS™ CRYSTAL-TO-LVCMOS/LVTTL CLOCK GENERATOR

ICS840001I

General Description

The ICS840001I is a Fibre Channel Clock Generator and a member of the HiPerClocks™ family of high performance devices from ICS. The ICS840001I uses a 26.5625MHz crystal to synthesize either 106.25MHz or 212.5MHz, using the FREQ_SEL pin. The ICS840001I has excellent phase jitter performance, over the 637kHz – 5MHz integration range. The ICS840001I is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

Features

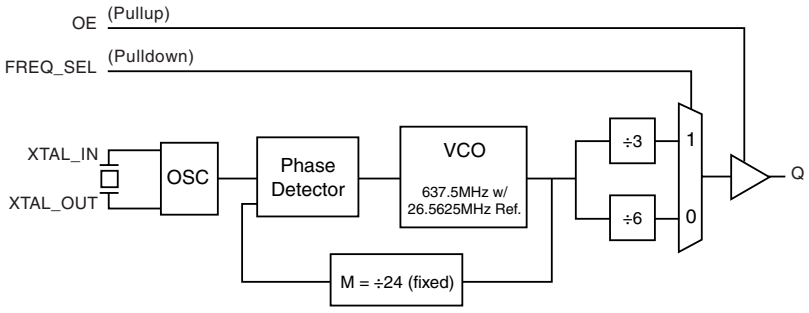
- 1 LVCMOS/LVTTL output, 7Ω typical output impedence
- Crystal oscillator interface designed for 26.5625MHz, 18pF parallel resonant crystal
- Selectable 106.25MHz or 212.5MHz output frequency
- VCO range: 560MHz to 680MHz
- RMS phase jitter @ 106.25MHz, using a 26.5625MHz crystal (637kHz - 5MHz): 0.70ps (typical)
- 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature

Function Table

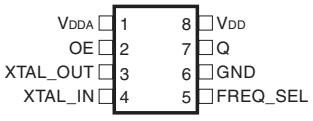
Input	Output Frequencies
FREQ_SEL	
0	106.25MHz (Default)
1	212.5MHz

Crystal: 26.5625MHz

Block Diagram



Pin Assignment



ICS840001I
8-Lead TSSOP
4.40mm x 3.0mm x 0.925mm
package body
G Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{DDA}	Power		Analog supply pin.
2	OE	Input	Pullup	Output enable pin. When HIGH, Q output is enabled. When LOW, forces Q to HiZ state. LVCMOS/LVTTL interface levels.
3, 4	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
5	FREQ_SEL	Input	Pulldown	Frequency select pin. LVCMOS/LVTTL interface levels.
6	GND	Power		Power supply ground.
7	Q	Output		Single-ended clock output. LVCMOS/LVTTL interface levels. 7Ω typical output impedance.
8	V_{DD}	Power		Core supply pin.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance	V_{DD}, V_{DDA} = 3.465V		TBD		pF
		V_{DD}, V_{DDA} = 2.625V		TBD		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance		5	7	12	Ω

TABLE 3. CONTROL FUNCTION TABLE

Control Inputs	Output
OE	**Q**
0	Hi-Z
1	Active

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	101.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			75		mA
I_{DDA}	Analog Supply Current			8		mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = 2.5V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			73		mA
I_{DDA}	Analog Supply Current			8		mA

Table 4C. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
			V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	FREQ_SEL	$V_{DD} = V_{IN}$ = 3.465V or 2.625V			150	µA
		OE	$V_{DD} = V_{IN}$ = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	FREQ_SEL	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
		OE	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1		V_{DD} = 3.465V	2.6			V
			V_{DD} = 2.625V	1.8			V
V_{OL}	Output Low Voltage; NOTE 1		V_{DD} = 3.465V or 2.625V			0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DD}/2$. See Parameter Measurement Information Section, "Output Load Test Circuit" diagrams.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency			26.5625		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

TABLE 6A. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V±5\%$, $T_A = -40°C$ TO $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	FREQ_SEL = 1	186.66	212.5	226.66	MHz
		FREQ_SEL = 0	93.33	106.25	113.33	MHz
$t$jit(Ø)	RMS Phase Jitter (Random); NOTE 1	fOUT = 106.25MHz, (637kHz to 5MHz)		0.70		ps
		fOUT = 212.5MHz, (2.55MHz to 20MHz)		0.50		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		400		ps
odc	Output Duty Cycle			50		%

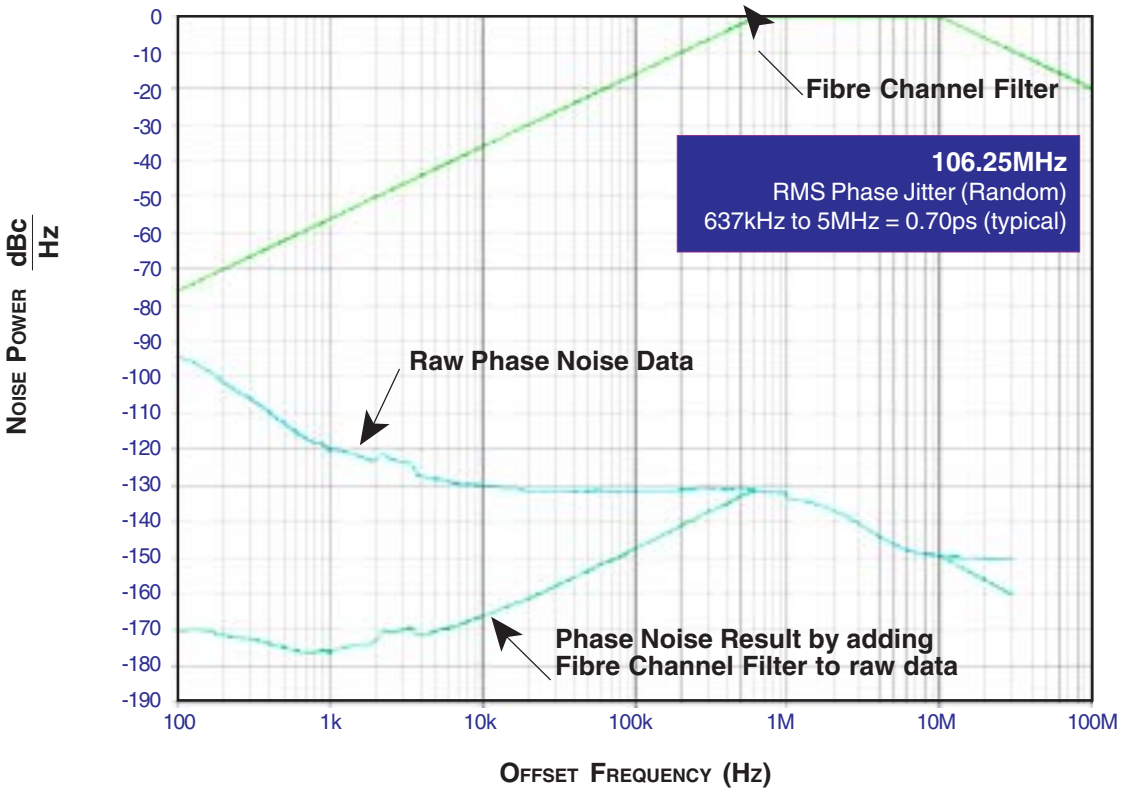
All parameters are characterized @ 212.5MHz and 106.25MHz.
NOTE 1: Please refer to the Phase Noise Plots following this section.

TABLE 6B. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 2.5V±5\%$, $T_A = -40°C$ TO $85°C$

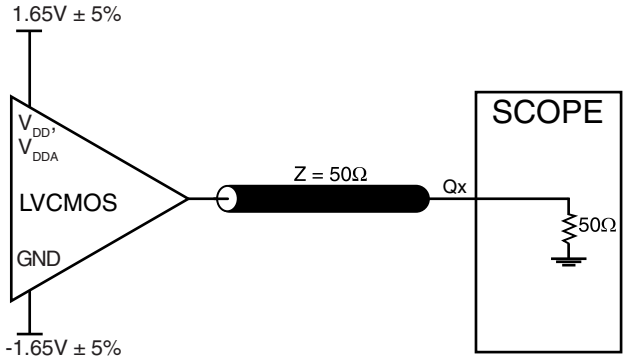
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	FREQ_SEL = 1	186.66	212.5	226.66	MHz
		FREQ_SEL = 0	93.33	106.25	113.33	MHz
$t$jit(Ø)	RMS Phase Jitter (Random); NOTE 1	fOUT = 106.25MHz, (637kHz to 5MHz)		0.70		ps
		fOUT = 212.5MHz, (2.55MHz to 20MHz)		0.50		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		450		ps
odc	Output Duty Cycle			50		%

All parameters are characterized @ 212.5MHz and 106.25MHz.
NOTE 1: Please refer to the Phase Noise Plots following this section.

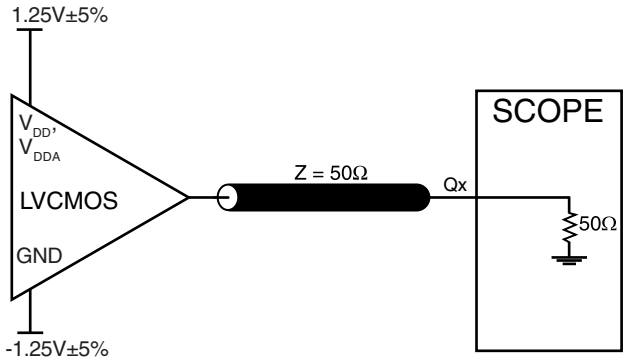
TYPICAL PHASE NOISE AT 106.25MHZ



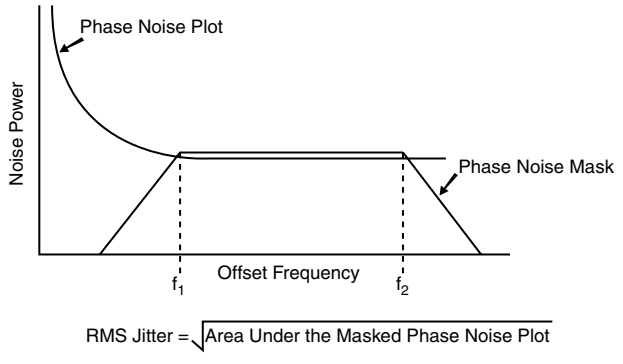
PARAMETER MEASUREMENT INFORMATION



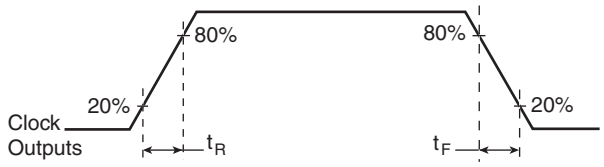
3.3V OUTPUT LOAD AC TEST CIRCUIT



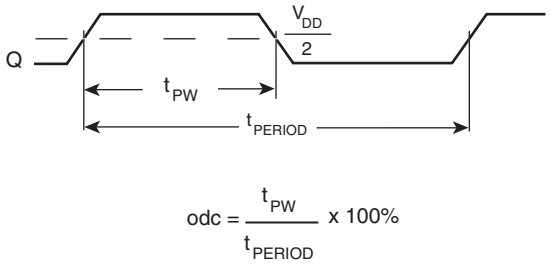
2.5V OUTPUT LOAD AC TEST CIRCUIT



RMS PHASE JITTER



OUTPUT RISE/FALL TIME



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS840001I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10μF and a .01μF bypass capacitor should be connected to each V_{DDA} pin.

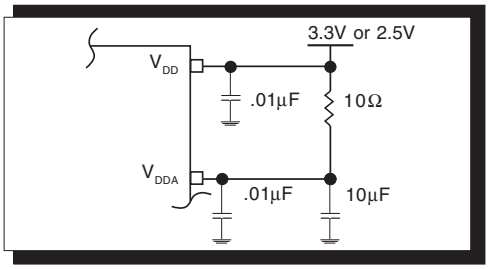


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS840001I has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 26.5625MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

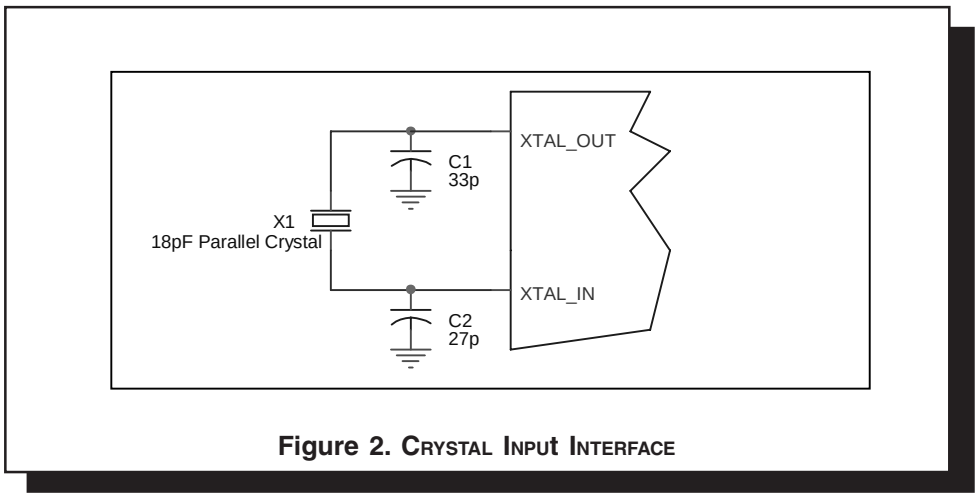


Figure 2. CRYSTAL INPUT INTERFACE

LAYOUT GUIDELINE

Figure 3A shows a schematic example of the ICS840001I. An example of LVCMOS termination is shown in this schematic. Additional LVCMOS termination approaches are shown in the LVCMOS Termination Application Note. In this example, an 18 pF parallel resonant 26.5625MHz crystal is used. The C1=27pF and C2=33pF are recommended for frequency accuracy. For different board layout, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. The output frequency can be set at either 106.25MHz or 212.5MHz. Leaving the R1 un-installed (or install 1k Ω pull-down) will set the output frequency at 106.25MHz. Installing the R1 pull up will set the output frequency at 212.5MHz.

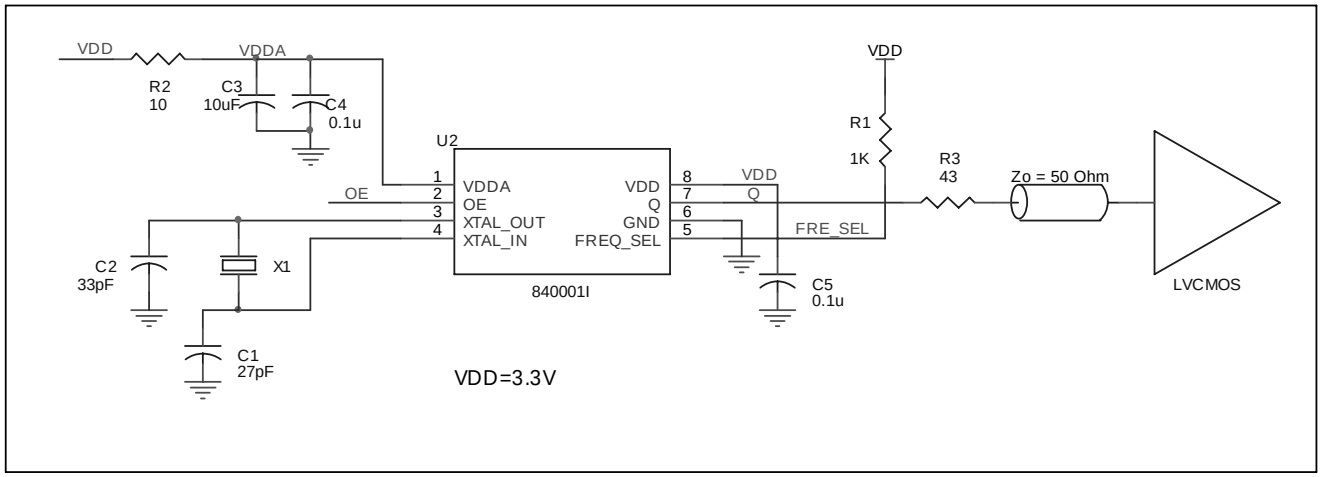


FIGURE 3A. ICS840001I SCHEMATIC EXAMPLE

PC BOARD LAYOUT EXAMPLE

Figure 3B shows an example of P.C. board layout. The crystal X1 footprint in this example allows either surface mount (HC49S) or through hole (HC49) package. C3 is 0805. C1 and C2 are 0402. Other resistors and capacitors are 0603. This layout assumes that the board has clean analog power and ground planes.

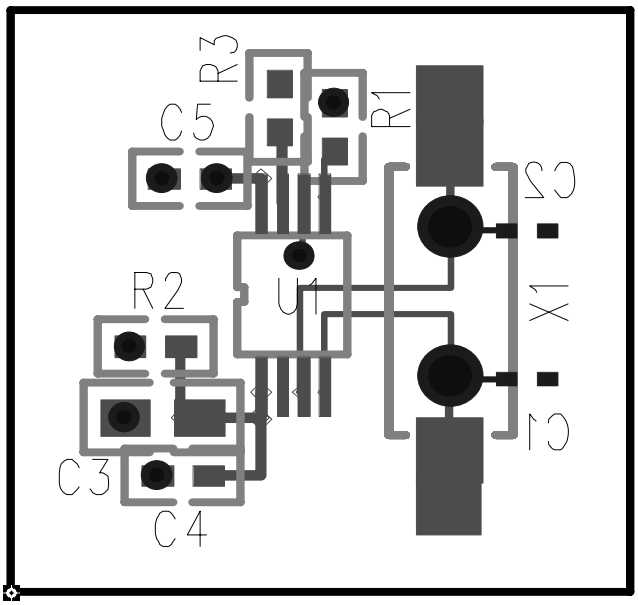


FIGURE 3B. ICS840001I PC BOARD LAYOUT EXAMPLE

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD TSSOP

θ_{JA} by Velocity (Meters Per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

TRANSISTOR COUNT

The transistor count for ICS840001I is: 1521

Package Outline - G Suffix for 8 Lead TSSOP

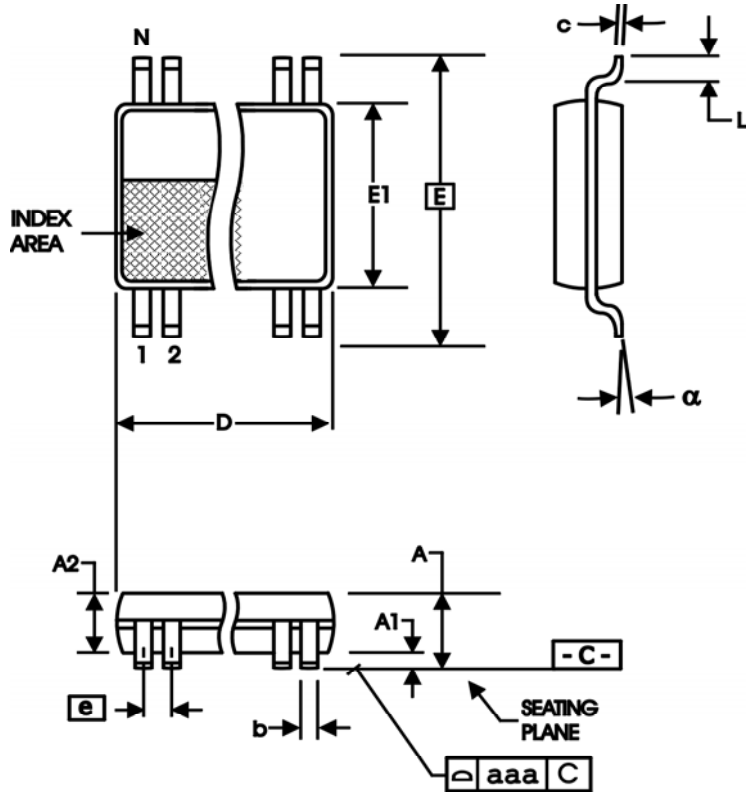


Table 8. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	8	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS840001AGI	001AI	8 lead TSSOP	tube	-40°C to 85°C
ICS840001AGIT	001AI	8 lead TSSOP	2500 tape & reel	-40°C to 85°C

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