M5M5408AFP,TP,RT-55L, -70L,-10L, -55LL,-70LL,-10LL

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5408A is a 4194304-bit CMOS Static RAM organized as 524288-word by 8-bit. This device is fabricated using Mitsubishi's high-performance silicon-gate CMOS technology. This state-of-the-art process technology, combined with innovative circuit design techniques, yields high-density and low-power devices. The M5M5408A is suitable for memory applications where high reliability, large storage, simple interfacing and battery back-up are important design objectives.

The M5M5408A is available in 32-pin plastic SOP(M5M5408AFP) , 32-pin plastic normal-lead-bend TSOP (M5M5408ATP) and 32-pin plastic reverse-lead-bend TSOP (M5M5408ART) packages. Two types of TSOP's are suitable for Surface Mounting on double-sided printed circuit boards.

FEATURES

Type name	Access time (max.)	Power supply current	
		Active (max.)	Stand-by (max.)
M5M5408AFP,TP,RT-55L M5M5408AFP,TP,RT-70L M5M5408AFP,TP,RT-10L	55ns 70ns 100ns	30mA (1MHz)	100μA (Vcc=5.5V*)
M5M5408AFP,TP,RT-55LL M5M5408AFP,TP,RT-70LL M5M5408AFP,TP,RT-10LL	55ns 70ns 100ns	30mA (1MHz)	20μA (Vcc=5.5V*) 0.4μA (Vcc=3V**)

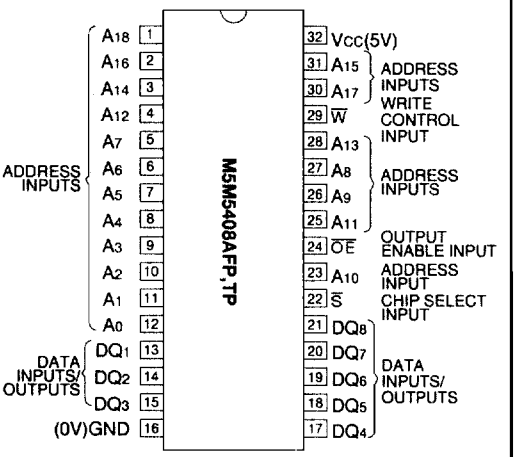
* at 70℃/**at 25 ℃

- Single +5V power supply
- No clocks, No refresh
- All inputs and outputs are TTL compatible
- Easy memory expansion and power down by $\overline{S}$
- Data retention supply voltage=2.0V to 5.5V
- Three-state outputs: OR-tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O
- Battery backup capability
- Small stand-by current ..... 0.4 μA(typ)
- Package
  - M5M5408AFP : 32 pin 525 mil SOP
  - M5M5408ATP : 32 pin 400 mil TSOP(II)
  - M5M5408ART : 32 pin 400 mil TSOP(II)

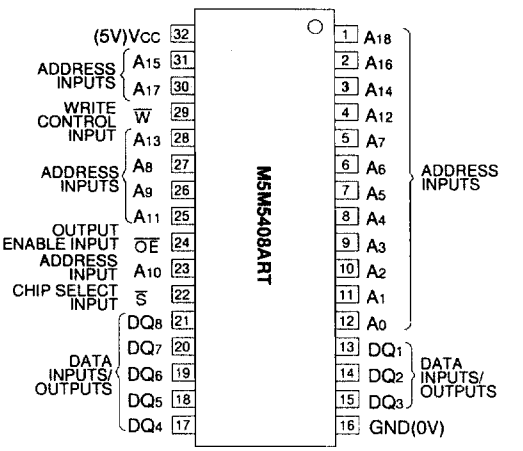
APPLICATION

Small capacity memory units, IC card, Battery operating system

PIN CONFIGURATION (TOP VIEW)



Outline 32P2M-A (FP)
32P3Y-H (TP)



Outline 32P3Y-J

FUNCTION

The operation mode of the M5M5408A is determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$ or $\overline{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

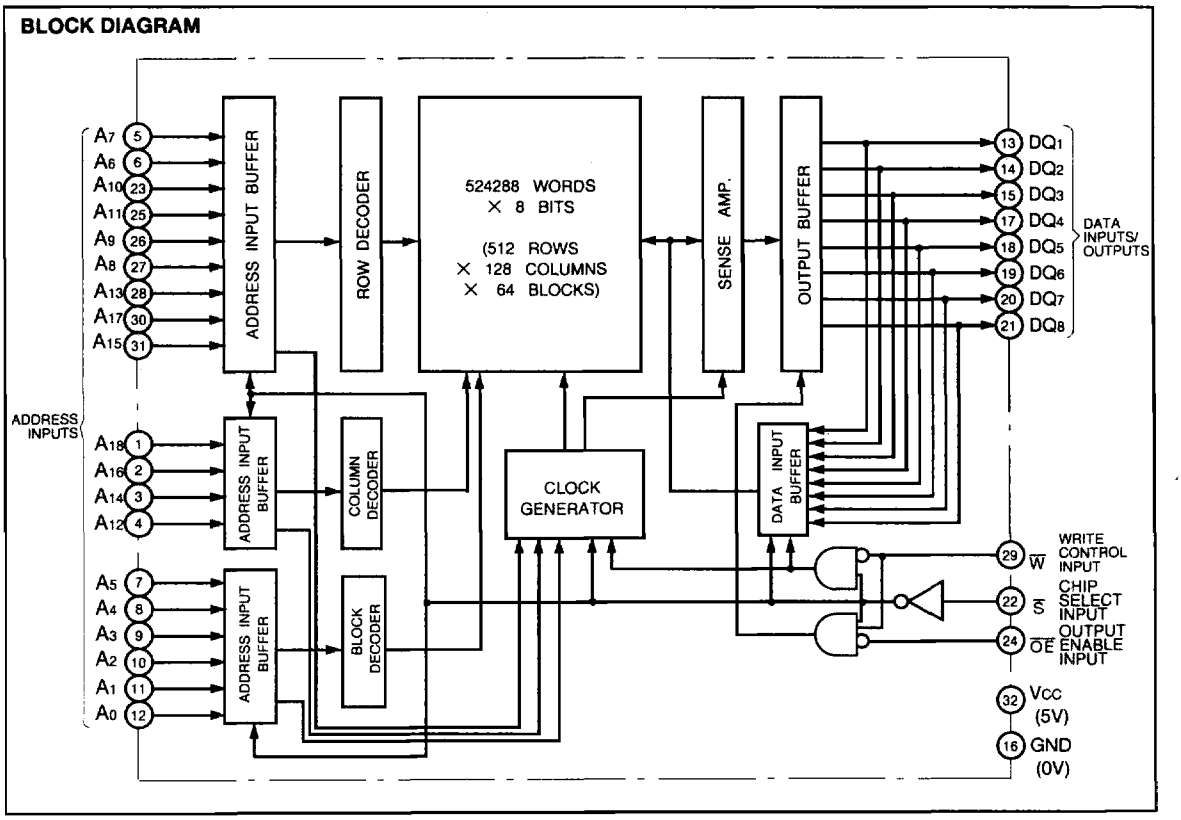
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state($\overline{S}$=L).

When setting $\overline{S}$ at a high level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	Data input	Active
L	H	L	Read	Data output	Active
L	H	H	Read	High-impedance	Active

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3～7	V
V_I	Input voltage		−0.3*～V_{CC}+0.3	V
V_O	Output voltage		0～V_{CC}	V
P_d	Power dissipation	Ta = 25℃	700	mW
T_{opr}	Operating temperature		0～70	℃
T_{stg}	Storage temperature		−65～150	℃

* −3.0V in case of AC (Pulse width ≦ 50ns)

DC ELECTRICAL CHARACTERISTICS (Ta = 0～70℃, V_{CC} = 5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{IH}	High-level input voltage			2.2		V_{CC}+0.3	V
V_{IL}	Low-level input voltage			−0.3*		0.8	V
V_{OH}	High-level output voltage	I_{OH} = −1mA		2.4			V
		I_{OH} = −0.1mA		V_{CC}−0.5			V
V_{OL}	Low-level output voltage	I_{OL} = 2mA				0.4	V
I_I	Input leakage current	Inputs = 0～V_{CC}				±1	μA
I_O	Output leakage current	$\overline{S}$ = V_{IH} $\overline{OE}$ = V_{IH}, DQ =0 ～V_{CC}				±1	μA
I_{CC1}	Active supply current (AC, MOS-level)	$\overline{S}$≦0.2V Other inputs≦0.2V or ≧V_{CC}−0.2V DQ = open (duty 100%)	Min cycle		50	80	mA
			1MHz		25	30	
I_{CC2}	Active supply current (AC, TTL-level)	$\overline{S}$ = V_{IL} Other inputs = V_{IH} or V_{IL} DQ = open (duty 100%)	Min cycle		60	90	mA
			1MHz		30	40	
I_{CC3}	Stand-by current	$\overline{S}$ ≧ V_{CC}−0.2V, Other inputs = 0～V_{CC}	-L			100	μA
			-LL		1	20	μA
I_{CC4}	Stand-by current	$\overline{S}$ = V_{IH}, other inputs = 0～V_{CC}				3	mA

* −3.0V in case of AC (Pulse width ≦ 50ns)

CAPACITANCE (Ta = 0～70℃, V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
C_I	Input capacitance	V_I = GND, V_I = 25mV rms, f = 1MHz			6	pF
C_O	Output capacitance	V_O = GND, V_O = 25mV rms, f = 1MHz			8	pF

Note 1. Direction for current flowing into IC is indicated as positive value.
2. Typical value is for Ta=25℃ and V_{CC}=5.0V
3. C_I and C_O are random samples ,not production tested.

AC ELECTRICAL CHARACTERISTICS (Ta=0~70℃, Vcc=5V±10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse ····· V_{IH}=2.4V, V_{IL}=0.6V(AFP,TP,RT-70L,-10L,-70LL,-10LL)
V_{IH}=3.0V, V_{IL}=0V(AFP,TP,RT-55L,-55LL)
Input rise and fall time ····· 5ns
Output reference level ····· V_{OH}=V_{OL}=1.5V
For t_{en} and t_{dis}, transition is measured ±500mV from steady state voltage
Output loads ····· Fig. 1; C_L=100pF(AFP,TP,RT-70L,-10L,-70LL,-10LL)
C_L=30pF(AFP,TP,RT-55L,-55LL)
C_L=5pF (for t_{en},t_{dis})

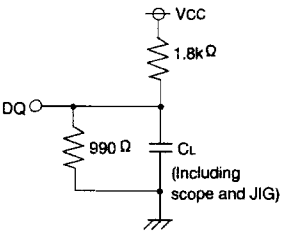


Fig.1 Output load

(2) READ CYCLE

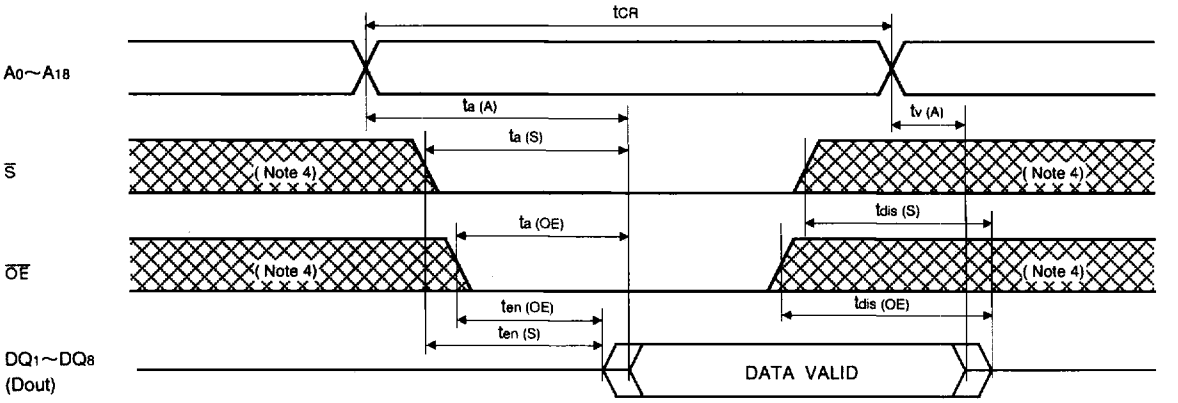
Symbol	Parameter	Limits						Unit
		M5M5408AFP,TP,RT -55L,55LL		M5M5408AFP,TP,RT -70L,70LL		M5M5408AFP,TP,RT -10L,10LL		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CR}	Read cycle time	55		70		100		ns
$t_{a(A)}$	Address access time		55		70		100	ns
$t_{a(S)}$	Chip select access time		55		70		100	ns
$t_{a(OE)}$	Output enable access time		25		35		50	ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high		20		25		35	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		20		25		35	ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	10		10		10		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		5		5		ns
$t_{v(A)}$	Data valid time after address change	10		10		10		ns

(3) WRITE CYCLE

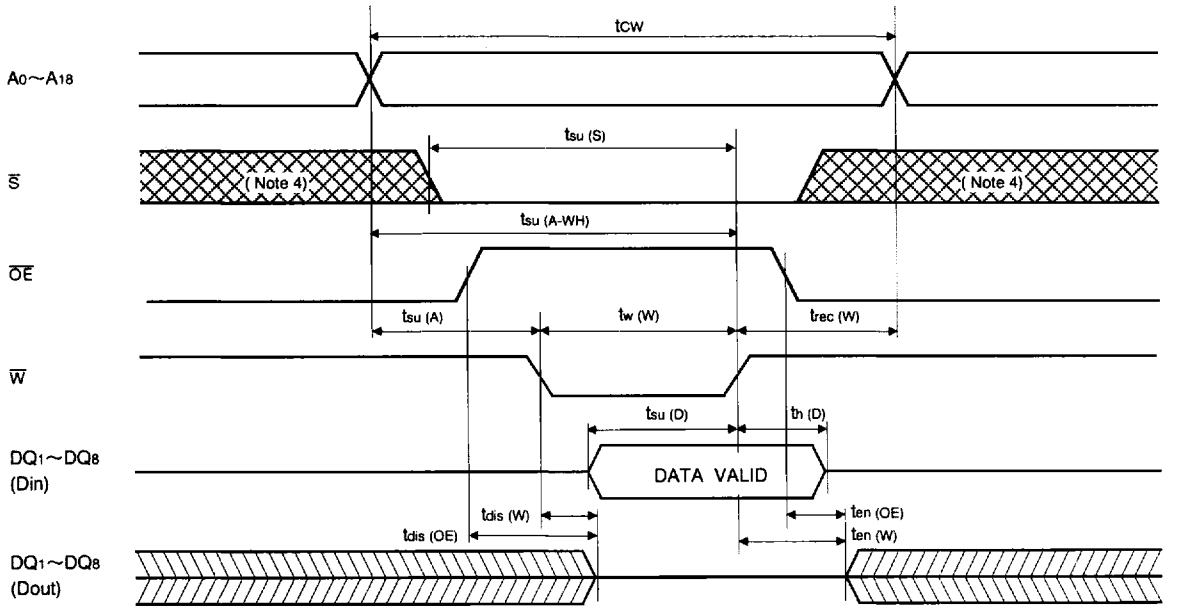
Symbol	Parameter	Limits						Unit
		M5M5408AFP,TP,RT -55L,55LL		M5M5408AFP,TP,RT -70L,70LL		M5M5408AFP,TP,RT -10L,10LL		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CW}	Write cycle time	55		70		100		ns
$t_{w(W)}$	Write pulse width	40		50		60		ns
$t_{su(A)}$	Address set up time	0		0		0		ns
$t_{su(A-WH)}$	Address set up time with respect to $\overline{W}$ high	50		60		80		ns
$t_{su(S)}$	Chip select set up time	50		60		80		ns
$t_{su(D)}$	Data set up time	25		30		35		ns
$t_{h(D)}$	Data hold time	0		0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		0		ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low		20		25		35	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		20		25		35	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	5		5		5		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		5		5		ns

(4) TIMING DIAGRAMS

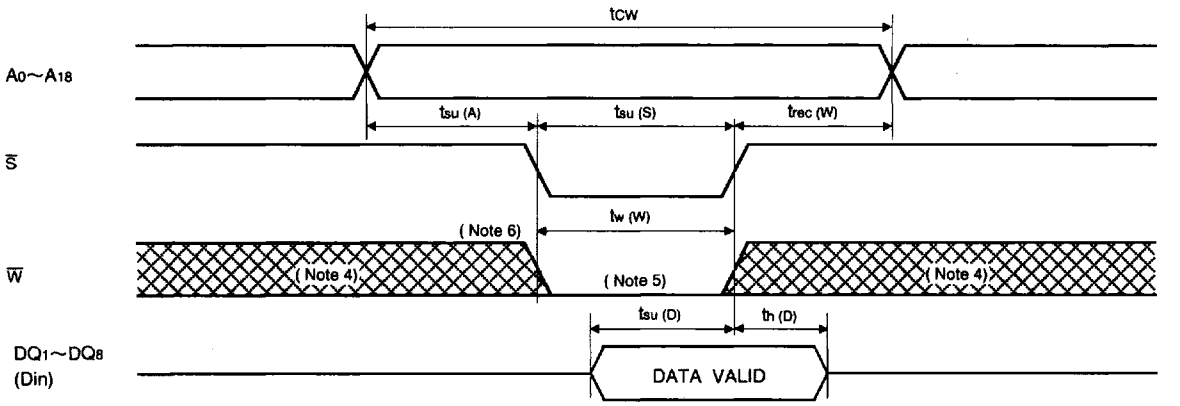
Read cycle



Write cycle ($\overline{WE}$ control mode)



Write cycle ($\overline{S}$ control mode)



Note 4: Hatching indicates the state is "don't care".
5: A Write occurs during the overlap of a low $\overline{S}$ and a low $\overline{W}$.
6: If $\overline{W}$ goes low simultaneously with or prior to $\overline{S}$, the output remains in the high-impedance state.
7: Don't apply inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS
(1) ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
$V_{CC\ (PD)}$	Power down supply voltage			2			V
$V_{I\ (\overline{S})}$	Chip select input $\overline{S}$	$V_{CC\ (PD)} \geqq 2.2V$		2.2			V
		$2.2V \geqq V_{CC\ (PD)} \geqq 2.0V$			$V_{CC(PD)}$		V
$I_{CC\ (PD)}$	Power down supply current	V_{CC} =3V, $\overline{S} \geqq V_{CC}-0.2V$, other inputs = 0~3V	-L			50	μA
			-LL		0.4	10*	μA

* $I_{CC\ (PD)}$ = 1 μA at Ta=25℃

(2) TIMING REQUIREMENTS (Ta=0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(PD)}$	Power down set up time		0			ms
$t_{rec(PD)}$	Power down recovery time		5			ms

(3) TIMING DIAGRAM
$\overline{S}$ control mode