T-46-07-09

National Semiconductor

DM74AS175A Quad D Flip-Flop with Clear

General Description

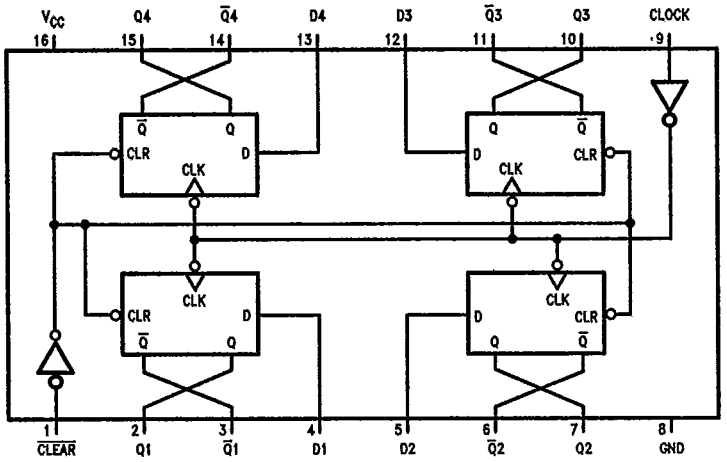
These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. This device has an asynchronous clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either a high or low level, the D input signal has no effect at the output.

Features

- Advanced Oxide-Isolated Ion-Implanted Schottky TTL process
- Pin and Functional compatible with LS and Schottky family counterpart
- Switching performance guaranteed over full temperature and V_{CC} supply range

Connection Diagram



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Order Number DM74AS175AN
See NS Package Number N16A*

Function Table

Inputs			Outputs	
$\overline{CLEAR}$	Clock	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = High Logic State

L = Low Logic State

Q_0 = The level of Q before the indicated steady-state input conditions were established.

↑ = Transition from Low Logic Level to High Logic Level

*Contact your local NSC representative about surface mount (M) package availability.

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Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temp. Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Typical θ_{JA} N Package	67.5°C/W

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−2	mA
I_{OL}	Low Level Output Current				20	mA
f_{CLOCK}	Clock Frequency		0		100	MHz
t_W	Pulse Width	Clock High	4			ns
		Clock Low	5			
		Clear	5			
t_{Setup}	Setup Time	Data	3			ns
		$\overline{\text{CLEAR}}$ Inactive	6			
t_{HOLD}	Data Input Hold Time		1			ns
T_A	Operating Free Air Temperature Range		0		70	°C

Electrical Characteristics (over recommended operating free air temperature range)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA			−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = Max, V_{CC} = 4.5V to 5.5V	V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max, V_{IH} = 2V		0.35	0.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.5V, V_I = 7V			100	μA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_I = 0.4V			−500	μA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V (Note 1)		22.5	34	mA

Note 1: I_{CC} is measured with D inputs and CLEAR grounded, and clock at 4.5V.

Switching Characteristics over recommended operating free air temperature range (Note 2)

Symbol	Parameter	From (Input)	To (Output)	Conditions	Min	Max	Units
f_{MAX}	Maximum Clock Frequency			V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 500Ω, T_A = Min to Max	100		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	$\overline{\text{CLEAR}}$	$\overline{Q}$		4	9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	$\overline{\text{CLEAR}}$	Q		4.5	13	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock	Q or $\overline{Q}$		4	7.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock	Q or $\overline{Q}$		4	10	ns

Note 2: See Section 1 for test waveforms and output load.

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Logic Diagram

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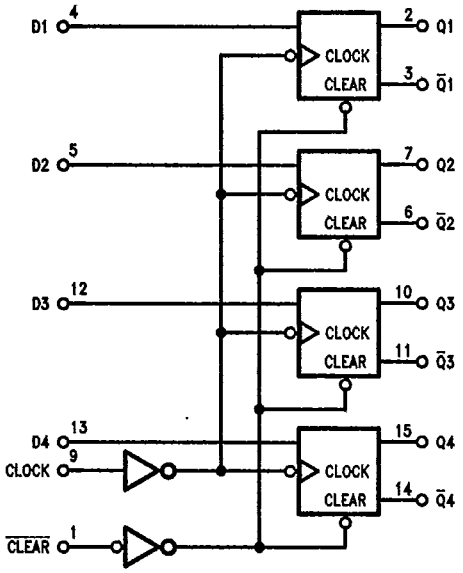

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