HD74HC175

Quad. D-type Flip-Flops (with Clear)

REJ03D0585-0300
Rev.3.00
Jan 31, 2006

Description

Information at the D inputs of the HD74HC175 is transferred to the Q and $\overline{Q}$ outputs on the positive going edge of the clock pulse. Both true and compliment outputs from each flip-flop are externally available. All four flip-flops are controlled by a common clock and a common clear. Clearing is accomplished by a negative pulse at the clear input. All four Q outputs are cleared to a logic low level and all four $\overline{Q}$ outputs to a logic high level.

Features

- High Speed Operation: t_{pd} (Clock to Q) = 14 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC} = 2 to 6 V
- Low Input Current: 1 µA max
- Low Quiescent Supply Current: I_{CC} (static) = 4 µA max (Ta = 25°C)
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC175P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—
HD74HC175TELL	TSSOP-16 pin	PTSP0016JB-A (TTP-16DAV)	T	ELL (2,000 pcs/reel)

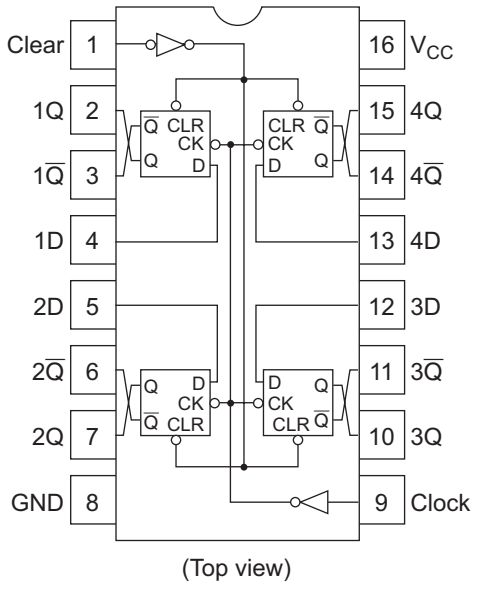
Note: Please consult the sales office for the above package availability.

Function Table

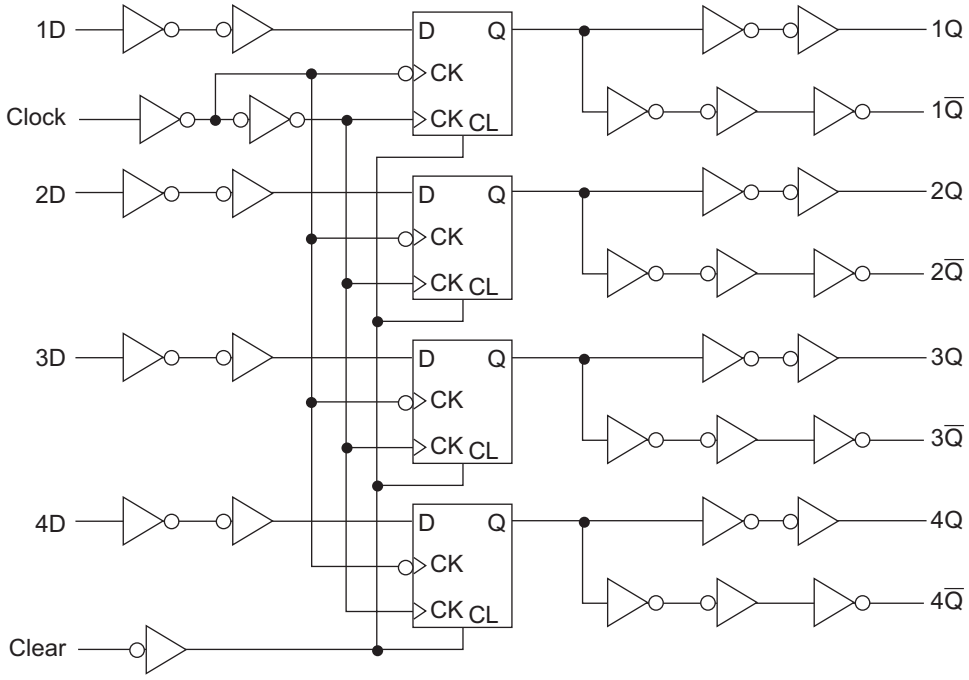
Inputs			Output	
Clear	Clock	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	no change	

H : High level
L : Low level
X : Irrelevant

Pin Arrangement



Logic Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	V_{CC}	–0.5 to 7.0	V
Input / Output voltage	Vin, Vout	–0.5 to V_{CC} +0.5	V
Input / Output diode current	I_{IK}, I_{OK}	±20	mA
Output current	I_O	±25	mA
V_{CC}, GND current	I_{CC} or I_{GND}	±50	mA
Power dissipation	P_T	500	mW
Storage temperature	Tstg	–65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	2 to 6	V	
Input / Output voltage	V_{IN}, V_{OUT}	0 to V_{CC}	V	
Operating temperature	Ta	–40 to 85	°C	
Input rise / fall time*1	t_r, t_f	0 to 1000	ns	V_{CC} = 2.0 V
		0 to 500		V_{CC} = 4.5 V
		0 to 400		V_{CC} = 6.0 V

Note: 1. This item guarantees maximum limit when one input switches.
Waveform: Refer to test circuit of switching characteristics.

Electrical Characteristics

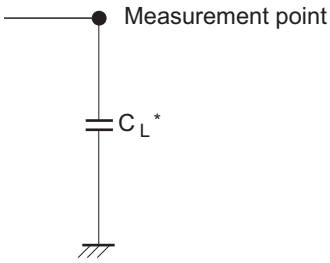
Item	Symbol	V_{CC} (V)	Ta = 25°C			Ta = –40 to+85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V_{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V_{IH} or V_{IL}	I_{OH} = –20 µA
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I_{OH} = –4 mA
		6.0	5.68	—	—	5.63	—			I_{OH} = –5.2 mA
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V_{IH} or V_{IL}	I_{OL} = 20 µA
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			I_{OL} = 4 mA
		6.0	—	—	0.26	—	0.33			I_{OL} = 5.2 mA
Input current	Iin	6.0	—	—	±0.1	—	±1.0	µA	Vin = V_{CC} or GND	
Quiescent supply current	I_{CC}	6.0	—	—	4.0	—	40	µA	Vin = V_{CC} or GND, Iout = 0 µA	

Switching Characteristics

(C_L = 50 pF, Input t_r = t_f = 6 ns)

Item	Symbol	V_{CC} (V)	Ta = 25°C			Ta = –40 to +85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	f_{max}	2.0	—	—	6	—	5	MHz	
		4.5	—	—	30	—	24		
		6.0	—	—	35	—	28		
Propagation delay time	t_{PLH}, t_{PHL}	2.0	—	—	150	—	190	ns	Clock to Q or $\overline{Q}$
		4.5	—	14	30	—	38		
		6.0	—	—	26	—	33		
		2.0	—	—	185	—	230	ns	Clear to Q or $\overline{Q}$
		4.5	—	14	37	—	46		
		6.0	—	—	31	—	39		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	Data to Clock
		4.5	20	3	—	25	—		
		6.0	17	–	—	21	—		
Hold time	t_h	2.0	5	—	—	5	—	ns	Clock to Data
		4.5	5	–1	—	5	—		
		6.0	5	—	—	5	—		
Removal time	t_{rem}	2.0	100	—	—	125	—	ns	Clear to Clock
		4.5	20	–1	—	25	—		
		6.0	17	—	—	21	—		
Pulse width	t_w	2.0	80	—	—	100	—	ns	Clock, Clear
		4.5	16	9	—	20	—		
		6.0	14	—	—	17	—		
Output rise/fall time	t_{TLH}, t_{THL}	2.0	—	—	75	—	95	ns	
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	Cin	—	—	5	10	—	10	pF	

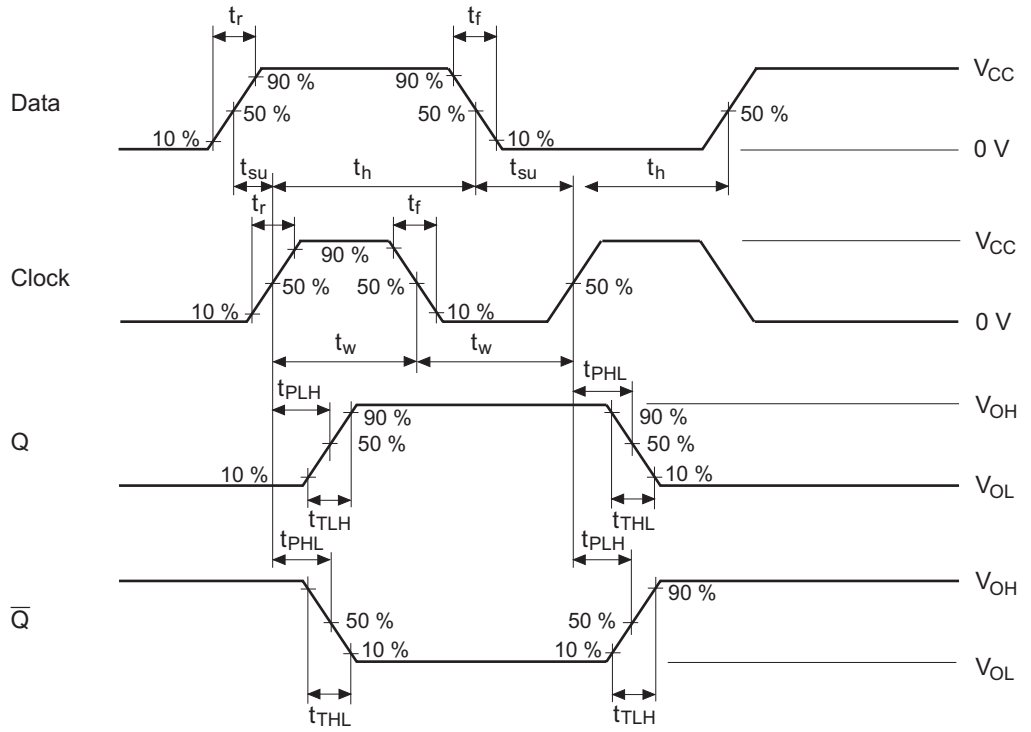
Test Circuit



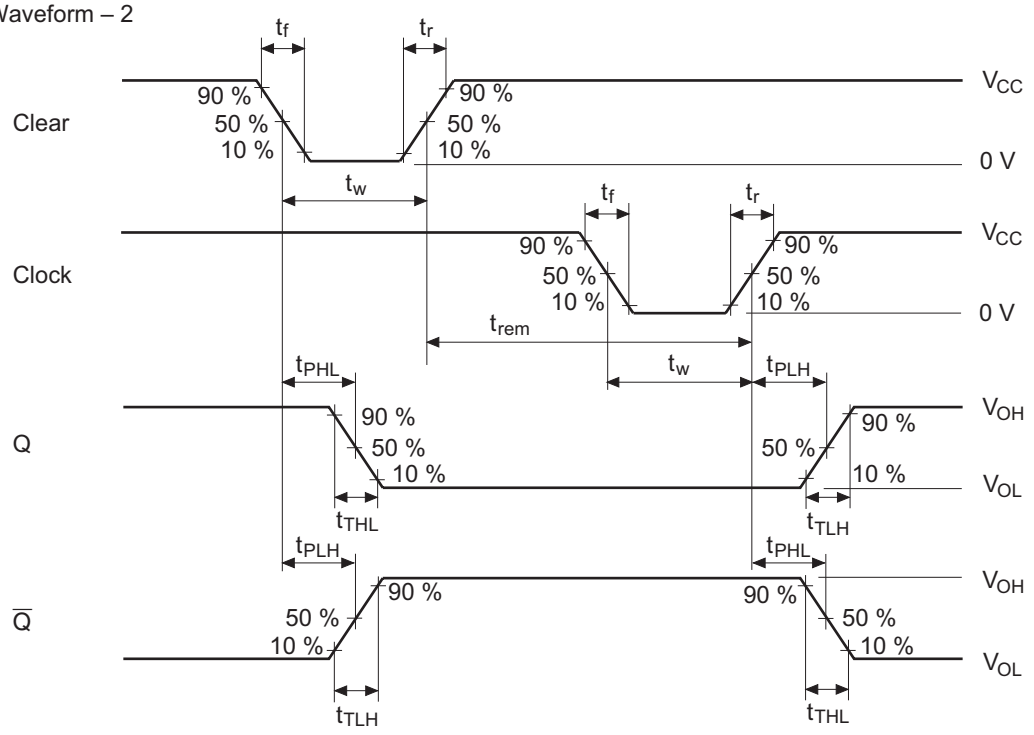
Note: C_L includes the probe and fig capacitance.

Waveforms

• Waveform – 1



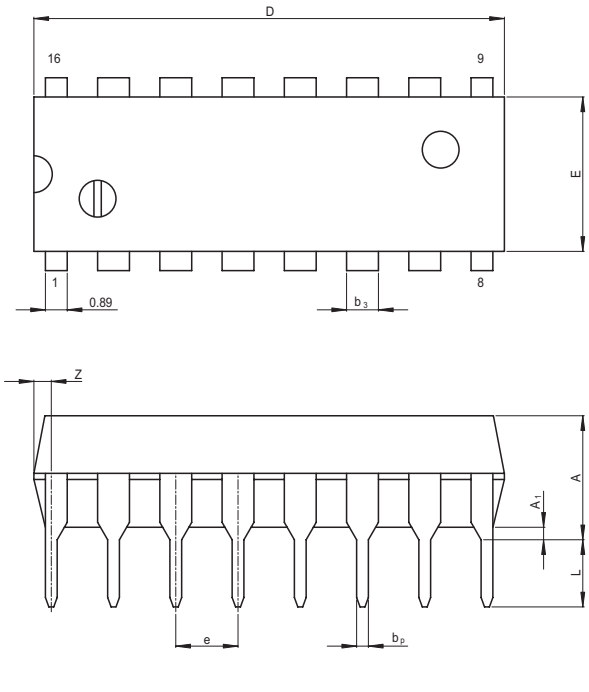
• Waveform – 2



Note : Clock Input : PRR ≤ 1 MHz, Zo = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns
Data Input : PRR ≤ 500 kHz

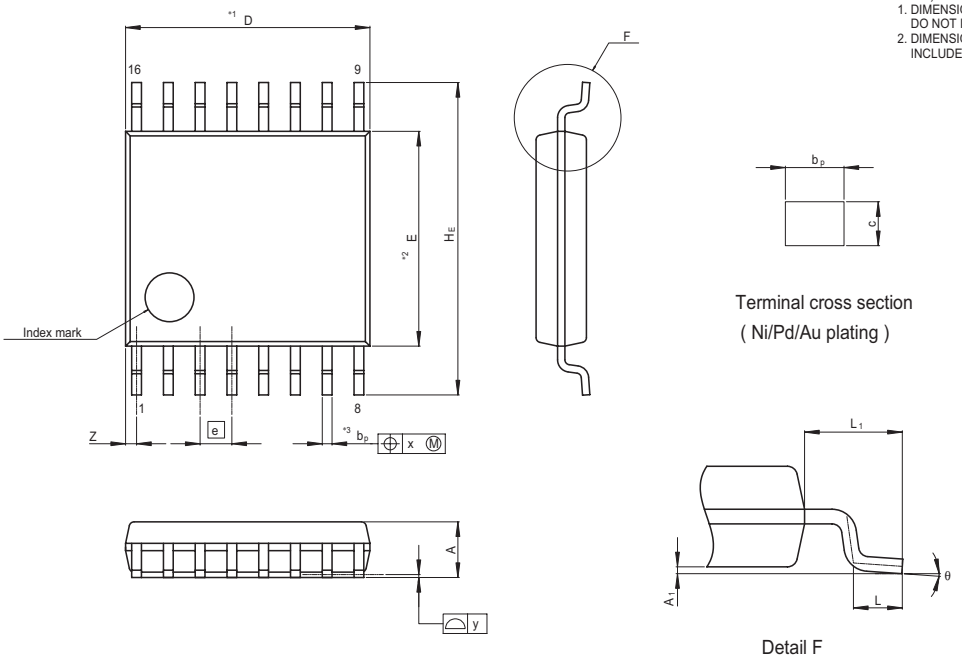
Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP16-6.3x19.2-2.54	PRDP0016AE-B	DP-16FV	1.05g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e 1	——	7.62	——
D	——	19.2	20.32
E	——	6.3	7.4
A	——	——	5.06
A 1	0.51	——	——
b p	0.40	0.48	0.56
b 3	——	1.30	——
c	0.19	0.25	0.31
θ	0°	——	15°
e	2.29	2.54	2.79
Z	——	——	1.12
L	2.54	——	——

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TSSOP16-4.4x5-0.65	PTSP0016JB-A	TTP-16DAV	0.05g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	5.0	5.3
E	——	4.40	——
A 2	——	——	——
A 1	0.03	0.07	0.10
A	——	——	1.10
b p	0.15	0.20	0.25
b 1	——	——	——
c	0.10	0.15	0.20
c 1	——	——	——
θ	0°	——	8°
H E	6.20	6.40	6.60
e	——	0.65	——
x	——	——	0.13
y	——	——	0.10
Z	——	——	0.65
L	0.4	0.5	0.6
L 1	——	1.0	——

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http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

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