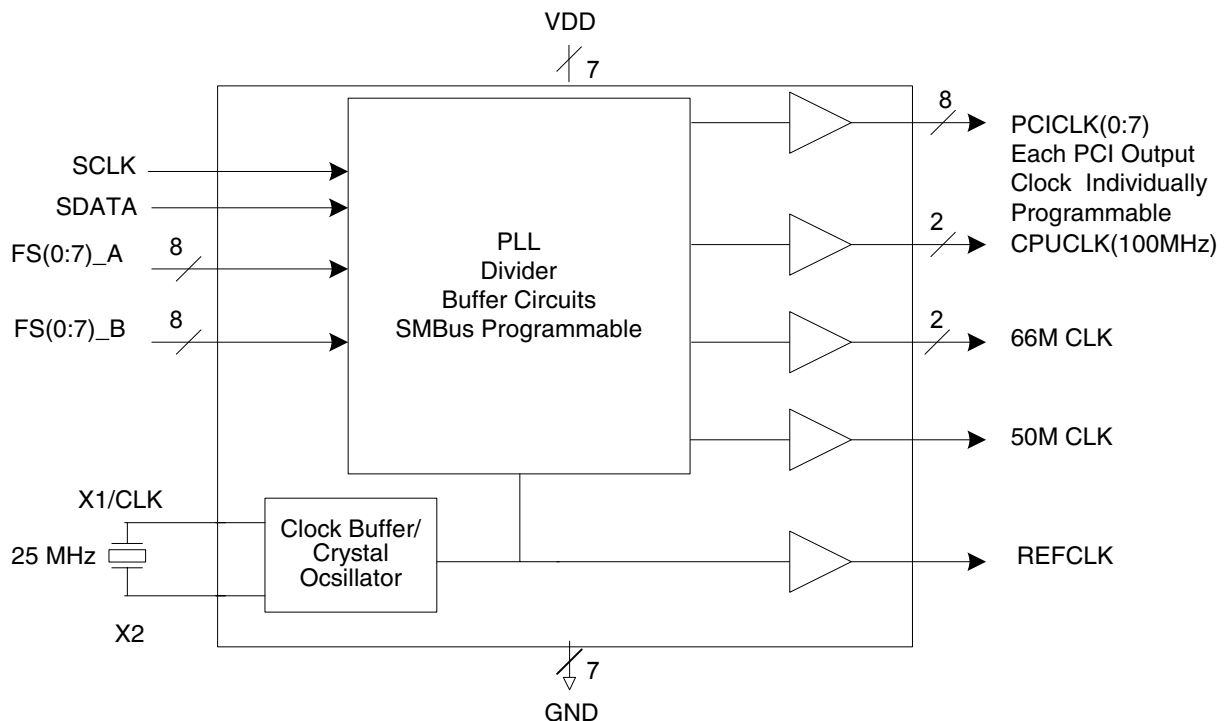


PCI CLOCK GENERATOR
MK1493-01
Description

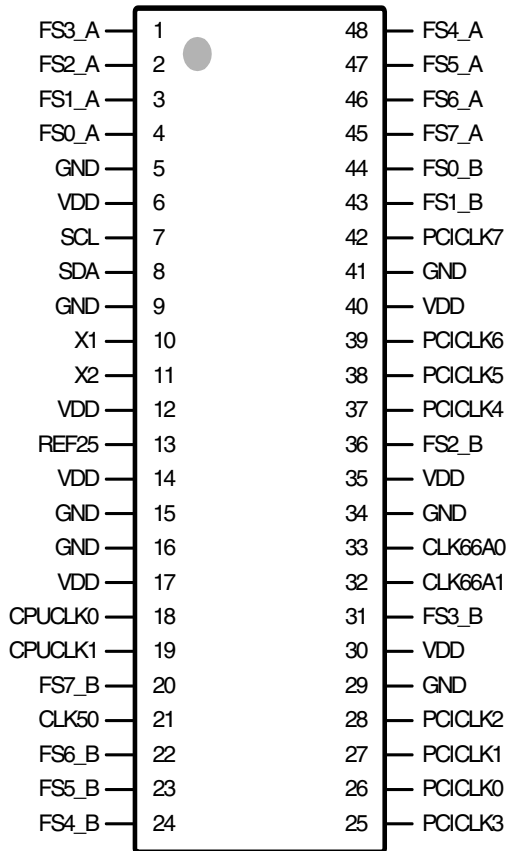
The MK1493-01 is a general purpose clock generator part that provides an integrated clocking solution for PCI/networking applications. It provides 8 individually programmable PCI clocks, 2 CPU clocks, additional fixed PCI clocks and a 25 MHz reference clock for LAN support. This part incorporates ICS's newest clock technology, offering more robust features and functionality. Using a serially programmable SMBus interface, the MK1493-01 can select the output clock frequency, and enabling/disabling each individual output clock.

Features

- 8 PCI clocks at 25, 33, 50, 66.66 MHz individually pin selectable and serial port selectable
- 2 CPU clocks at 100 MHz
- 2 PCI clocks at 66.66 MHz
- 1 PCI clock @ 50 MHz
- 25 MHz reference clock
- SMBus Programming
- Power-up default frequency can be selected through FS inputs
- 25 MHz crystal or clock input required
- PCICLK cycle to cycle jitter <250ps
- CPUCLK cycle to cycle jitter <100ps
- Packaged in 48-pin (240mil) TSSOP Package
- Operating Voltage 3.3V + - 5%

Block Diagram


Pin Assignment



Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|----------|----------|---|
| 1 | FS3_A | Input | Frequency select input pin for PCI CLK3 per per table 1. Pull up resistor. |
| 2 | FS2_A | Input | Frequency select input pin for PCI CLK2 per per table 1. Pull up resistor. |
| 3 | FS1_A | Input | Frequency select input pin for PCI CLK1 per per table 1. Pull up resistor. |
| 4 | FS0_A | Input | Frequency select input pin for PCI CLK0 per per table 1. Pull up resistor. |
| 5 | GND | Power | Connect to ground. |
| 6 | VDD | Power | Connect to +3.3 V. |
| 7 | SCL | Input | Clock pin for SMBus circuitry, 5 V tolerant. |
| 8 | SDA | Input | Data pin for SMBus circuitry, 5 V tolerant. |
| 9 | GND | Power | Connect to ground. |
| 10 | X1/ICLK | Input | Crystal connection/input clock. Connect to a 25 MHz fundamental mode crystal. |
| 11 | X2 | XO | Crystal connection. Connect to a 25 MHz fundamental mode crystal or leave open. |
| 12 | VDD | Power | Connect to +3.3 V. |

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|----------|----------|---|
| 13 | REF25 | Output | Buffered reference output of 25 MHz crystal input. |
| 14 | VDD | Power | Connect to +3.3 V. |
| 15 | GND | Power | Connect to ground. |
| 16 | GND | Power | Connect to ground. |
| 17 | VDD | Power | Connect to +3.3 V. |
| 18 | CPUCLK0 | Output | 100 MHz CPU clock. |
| 19 | CPUCLK1 | Output | 100 MHz CPU clock. |
| 20 | FS7_B | Input | 1 of 4 frequency select input pin for PCI CLK7 per per table 1. Pull-up resistor. |
| 21 | CLK50 | Output | 50 MHz clock output. |
| 22 | FS6_B | Input | Frequency select input pin for PCI CLK6 per per table 1. Pull-up resistor. |
| 23 | FS5_B | Input | Frequency select input pin for PCI CLK5 per per table 1. Pull-up resistor. |
| 24 | FS4_B | Input | Frequency select input pin for PCI CLK4 per per table 1. Pull-up resistor. |
| 25 | PCICLK3 | Output | PCI CLK3. |
| 26 | PCICLK0 | Output | PCI CLK0. |
| 27 | PCICLK1 | Output | PCI CLK1. |
| 28 | PCICLK2 | Output | PCI CLK2. |
| 29 | GND | Power | Connect to ground. |
| 30 | VDD | Power | Connect to +3.3 V. |
| 31 | FS3_B | Input | Frequency select input pin for PCI CLK3 per per table 1. Pull-up resistor. |
| 32 | CLK66A1 | Output | Additional PCI Clock (fixed frequency 66 MHz). |
| 33 | CLK66A0 | Output | Additional PCI Clock (fixed frequency 66 MHz). |
| 34 | GND | Power | Connect to ground. |
| 35 | VDD | Power | Connect to +3.3 V. |
| 36 | FS2_B | Input | Frequency select input pin for PCI CLK2 per per table 1. Pull-up resistor. |
| 37 | PCICLK4 | Output | PCI CLK4. |
| 38 | PCICLK5 | Output | PCI CLK5. |
| 39 | PCICLK6 | Output | PCI CLK6. |
| 40 | VDD | Power | Connect to +3.3 V. |
| 41 | GND | Power | Connect to ground. |
| 42 | PCICLK7 | Output | PCI CLK7. |
| 43 | FS1_B | Input | Frequency select input pin for PCI CLK1 per per table 1. Pull-up resistor. |
| 44 | FS0_B | Input | Frequency select input pin for PCI CLK0 per per table 1. Pull-up resistor. |
| 45 | FS7_A | Input | Frequency select input pin for PCI CLK7 per per table 1. Pull-up resistor. |
| 46 | FS6_A | Input | Frequency select input pin for PCI CLK6 per per table 1. Pull-up resistor. |
| 47 | FS5_A | Input | Frequency select input pin for PCI CLK5 per per table 1. Pull-up resistor. |
| 48 | FS4_A | Input | Frequency select input pin for PCI CLK4 per per table 1. Pull-up resistor. |

Table 1. Frequency Select

| FS(0:7)_B | FS(0:7)_A | PCICLK(0:7) |
|-----------|-----------|-------------|
| 0 | 0 | 25 MHz |
| 0 | 1 | 33.33 MHz |
| 1 | 0 | 50 MHz |
| 1 | 1 | 66.66 MHz |

Power Groups

| Pin Number | | Description |
|------------|--------|-------------------------------|
| VDD | GND | |
| 12 | 9 | Ref, Crystal Osc Power supply |
| 30, 40 | 29, 41 | PCICLK |
| 35 | 34 | PCI 66 clocks |
| 6 | 5 | SCLK |
| 17 | 16 | CPU Clocks(100MHz) |
| 14 | 15 | PLL |

| Index Block Write Operation | | |
|---------------------------------|-----------|----------------------|
| Controller (Host) | | ICS (Slave/Receiver) |
| T | starT bit | |
| Slave Address D2 _(H) | | |
| WR | WRite | |
| Beginning Byte = N | | ACK |
| Data Byte Count = X | | ACK |
| Beginning Byte N | | ACK |
| 0 | | |
| 0 | | 0 |
| 0 | | 0 |
| | | 0 |
| Byte N + X - 1 | | |
| | | ACK |
| P | stoP bit | |

General I²C Serial Interface Information

How to Write:

- Controller (host) sends a start bit
- Controller (host) sends the write address D2_(H)
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1(note 2)**
- ICS clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send a start bit
- Controller (host) sends the write address D2_(H)
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address D3_(H)
- ICS clock will **acknowledge**
- ICS clock will send the data byte count = X
- ICS clock sends Byte N+X-1
- ICS clock sends **Byte 0 through Byte X (if X_(H) was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation | | |
|---------------------------------|--------------|----------------------|
| Controller (Host) | | ICS (Slave/Receiver) |
| T | starT bit | |
| Slave Address D2 _(H) | | |
| WR | WRite | |
| Beginning Byte = N | | ACK |
| | | ACK |
| RT | Repeat starT | |
| Slave Address D3 _(H) | | |
| RD | ReaD | |
| | | ACK |
| | | Data Byte Count=X |
| ACK | | Beginning Byte N |
| ACK | | |
| O | | O |
| O | | O |
| O | | O |
| | | Byte N + X - 1 |
| N | Not | |
| P | stoP bit | |

SMBus Table 2: Read-Back Register

| Byte 0 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|-------|-------------------|---------------------|------|-----------------------|----|-----|
| Bit 7 | - | | RESERVED | | | | 0 |
| Bit 6 | - | FS vs. SMBus prog | HW/SW select | RW | HW | SW | 0 |
| Bit 5 | - | | RESERVED | | | | 0 |
| Bit 4 | - | | RESERVED | | | | 0 |
| Bit 3 | - | | RESERVED | | | | 0 |
| Bit 2 | - | | Frequency Selection | | See Frequency table 3 | | 0 |
| Bit 1 | - | | | 0 | | | |
| Bit 0 | - | | | 0 | | | |

SMBus Table 2: Output Control Register

| Byte 1 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|-------|---------|------------------|------|---------|--------|-----|
| Bit 7 | 40 | PCICLK7 | Output Control | RW | Disable | Enable | 1 |
| Bit 6 | 39 | PCICLK6 | Output Control | RW | Disable | Enable | 1 |
| Bit 5 | 38 | PCICLK5 | Output Control | RW | Disable | Enable | 1 |
| Bit 4 | 37 | PCICLK4 | Output Control | RW | Disable | Enable | 1 |
| Bit 3 | 31 | PCICLK3 | Output Control | RW | Disable | Enable | 1 |
| Bit 2 | 28 | PCICLK2 | Output Control | RW | Disable | Enable | 1 |
| Bit 1 | 27 | PCICLK1 | Output Control | RW | Disable | Enable | 1 |
| Bit 0 | 26 | PCICLK0 | Output Control | RW | Disable | Enable | 1 |

SMBus Table 2: Output Control Register

| Byte 2 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|-------|---------|------------------|------|---------|--------|-----|
| Bit 7 | - | | RESERVED | | | | 0 |
| Bit 6 | - | | RESERVED | | | | 0 |
| Bit 5 | 32 | CLK66A1 | Output Control | RW | Disable | Enable | 0 |
| Bit 4 | 33 | CLK66A0 | Output Control | RW | Disable | Enable | 1 |
| Bit 3 | 12 | REF25 | Output Control | RW | Disable | Enable | 0 |
| Bit 2 | 19 | CPUCLK1 | Output Control | RW | Disable | Enable | 1 |
| Bit 1 | 18 | CPUCLK0 | Output Control | RW | Disable | Enable | 1 |
| Bit 0 | 20 | CLK50 | Output Control | RW | Disable | Enable | 1 |

SMBus Table 2: Frequency Control Register

| Byte 3 | Pin # | Control Function | Type | 0 | 1 | PWD |
|--------|-------|------------------|------|-----------------------|---|-----|
| Bit 7 | 4 | FS0_A | RW | See Frequency Table 1 | | X |
| Bit 6 | 44 | FS0_B | RW | | | X |
| Bit 5 | 3 | FS1_A | RW | | | X |
| Bit 4 | 43 | FS1_B | RW | | | X |
| Bit 3 | 2 | FS2_A | RW | | | X |
| Bit 2 | 36 | FS2_B | RW | | | X |
| Bit 1 | 1 | FS3_A | RW | | | X |
| Bit 0 | 31 | FS3_B | RW | | | X |

SMBus Table 2: Frequency Control Register

| Byte 4 | Pin # | Control Function | Type | 0 | 1 | PWD |
|--------|-------|------------------|------|-----------------------|---|-----|
| Bit 7 | 48 | FS4_A | RW | See Frequency Table 1 | | X |
| Bit 6 | 24 | FS4_B | RW | | | X |
| Bit 5 | 47 | FS5_A | RW | | | X |
| Bit 4 | 23 | FS5_B | RW | | | X |
| Bit 3 | 46 | FS6_A | RW | | | X |
| Bit 2 | 22 | FS6_B | RW | | | X |
| Bit 1 | 45 | FS7_A | RW | | | X |
| Bit 0 | 20 | FS7_B | RW | | | X |

SMBus Table 2: Reserved

| Byte 5 | Pin # | Control Function | Type | 0 | 1 | PWD |
|--------|-------|------------------|------|----------|---|-----|
| Bit 7 | | RESERVED | - | RESERVED | | 0 |
| Bit 6 | | RESERVED | - | | | 0 |
| Bit 5 | | RESERVED | - | | | 0 |
| Bit 4 | | RESERVED | - | | | 0 |
| Bit 3 | | RESERVED | - | | | 0 |
| Bit 2 | | RESERVED | - | | | 0 |
| Bit 1 | | RESERVED | - | | | 0 |
| Bit 0 | | RESERVED | - | | | 0 |

SMBus Table 2: Reserved

| Byte 6 | Pin # | Control Function | Type | 0 | 1 | PWD |
|--------|-------|------------------|------|----------|---|-----|
| Bit 7 | | RESERVED | - | RESERVED | | 0 |
| Bit 6 | | RESERVED | - | | | 0 |
| Bit 5 | | RESERVED | - | | | 0 |
| Bit 4 | | RESERVED | - | | | 0 |
| Bit 3 | | RESERVED | - | | | 1 |
| Bit 2 | | RESERVED | - | | | 0 |
| Bit 1 | | RESERVED | - | | | 0 |
| Bit 0 | | RESERVED | - | | | 0 |

Mbus Table 2: Vendor and Revision ID Register

| Byte 7 | Pin # | Control Function | Type | 0 | 1 | PWD |
|--------|-------|------------------|------|-------------|---|-----|
| Bit 7 | | RID3 | R | REVISION ID | | 0 |
| Bit 6 | | RID2 | R | | | 0 |
| Bit 5 | | RID1 | R | | | 0 |
| Bit 4 | | RID0 | R | | | 0 |
| Bit 3 | | VID3 | R | VENDOR ID | | 0 |
| Bit 2 | | VID2 | R | | | 0 |
| Bit 1 | | VID1 | R | | | 0 |
| Bit 0 | | VID0 | R | | | 1 |

Mbus Table 2: Byte Count Register

| Byte 8 | Pin # | Control Function | Type | 0 | 1 | PWD |
|--------|-------|------------------|------|--|---|-----|
| Bit 7 | | BC7 | RW | Writing to this Register will confirm how many bytes will be read back, default 08=8 bytes | | 0 |
| Bit 6 | | BC6 | RW | | | 0 |
| Bit 5 | | BC5 | RW | | | 0 |
| Bit 4 | | BC4 | RW | | | 0 |
| Bit 3 | | BC3 | RW | | | 1 |
| Bit 2 | | BC2 | RW | | | 0 |
| Bit 1 | | BC1 | RW | | | 0 |
| Bit 0 | | BC0 | RW | | | 0 |

Tabel 3. Frequency Selection through SMBus (Byte 0)

| Bit 2 | Bit 1 | Bit 0 | CPUCLK1,0 (MHz) | CLK50 (MHz) | CLK66A1,A0 (MHz) | PCICLK (MHz) |
|-------|-------|-------|-----------------|---------------|------------------|---------------|
| 0 | 0 | 0 | 100.00 | 50.00 | 66.66 | nominal |
| 0 | 0 | 1 | 105.00 | nominal + 5% | nominal + 5% | nominal + 5% |
| 0 | 1 | 0 | 110.00 | nominal + 10% | nominal + 10% | nominal + 10% |
| 0 | 1 | 1 | 95.00 | nominal - 5% | nominal - 5% | nominal - 5% |
| 1 | 0 | 0 | 90.00 | nominal - 10% | nominal - 10% | nominal - 10% |

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK1493-01. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Recommended Operation Conditions

| Item | Rating |
|-------------------------------|---------------------|
| Supply Voltage, VDD | 5.5 V |
| All Inputs and Outputs | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature | 0 to +70°C |
| Storage Temperature | -65 to +150°C |
| Junction Temperature | 125°C |
| Soldering Temperature | 260°C |

| Parameter | Min. | Typ. | Max. | Units |
|---|-------|------|-------|-------|
| Ambient Operating Temperature | 0 | | +70 | °C |
| Power Supply Voltage (measured in respect to GND) | +3.15 | 3.3 | +3.45 | V |

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V+5%**, Ambient Temperature 0 to +70°C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--------------------------|------------------|---|------|------|------|-------|
| Input High Voltage | V _{IH} | | 2 | | | V |
| Input Low Voltage | V _{IL} | | | | 0.8 | V |
| Input High Current | I _{IH} | V _{IN} =VDD | -5 | | 5 | μA |
| Input Low Current | I _{IL1} | V _{IN} =0V, SDA, SCL inputs with no pull-up resistors. | -5 | | | μA |
| | I _{IL2} | V _{IN} =0V, All other inputs with pull-up resistors | -200 | | | μA |
| Operating Supply Current | I _{DD} | CL = Full load | | 350 | | mA |
| Input Frequency | F _{IN} | Note 3 | | 25 | | MHz |
| Pin Inductance | L _{PIN} | Note 1 | | | 7 | nH |

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|-----------------------------|-------------------|-----------------------------|------|------|------|-------|
| Input Capacitance Note 1 | C _{IN} | Logic inputs | | | 5 | pF |
| | C _{OUT} | Output pin capacitance | | | 6 | pF |
| | C _{INX} | X1 and X2 pins | | | 5 | pF |
| CLK Stabilization | T _{STAB} | From VDD Power-up Note 2 | | | 3 | ms |

Note 1: Guaranteed by design, not 100% tested in production.

Note 2: See timing diagrams for timing requirements.

Note 3: Input frequency should be measured at the REF output pin and tuned to ideal 25 MHz to meet ppm frequency accuracy on PLL outputs.

Electrical Characteristics - CPUCLK

Unless stated otherwise, VDD = 3.3 V+5%, CL=20 pf, Ambient Temperature 0 to +70° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|-----------------------|------------------|---|------|------|------|-------|
| Output Frequency | F _{O1} | | | 100 | | MHz |
| Output Impedance | R _{DSP} | V _O = V _{DD} *(0.5) Note 1 | 12 | | 55 | Ω |
| Output High Voltage | V _{OH} | I _{OH} = -12 mA, Note 1 | 2.4 | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 12 mA, Note 1 | | 0.3 | 0.4 | V |
| Output High Current | I _{OH} | V _{OH@MIN} = 2.0 V, Note 1 | | | -19 | mA |
| Output Low Current | I _{OL} | V _{OL@MAX} = 0.8 V Note 1 | 19 | | | mA |
| Rise Time | t _{r1} | V _{OL} = 0.4 V, V _{OH} = 2.4 V, Note 1 | | 1.2 | 1.7 | ns |
| Fall Time | t _{f1} | V _{OH} = 2.4 V, V _{OL} = 0.8 V, Note 1 | | 1.2 | 1.7 | ns |
| Duty Cycle | dt1 | V _T = 1.5 V | 45 | 50 | 55 | % |
| Output to Output Skew | tsk1 | V _T = 1.5 V | | | 175 | ps |
| Cycle to Cycle Jitter | | V _T = 1.5 V | | 50 | 100 | ps |

Note 1: Guaranteed by design, not 100% tested in production

Electrical Characteristics - CLK50, CLK66A0 & CLK66A1

Unless stated otherwise, VDD = 3.3 V+5%, CL= 20 pf, Ambient Temperature 0 to +70° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---------------------|------------------|---|------|-------|------|-------|
| Output Frequency | F _{O1} | | | 50&66 | | MHz |
| Output Impedance | R _{DSP} | V _O = V _{DD} *(0.5) Note 1 | 12 | | 55 | Ω |
| Output High Voltage | V _{OH} | I _{OH} = -12 mA, Note 1 | 2.4 | | | V |

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|----------|---|------|------|------|-------|
| Output Low Voltage | V_{OL} | $I_{OL} = 12 \text{ mA}$, Note 1 | | 0.3 | 0.4 | V |
| Output High Current | I_{OH} | $V_{OH@MIN} = 2.0 \text{ V}$, Note 1 | | | -19 | mA |
| Output Low Current | I_{OL} | $V_{OH@MAX} = 0.8 \text{ V}$ Note 1 | 19 | | | mA |
| Rise Time | t_{r1} | $V_{OL} = 0.4 \text{ V}$, $V_{OH} = 2.4 \text{ V}$, Note 1 | | 1.2 | 1.7 | ns |
| Fall Time | t_{f1} | $V_{OH} = 2.4 \text{ V}$, $V_{OL} = 0.4 \text{ V}$, Note 1 | | 1.2 | 1.7 | ns |
| Duty Cycle | | $V_T = 1.5 \text{ V}$ | 45 | 50 | 55 | % |
| Output to Output Skew (CLK66A0, A1) | | $V_T = 1.5 \text{ V}$ | | | 175 | ps |
| Cycle to Cycle Jitter | | $V_T = 1.5 \text{ V}$ | | | 250 | ps |

Note 1: Guaranteed by design, not 100% tested in production

Electrical Characteristics - PCICLK

Unless stated otherwise, $V_{DD} = 3.3 \text{ V} \pm 5\%$, $CL = 30 \text{ pf}$, Ambient Temperature 0 to $+70^\circ \text{ C}$

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|-----------------------|-----------|---|------|------|------|----------|
| Output Frequency | F_{O1} | FS0 | | 25 | | MHz |
| Output Impedance | R_{DSP} | $V_O = V_{DD} * (0.5)$ Note 1 | 12 | | 55 | Ω |
| Output High Voltage | V_{OH} | $I_{OH} = -1 \text{ mA}$, Note 1 | 2.4 | | | V |
| Output Low Voltage | V_{OL} | $I_{OL} = 1 \text{ mA}$, Note 1 | | | 0.55 | V |
| Output High Current | I_{OH} | $V_{OH@MIN} = 2.0 \text{ V}$, Note 1 | -33 | | | mA |
| Output Low Current | I_{OL} | $V_{OL@MAX} = 0.8 \text{ V}$ Note 1 | 30 | | | mA |
| Rise Time | t_{r1} | $V_{OL} = 0.4 \text{ V}$, $V_{OH} = 2.4 \text{ V}$, Note 1 | | 1.7 | 2.4 | ns |
| Fall Time | t_{f1} | $V_{OH} = 2.4 \text{ V}$, $V_{OL} = 0.4 \text{ V}$, Note 1 | | 1.7 | 2.4 | ns |
| Duty Cycle | | $V_T = 1.5 \text{ V}$ | 45 | 50 | 55 | % |
| Output to Output Skew | | $V_T = 1.5 \text{ V}$ | | | 250 | ps |
| Cycle to Cycle Jitter | | $V_T = 1.5 \text{ V}$ | | | 250 | ps |

Note 1: Guaranteed by design, not 100% tested in production

Electrical Characteristics - 25 MHz Reference

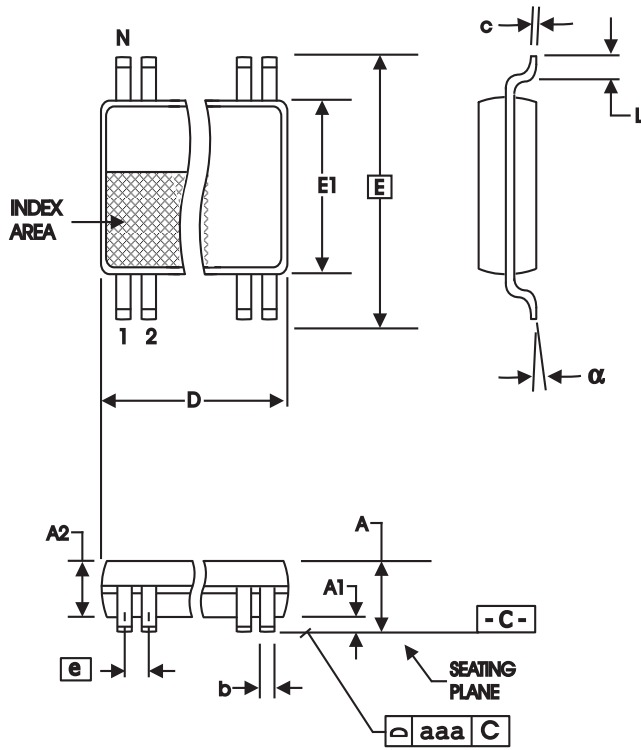
Unless stated otherwise, $V_{DD} = 3.3\text{ V} \pm 5\%$, $C_L = 20\text{ pf}$, $V_{DD} = 3.3\text{ V}$, Ambient Temperature 0 to $+70^\circ\text{ C}$

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|-----------------------|-----------|--|------|------|------|----------|
| Output Frequency | F_{O1} | | | 25 | | MHz |
| Output Impedance | R_{DSP} | $V_O = V_{DD} \cdot (0.5)$ Note 1 | 20 | | 60 | Ω |
| Output High Voltage | V_{OH} | $I_{OH} = -1\text{ mA}$, Note 1 | 2.4 | | | V |
| Output Low Voltage | V_{OL} | $I_{OL} = 1\text{ mA}$, Note 1 | | | 0.4 | V |
| Output High Current | I_{OH} | $V_{OH@MIN} = 1.0\text{ V}$, $V_{OH@MAX} = 3.135\text{ V}$ Note 1 | -29 | | | mA |
| Output Low Current | I_{OL} | $V_{OL@MAX} = 0.8\text{ V}$ Note 1 | 29 | | | mA |
| Rise Time | t_{r1} | $V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.4\text{ V}$, Note 1 | | 1.2 | 1.7 | ns |
| Fall Time | t_{f1} | $V_{OH} = 2.4\text{ V}$, $V_{OL} = 0.4\text{ V}$, Note 1 | | 1.2 | 1.7 | ns |
| Duty Cycle | | $V_T = 1.5\text{ V}$ | 45 | 50 | 55 | % |
| Jitter Cycle to Cycle | | $V_T = 1.5\text{ V}$ | | | 500 | ps |

Note 1: Guaranteed by design, not 100% tested in production

Package Outline and Package Dimensions (48-pin TSSOP, 240 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



| 6.10 mm. Body, 0.40 mm. Pitch TSSOP | | | | |
|-------------------------------------|-------------------|-----------|-------------------|----------|
| | | (240 mil) | | (16 mil) |
| SYMBOL | In Millimeters | | In Inches | |
| | COMMON DIMENSIONS | | COMMON DIMENSIONS | |
| | MIN | MAX | MIN | MAX |
| A | -- | 1.20 | -- | .047 |
| A1 | 0.05 | 0.15 | .002 | .006 |
| A2 | 0.80 | 1.05 | .032 | .041 |
| b | 0.13 | 0.23 | .005 | .009 |
| c | 0.09 | 0.20 | .0035 | .008 |
| D | 12.40 | 12.60 | 0.488 | 0.496 |
| E | 8.10 BASIC | | 0.319 BASIC | |
| E1 | 6.00 | 6.20 | .236 | .244 |
| e | 0.5 BASIC | | 0.02 BASIC | |

Ordering Information

| Part / Order Number | Marking | Shipping packaging | Package | Temperature |
|---------------------|------------|--------------------|--------------|-------------|
| MK1493-01G | MK1493-01G | Tubes | 48-pin TSSOP | 0 to +70° C |
| MK1493-01GTR | MK1493-01G | Tape and Reel | 48-pin TSSOP | 0 to +70° C |

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