TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC7WBD126AFK

# Dual Bus Switch with Level Shift

The TC7WBD126AFK is a low on-resistance, high-speed CMOS 2-bit bus switch. This bus switch allows the connections or disconnections to be made with minimal propagation delay while maintaining Low power dissipation which is the feature of CMOS.

When output enable (OE) is at High level, the switch is on; when at Low level, the switch is off.

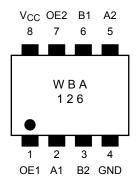
The device is enable to realize the shift of signal level from 5 V to 3.3 V.

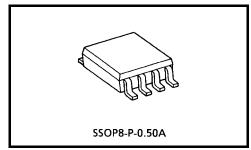
All inputs are equipped with protector circuits to protect the device from static discharge.

### Features

- Operating voltage:  $V_{CC} = 4.5 \sim 5.5 \text{ V}$
- High speed operation:  $t_{pd} = 0.32 \text{ ns} (max)$
- Ultra-low on resistance:  $R_{ON} = 5 \Omega$  (typ.)
- ESD performance: Machine model  $\ge \pm 200 \text{ V}$ Human body model  $\ge \pm 2000 \text{ V}$
- TTL level input (control input)
- Low Power Dissipation: Icc = 10 µA (max.)
- Package: US8

#### Pin Assignment (top view)





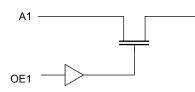
Weight: 0.01 g (typ.)

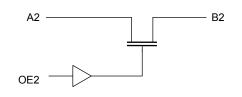
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#### Truth Table

Inputs	Function		
OE	Function		
L	Disconnect		
Н	A port = B port		

#### System Diagram





# Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Power supply range	V <sub>CC</sub>	-0.5~7.0	V
DC input voltage	V <sub>IN</sub>	-0.5~7.0	V
DC switch voltage	VS	-0.5~7.0	V
Input diode current	I <sub>IK</sub>	-50	mA
Continuous channel current	IS	128	mA
Power dissipation	PD	200	mW
DC V <sub>CC</sub> /GND current	I <sub>CC</sub> /I <sub>GND</sub>	±100	mA
Storage temperature	T <sub>stg</sub>	-65~150	°C

B1

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

# **Operating Ranges (Note)**

Characteristics	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	4.5~5.5	V
Input voltage	V <sub>IN</sub>	0~5.5	V
Switch voltage	VS	0~5.5	V
Operating temperature	T <sub>opr</sub>	-40~85	°C
Input rise and fall time	dt/dv	0~10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

#### **Electrical Characteristics**

#### DC Characteristics (Ta = -40~85°C)

Charac	teristics	Symbol	Test Co	ndition	V <sub>CC</sub> (V)	Min	Typ. (Note 1)	Max	Unit	
Input voltage	"H" level	VIH	_	-	4.5~5.5	2.0	—	_	V	
Input voltage	"L" level	V <sub>IL</sub>	_	-	4.5~5.5	_		0.8	v	
Lligh lovel outp	utvaltaga				4.75	2.3	2.8	3.2		
High-level outp	(Note 2)	V <sub>OH</sub>	IOH=-1μA		5.0	2.5	3.0	3.4	V	
	(NOLE 2)		VIS – VCC	$V_{IS} = V_{CC}$		2.7	3.2	3.6		
Input leakage of	current	I <sub>IN</sub>	V <sub>IN</sub> = 0~5.5 V		4.5~5.5		—	±1.0	μA	
Power off leaka	age current	I <sub>OFF</sub>	A, B, OE = 0~5.5 V		0	_	—	±1.0	μA	
Off-STATE lea (switch off)	kage current	I <sub>SZ</sub>	A, B = 0~5.5 V, OE = \	/cc	4.5~5.5	_	_	±1.0	μA	
			V <sub>IS</sub> = 0 V		h. 64 mA	4.5	_	5	9	
					I <sub>IS</sub> = 64 mA	4.75		5	8	
ON resistance	(Note 3)	Bass	VIS = 0 V	ha 20 mA	4.5	_	5	9	Ω	
		R <sub>ON</sub>		I <sub>IS</sub> = 30 mA	4.75	_	5	8	52	
			V 0.0.V I 15 m	A	4.5	_	35	65		
			$V_{IS} = 2.3 \text{ V}, I_{IS} = 15 \text{ m}$	A	4.75	_	35	50		
Quiescent supp	oly current	ICC	VIN = VCC or GND,I <sub>OUT</sub> = 0		5.5	_	_	10	μA	
Increase in I <sub>CC</sub>	; per input	$\Delta I_{CC}$	V <sub>IN</sub> = 3.4 V (one input)		5.5	_		2.5	mA	

Note 1: Typical values are at  $V_{CC} = 5 V$ ,  $Ta = 25^{\circ}C$ .

- Note 2: It recommends that this device uses Pull-up resistance when adding and using resistance for an output terminal. Since it couses to drop a VOH voltage level when using Pull-down resistance for an output terminal.
- Note 3: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

# AC Characteristics (Ta = -40~85°C)

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Min	Max	Unit
Propagation delay time	t <sub>pLH</sub>	Figure 1, Figure 2 (Note)	4.5		0.32	ns
(bus to bus)	t <sub>pHL</sub>		4.0		0.02	110
Output enable time	t <sub>pZL</sub>	Figure 1, Figure 3	4.5		4.5	ns
	t <sub>pZH</sub>		4.0		4.5	113
Output disable time	t <sub>pLZ</sub>	Figure 1, Figure 3	4.5		5.5	ns
	t <sub>pHZ</sub>		4.5		5.5	115

Note: The propagation delay time is calculated by the RC (on-resistance and load capacitance) time constant.

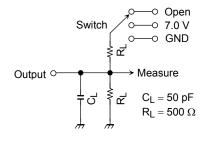
#### **Capacitive Characteristics (Ta = 25°C)**

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Тур.	Unit
Control pin input capacitance	C <sub>IN</sub>	(Note)	5.0	3	pF
Switch terminal capacitance	C <sub>I/O</sub>	OE = V <sub>CC</sub> (Note)	5.0	10	pF

Note: This parameter is guaranteed by design.

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# **AC Test Circuit**



Parameter	Switch
t <sub>pLH</sub> , t <sub>pHL</sub>	Open
t <sub>pLZ</sub> , t <sub>pZL</sub>	7.0 V
t <sub>pHZ</sub> , t <sub>pZH</sub>	GND



### AC Waveform

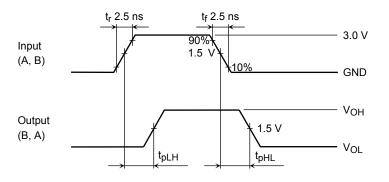
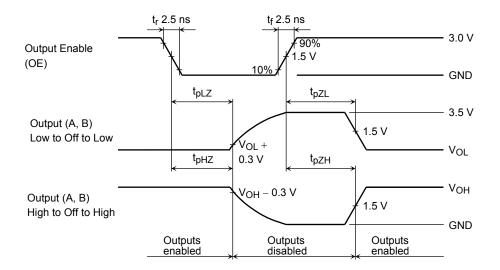
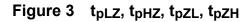


Figure 2 t<sub>pLH</sub>, t<sub>pHL</sub>





# V<sub>OH</sub> – V<sub>CC</sub> Characteristics (typ.)

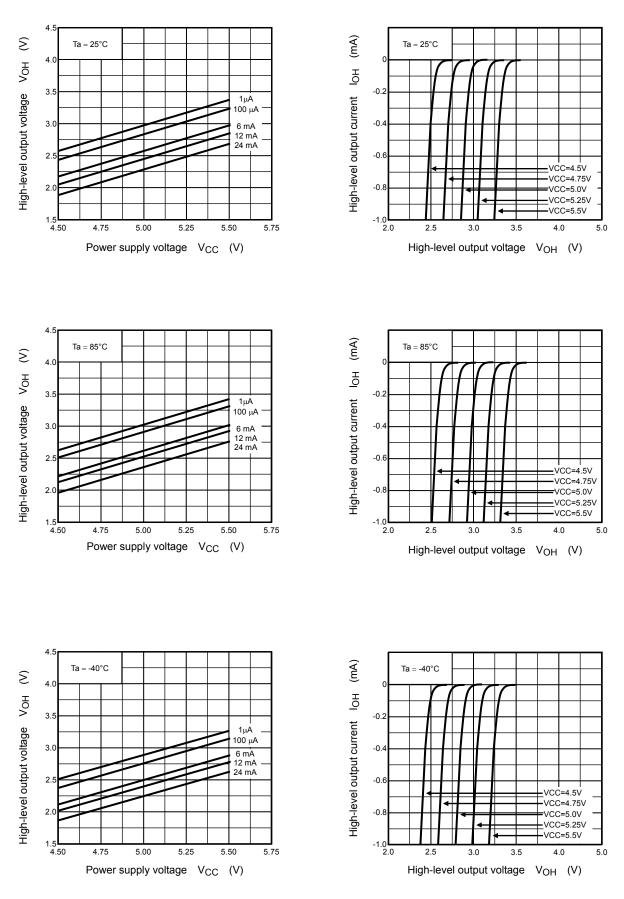


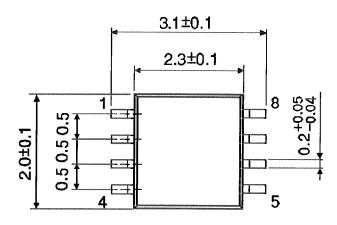
Figure 4

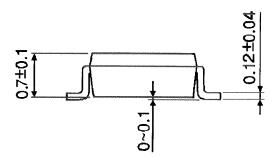
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# **Package Dimensions**

SSOP8-P-0.50A

Unit : mm





Weight: 0.01 g (typ.)

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