Integrated Circuit Systems, Inc.

ICS93V857

Preliminary Product Preview

DDR Phase Lock Loop Clock Driver

Recommended Application:

DDR Memory Modules

Product Description/Features:

- Low skew, low jitter PLL clock driver
- 1 to 10 differential clock distribution
- Feedback pins for input to output synchronization
- PD# for power management
- Spread Spectrum tolerant inputs

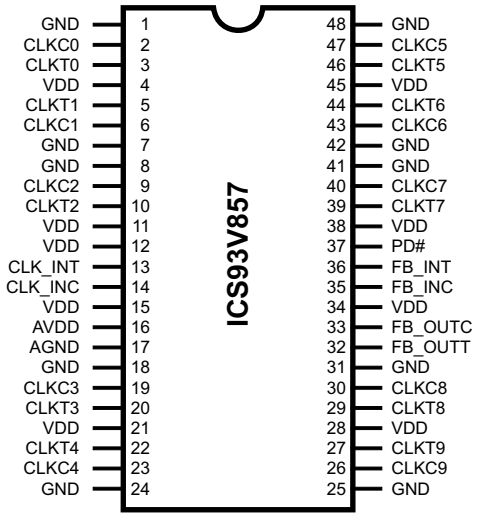
Specifications:

- Meet JEDEC standard #82 for registered DDR clock driver.

Switching Characteristics:

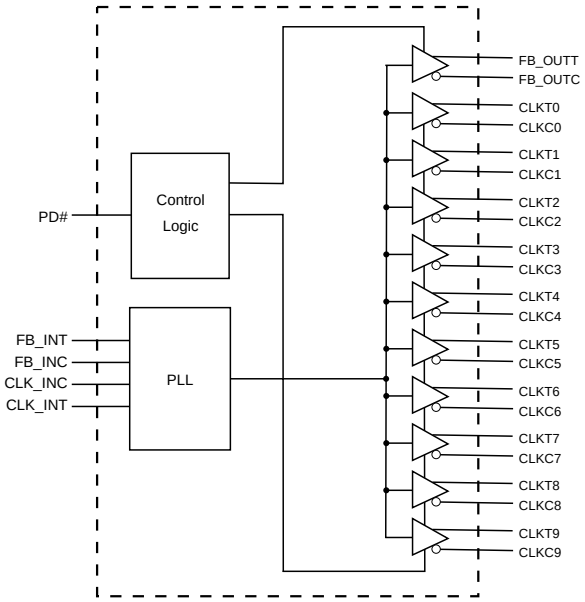
- PEAK - PEAK jitter (66MHz): <120ps
- PEAK - PEAK jitter (>100MHz): <75ps
- CYCLE - CYCLE jitter (66MHz):<120ps
- CYCLE - CYCLE jitter (>100MHz):<65ps
- OUTPUT - OUTPUT skew: <100ps
- Output Rise and Fall Time: 650ps - 950ps
- DUTY CYCLE: 49.5% - 50.5%

Pin Configuration



48-Pin TSSOP

Block Diagram



Functionality

INPUTS				OUTPUTS				PLL State
AVDD	PD#	CLK_INT	CLK_INC	CLKT	CLKC	FB_OUTT	FB_OUTC	
GND	H	L	H	L	H	L	H	Bypassed/off
GND	H	H	L	H	L	H	L	Bypassed/off
2.5V (nom)	L	L	H	Z	Z	Z	Z	off
2.5V (nom)	L	H	L	Z	Z	Z	Z	off
2.5V (nom)	H	L	H	L	H	L	H	on
2.5V (nom)	H	H	L	H	L	H	L	on
2.5V (nom)	X	<20MHz)(1)		Z	Z	Z	Z	off

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
4, 11, 12, 15, 21, 28, 34, 38, 45,	VDD	PWR	Power supply 2.5V
1, 7, 8, 18, 24, 25, 31, 41, 42, 48	GND	PWR	Ground
16	AVDD	PWR	Analog power supply, 2.5V
17	AGND	PWR	Analog ground.
27, 29, 39, 44, 46, 22, 20, 10, 5, 3	CLKT(9:0)	OUT	"True" Clock of differential pair outputs.
26, 30, 40, 43, 47, 23, 19, 9, 6, 2	CLKC(9:0)	OUT	"Complementory" clocks of differential pair outputs.
14	CLK_INC	IN	"Complementory" reference clock input
13	CLK_INT	IN	"True" reference clock input
33	FB_OUTC	OUT	"Complementory" Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INC.
32	FB_OUTT	OUT	"True" " Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INT.
36	FB_INT	IN	"True" Feedback input, provides feedback signal to the internal PLL for synchronization with CLK_INT to eliminate phase error.
35	FB_INC	IN	"Complementory" Feedback input, provides signal to the internal PLL for synchronization with CLK_INC to eliminate phase error.
37	PD#	IN	Power Down. LVCMOS input

Absolute Maximum Ratings

Supply Voltage (VDD & AVDD) . . . . . -0.5V to 4.6V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +85°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 85C; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Current	I_{IH}	VI = VDD or GND	5			µA
Input Low Current	I_{IL}	VI = VDD or GND			5	µA
Operating Supply Current	$I_{DD2.5}$	CL = 0pf				mA
	I_{DDPD}	CL = 0pf			100	µA
Output High Current	I_{OH}	VDD = 2.3V, V_{OUT} = 1V	-18	-32		mA
Output Low Current	I_{OL}	VDD = 2.3V, V_{OUT} = 1.2V	26	35		mA
High Impedance Output Current	I_{OZ}	VDD=2.7V, Vout=VDD or GND			±10	µA
Input Clamp Voltage	V_{IK}	VDDQ = 2.3V Iin = -18mA			-1.2	V
High-level output voltage	V_{OH}	VDD = min to max, IOH = -1 mA	VDDQ -0.1			V
		VDDQ = 2.3V, IOH = -12 mA	1.7			V
Low-level output voltage	V_{OL}	VDD = min to max I_{OL}=1 mA			0.1	V
		VDDQ = 2.3V IOH=12 mA			0.6	V
Input Capacitance[1]	C_{IN}	VI = GND or VDD		3		pF
Output Capacitance[1]	C_{OUT}	VOUT = GND or VDD		3		pF
Output differential-pair crossing voltage	V_{OC}		(V_{DD}/2) -0.2		(V_{DD}/2) +0.2	V

[1]Guaranteed by design, not 100% tested in production.

Recommended Operating Condition (see note1)

T_A = 0 - 85C; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DDQ}, A_{VDD}		2.3		2.7	V
Low level input voltage	V_{IL}	CLKT, CLKC, FBINC			V_{DDQ}/2 -0.18	V
		PD#	-0.3		0.7	V
High level input voltage	V_{IH}	CLKT, CLKC, FBINC	V_{DDQ}/2 +018			V
		PD#	1.7		V_{DDQ} +0.6	V
DC input signal voltage (note 2)			-0.3		V_{DDQ}	V
Differential input signal voltage (note 3)	V_{ID}	DC - CLKT, FBINT	0.36		V_{DDQ} +0.6	V
		AC - CLKT, FBINT	0.7		V_{DDQ} +0.6	V
Output differential cross-voltage (note 4)	V_{OX}		V_{DDQ}/2 -0.2		V_{DDQ}/2 +0.2	V
Input differential cross-voltage (note 4)	V_{IX}		V_{DDQ}/2 -0.2		V_{DDQ}/2 +0.2	V
High level output current	I_{OH}				-12	mA
Low level output current	I_{OL}				12	mA
Input slew rate	S_R		1		4	V/ns
Operating free-air temperature	T_A		0		85	°C

Notes:

1. Unused inputs must be held high or low to prevent them from floating.
2. DC input signal voltage specifies the allowable DC execution of differential input.
3. Differential inputs signal voltages specifies the differential voltage [VTR-VCP] required for switching, where VT is the true input level and VCP is the complementary input level.
4. Differential cross-point voltage is expected to track variations of VCC and is the voltage at which the differential signal must be crossing.

Timing Requirements

T_A = 0 - 85C; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Operating clock frequency	$freq_{op}$		66	170	MHz
Input clock duty cycle	d_{tin}		40	60	%
CLK stabilization	T_{STAB}	from VDD = 3.3V to 1% target freq.		100	µs

Switching Characteristics

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Low-to high level propagation delay time	t_{PLH}[1]	CLK_IN to any output		3.5		ns
High-to low level propagation delay time	t_{PLL}[1]	CLK_IN to any output		3.5		ns
Output enable time	t_{EN}	PD# to any output		3		ns
Output disable time	tdis	PD# to any output		3		ns
Jitter period	$T_{jit\ (per)}$	66MHz				ps
		100/125/133/167MHz	-75		75	ps
Half-period jitter	t(jit_hper)	100/133/167MHz	-100		100	
Input clock slew rate	t(sir_I)		1		4	
Output clock slew reate	t(sl_o)		1		4	
Cycle to Cycle Jitter1	T_{cyc}-T_{cyc}	66MHz				ps
		100/125/133/167MHz			75	ps
Phase error	$t_{(phase\ error)}$		-50		50	ps
Output to Output Skew	T_{skew}				100	ps
Pulse skew	T_{skewp}				100	ps
Duty cycle	D_C[2]	66MHz to 100MHz	49.5		50.5	%
		101MHz to 167MHz	49		51	%
Rise Time, Fall Time	tr, tf	Load = 120Ω/16pF	650	800	950	ps

Notes:

1. Refers to transition on noninverting output in PLL bypass mode.
2. While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle=t_{wH}/t_c, were the cycle (t_c) decreases as the frequency goes up.

Parameter Measurement Information

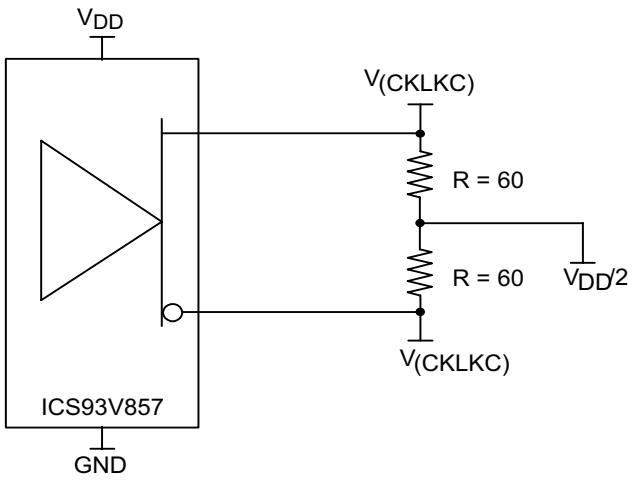
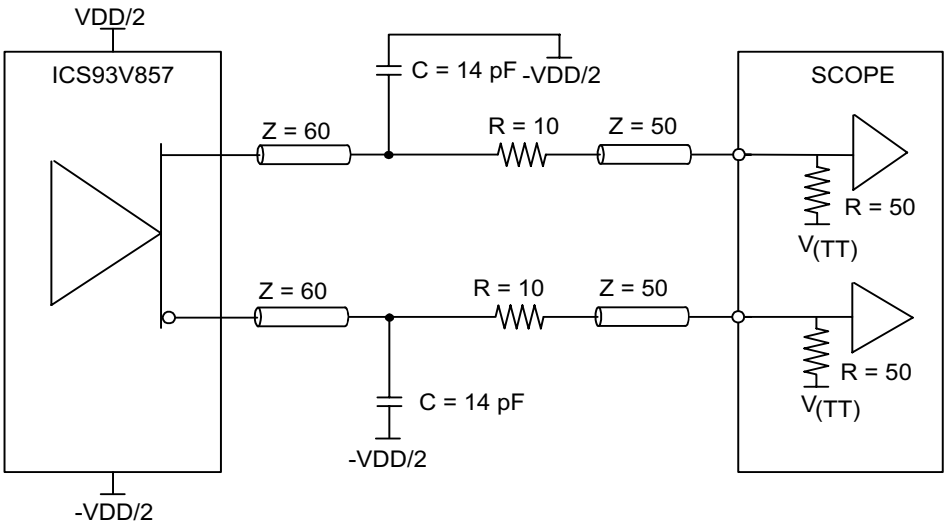
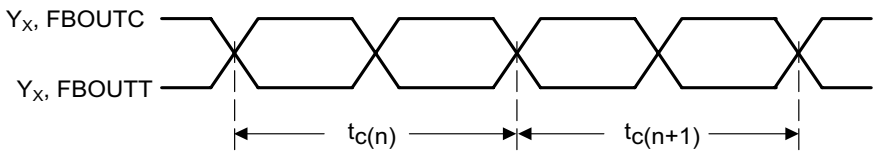


Figure 1. IBIS Model Output Load



NOTE: $V_{(TT)}$ = GND

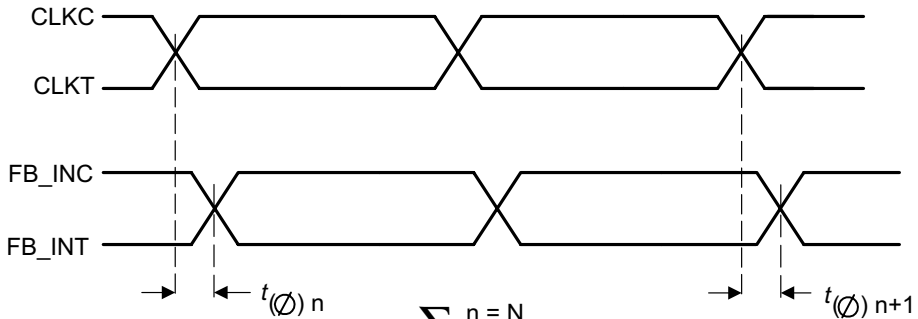
Figure 2. Output Load Test Circuit



$t_{jit(cc)} = t_{c(n)} \pm t_{c(n+1)}$

Figure 3. Cycle-to-Cycle Jitter

Parameter Measurement Information



$$t_{(\varnothing)} = \frac{\sum_{1}^{n=N} t_{(\varnothing)\ n}}{N}$$

(N is a large number of samples)

Figure 4. Static Phase Offset

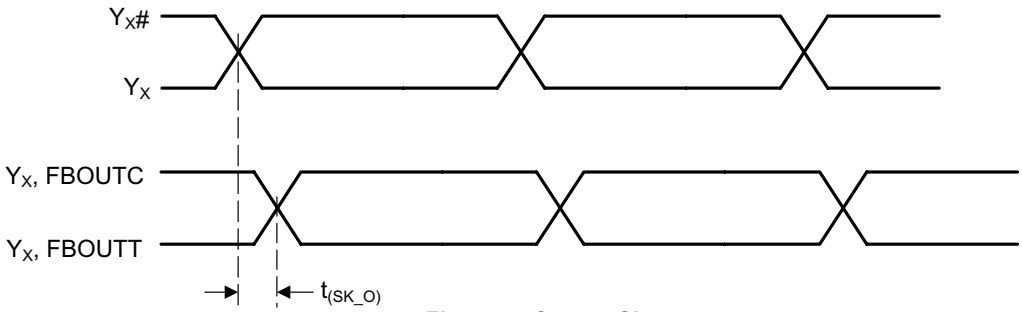
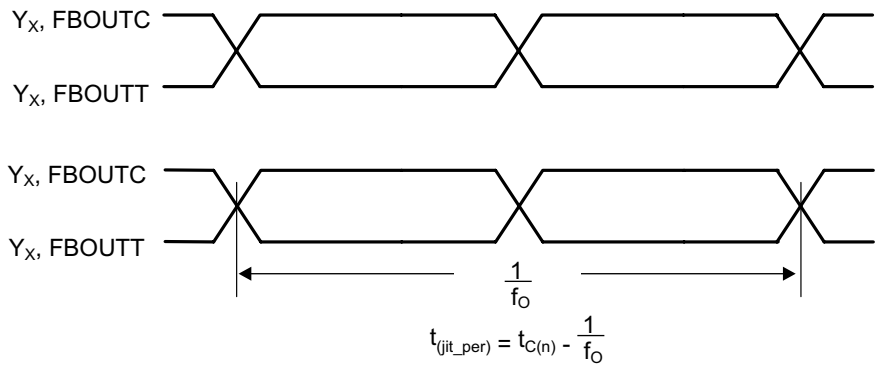


Figure 5. Output Skew



$$t_{(jit\_per)} = t_{C(n)} - \frac{1}{f_O}$$

Figure 6. Period Jitter

Parameter Measurement Information

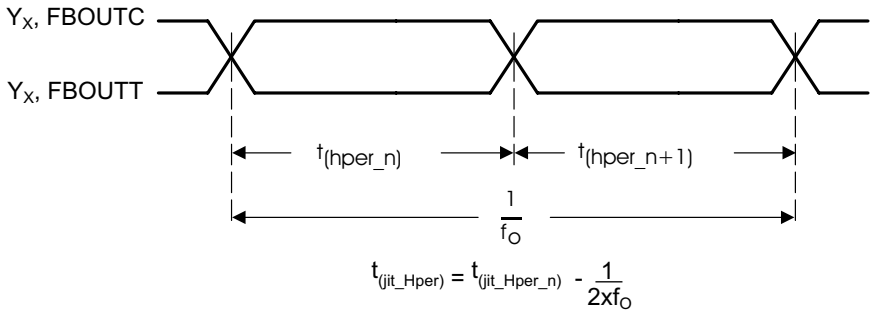
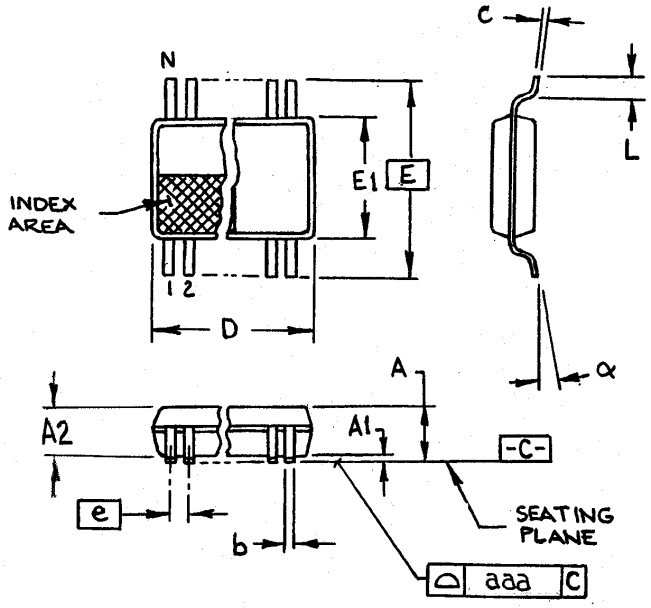


Figure 7. Half-Period Jitter

Figure 8. Input and Output Slew Rates



6.10 mm. Body, 0.50 mm. pitch TSSOP
(240 mil) (0.020 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	-	1.20	-	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.30
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	-	0.10	-	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	12.40	12.60	.488	.496

MO-153 JEDEC 7/6/00 Rev B
Doc.# 10-0039

Ordering Information

ICS93V857yGT

Example:

ICS XXXX y G - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  G=TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device

93V857B (DDR PLL)

Description

Market Group
DIMM
Additional Info

Related Orderable Parts

Attributes	93V857BG-025LF	93V857BG-025LFT
Package	TSSOP 48 (PAG48)	TSSOP 48 (PAG48)
Speed	NA	NA
Temperature	C	C
Voltage	3.3 V	3.3 V
Status	Active	Active
Sample	No	No
Minimum Order Quantity	760	1000
Factory Order Increment	38	1000

Related Documents

Type	Title	Size	Revision Date
Datasheet	93V857 Datasheet	169 KB	06/01/2007
Product Change Notice	PCN#: TB-0510-05 New Shipping Tube for TSSOP/TVSOP/TSSOP Exposed	202 KB	12/13/2005