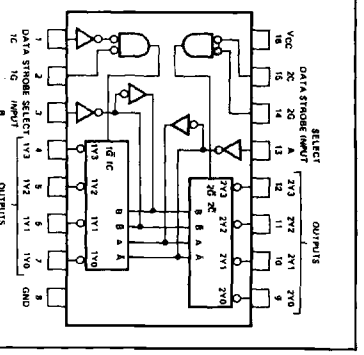
SPEED/PACKAGE AVAILABILITY

54 F,W 74 B,F

PIN CONFIGURATION

B,F,W PACKAGE



TRUTH TABLE

2-LINE TO 4-LINE DECODER							
INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

1-LINE TO 4-LINE DEMULTIPLEXER							
INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

†C = inputs 1C and 2C connected together
‡G = inputs 1G and 2G connected together

3-LINE TO 8-LINE DECODER TO 1-LINE TO 8-LINE DEMULTIPLEXER										
INPUTS				OUTPUTS						
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

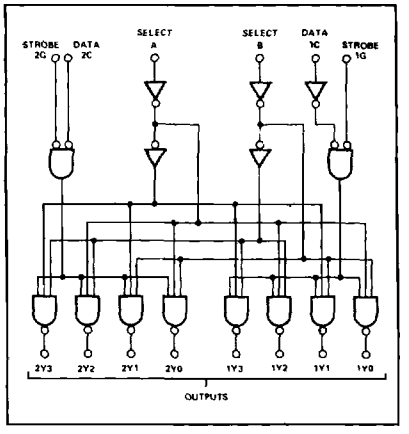
†C=inputs 1C and 2C connected together
‡G=inputs 1G and 2G connected together

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L=15pF R_L=400Ω				
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	LEVELS OF LOGIC	UNIT
Propagation delay time							
t_{PLH} Low-to-high	A,B,2C, 1G,2G	Y		13	20	2	ns
t_{PHL} High-to-low				18	27		
t_{PLH} Low-to-high	A,B	Y		21	32	3	
t_{PHL} High-to-low				21	32		
t_{PLH} Low-to-high	1C	Y		16	24	3	
t_{PHL} High-to-low				20	30		

Load circuit and typical waveforms are shown at the front of section.

LOGIC DIAGRAM



LOGIC