

DATA SHEET

74LVT14

3.3V Hex inverter Schmitt trigger

Product specification

1996 Aug 28

IC24 Data Handbook

3.3V Hex inverter Schmitt trigger

74LVT14

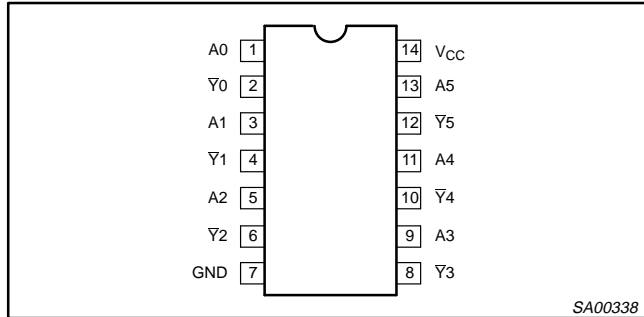
DESCRIPTION

The 74LVT14 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V. They are capable of transforming slowly changing input signals into sharply defined, jitter free output signals. In addition, they have greater noise margin than conventional inverters. Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive-going and negative-going input threshold (typically 600mV) is determined internally by resistor ratios and is insensitive to temperature and supply voltage variations.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}C$; $GND = 0V$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to \bar{Y}_n	$C_L = 50pF$; $V_{CC} = 3.3V$	3.2 3.0	ns
C_{IN}	Input capacitance	$V_I = 0V$ or 3.0V	3	pF
I_{CCL}	Total supply current	Outputs low; $V_{CC} = 3.6V$	1.5	mA

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	A_n	Data inputs
2, 4, 6, 8, 10, 12	\bar{Y}_n	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	-40°C to +85°C	74LVT14 D	74LVT14 D	SOT108-1
14-Pin Plastic SSOP	-40°C to +85°C	74LVT14 DB	74LVT14 DB	SOT337-1
14-Pin Plastic TSSOP	-40°C to +85°C	74LVT14 PW	74LVT14 PWDH	SOT402-1

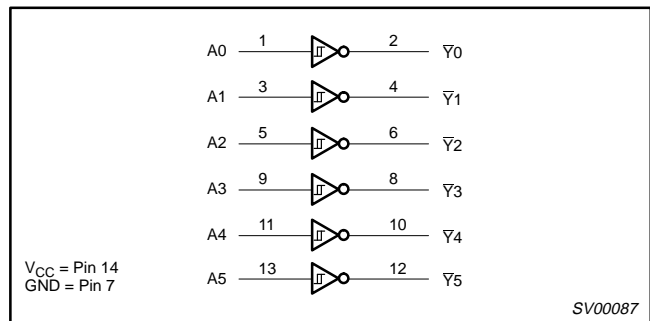
FUNCTION TABLE

INPUTS	OUTPUT
D_n	Q_n
L	H
H	L

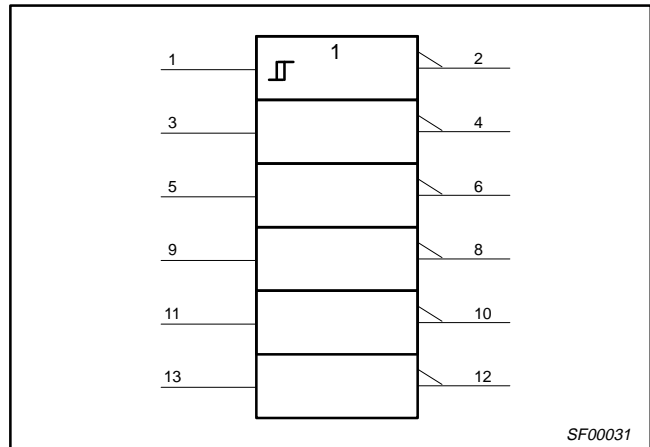
NOTES:

H = High voltage level
L = Low voltage level

LOGIC DIAGRAM



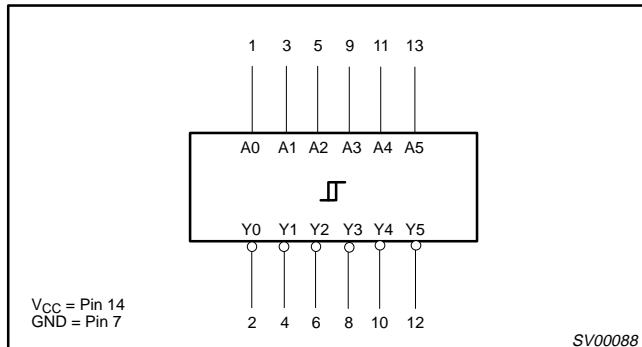
IEC/IEEE SYMBOL



3.3V Hex inverter Schmitt trigger

74LVT14

LOGIC SYMBOL

ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage ³		-0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage ³	Output in Off or High state	-0.5 to +7.0	V
I_{OUT}	DC output current	Output in High state	-32	mA
		Output in Low state	64	
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		-20	mA
I_{OL}	Low-level output current		32	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

3.3V Hex inverter Schmitt trigger

74LVT14

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions
 Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
V_{T+}	Positive-going threshold	$V_{CC} = 3.3V$	1.5	1.7	2.0	V
V_{T-}	Negative-going threshold	$V_{CC} = 3.3V$	0.9	1.1	1.3	V
ΔV_T	Hysteresis	$V_{CC} = 3.3V$	0.4	0.6		V
V_{IK}	Input clamp voltage	$V_{CC} = 2.7V; I_{IK} = -18mA$			-1.2	V
V_{OH}	High-level output voltage	$V_{CC} = 2.7$ to $3.6V; I_{OH} = -100\mu A$	$V_{CC}-0.2$			V
		$V_{CC} = 2.7V; I_{OH} = -6mA$	2.4			
		$V_{CC} = 3.0V; I_{OH} = -20mA$	2.0			
V_{OL}	Low-level output voltage	$V_{CC} = 2.7V; I_{OL} = 100\mu A$			0.2	V
		$V_{CC} = 2.7V; I_{OL} = 24mA$			0.5	
		$V_{CC} = 3.0V; I_{OL} = 32mA$			0.5	
I_I	Input leakage current	$V_{CC} = 0$ or $3.6V; V_I = 5.5V$			10	μA
		$V_{CC} = 3.6V; V_I = V_{CC}$ or GND			± 1	
I_{OFF}	Output off current	$V_{CC} = 0V; V_I$ or $V_O = 0$ to $4.5V$			± 100	μA
I_{CCH}	Quiescent supply current	$V_{CC} = 3.6V; \text{Outputs High, } V_I = \text{GND or } V_{CC}, I_O = 0$			0.02	mA
I_{CCL}		$V_{CC} = 3.6V; \text{Outputs Low, } V_I = \text{GND or } V_{CC}, I_O = 0$		1.5	3	
ΔI_{CC}	Additional supply current per input pin ²	$V_{CC} = 3V$ to $3.6V; \text{One input at } V_{CC}-0.6V, \text{Other inputs at } V_{CC}$ or GND			0.2	μA
C_I	Input capacitance	$V_I = 3V$ or 0		3		pF

NOTES:

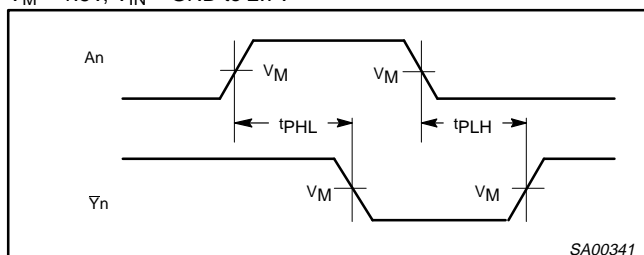
1. All typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25^\circ C$.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS				UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$	
			MIN	TYP	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay An to \bar{Y}_n	Waveform 1	1.0 1.0	3.8 3.2	5.7 4.5	6.9 4.1	ns

AC WAVEFORMS

$V_M = 1.5V, V_{IN} = \text{GND to } 2.7V$

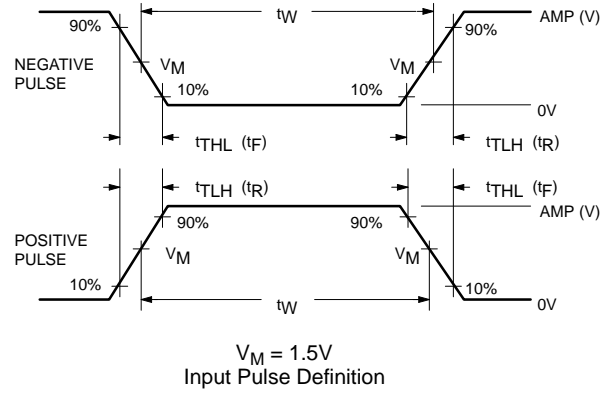
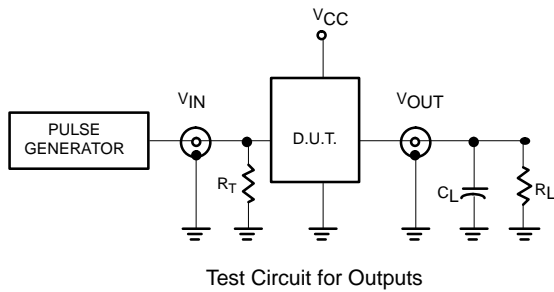


Waveform 1. Propagation delay for inverting outputs

3.3V Hex inverter Schmitt trigger

74LVT14

TEST CIRCUIT AND WAVEFORMS



DEFINITIONS

- R_L = Load resistor; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_w	t_R	t_F
74LVT	2.7V	$\leq 10MHz$	500ns	$\leq 2.5ns$	$\leq 2.5ns$

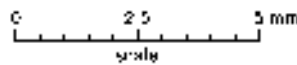
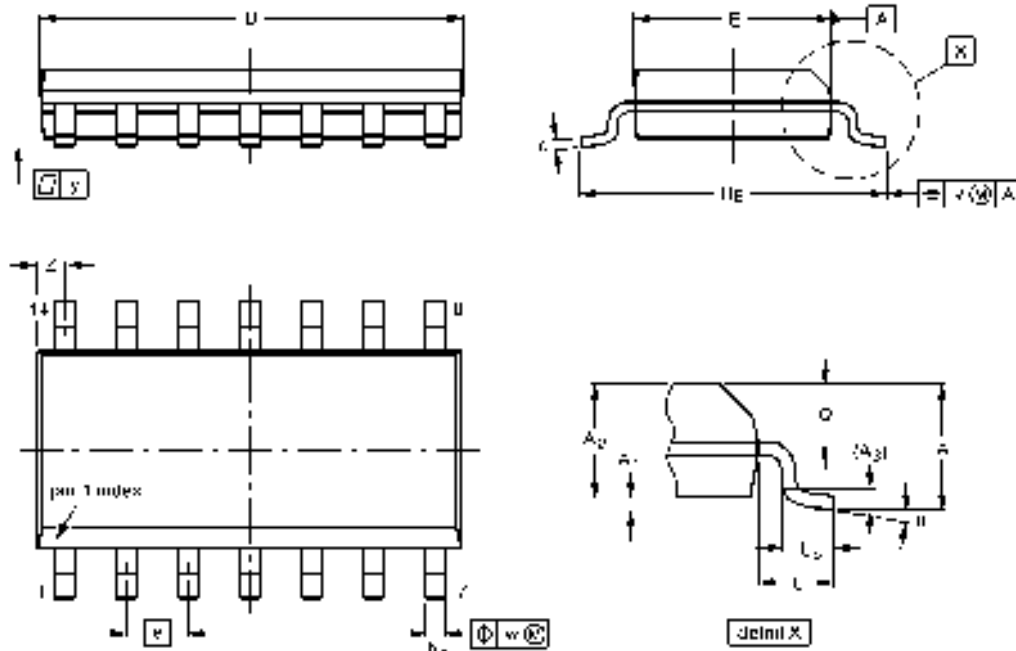
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3.3V Hex inverter Schmitt trigger

74LVT14

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	e	Ø ⁽¹⁾	ε ⁽¹⁾	φ	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	⋮
mm	1.75	0.25 0.10	1.45 1.25	0.20	0.45 0.30	0.25 0.19	8.75 8.00	4.0 3.0	1.27	5.2 5.0	1.6	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	⋮
inches	0.069	0.0098 0.0039	0.057 0.049	0.008	0.018 0.014	0.0099 0.0075	0.34 0.31	0.16 0.12	0.050	0.21 0.20	0.063	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	B ⁽²⁾ D ⁽²⁾

Note

1 Plastic or metal protrusions of 0.15 mm maximum per side are not included

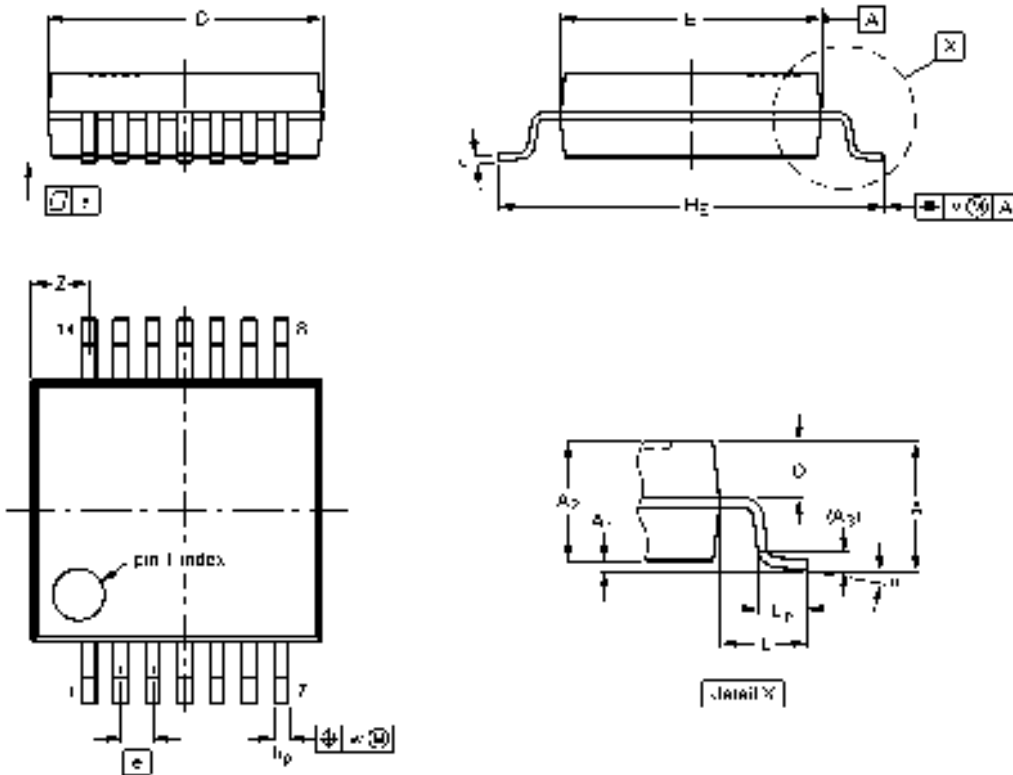
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT108-1	076E060	MS-012AB			94-08-19 95-01-23

3.3V Hex inverter Schmitt trigger

74LVT14

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	D ⁽¹⁾	e	H ₂	L	L _p	Q	y	w	y	z ⁽¹⁾	r
mm	2.0	0.71 0.75	1.80 1.05	0.20	0.50 0.25	0.20 0.09	6.4 0.0	5.4 5.2	0.65	7.0 7.8	1.25	1.00 0.82	0.9 0.7	0.2	0.12	0.1	1.4 0.9	0° 0°

Note

1 Plastic or metal protrusions of 0.25 mm maximum per side are not included

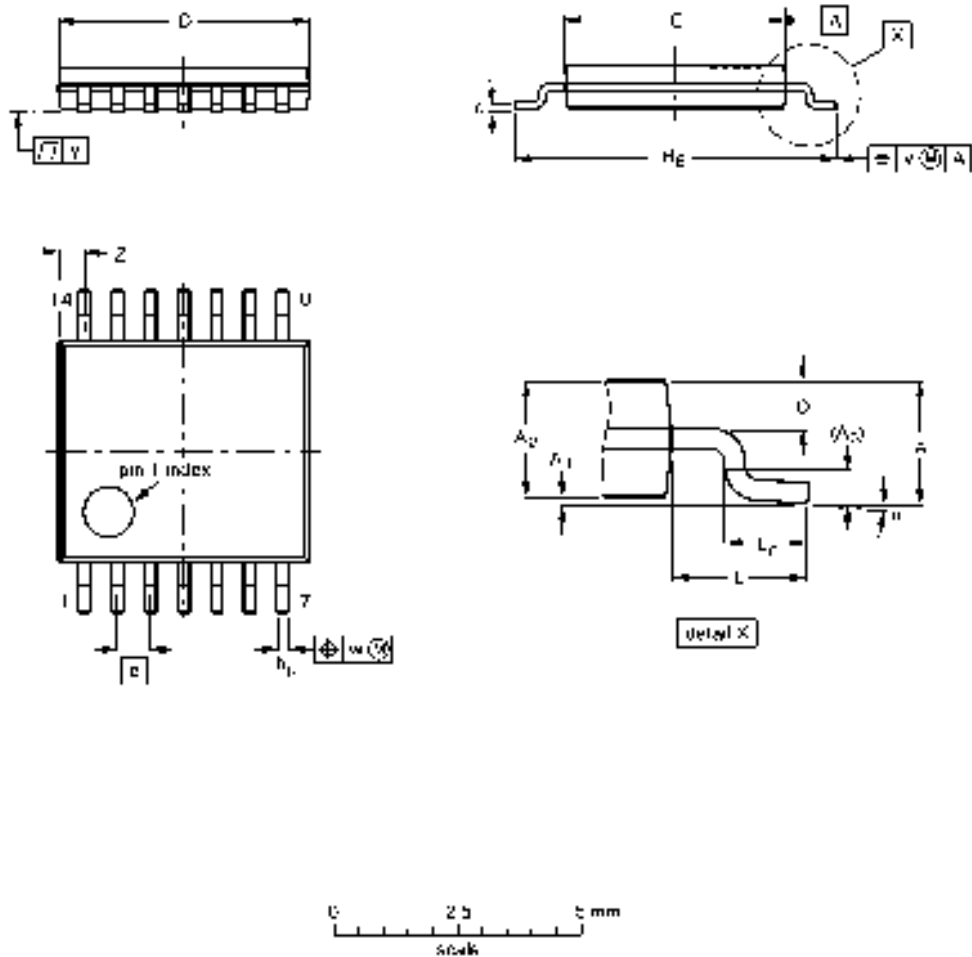
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT337-1		MO-150AB			95-85-94 96-01-19

3.3V Hex inverter Schmitt trigger

74LVT14

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	e ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	u
mm	1.10	0.15 0.75	0.05 0.00	0.25	0.50 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.55	6.6 6.2	1.0	0.75 0.53	0.4 0.3	0.2	0.13	0.1	0.72 0.30	0° 0°

Notes

- 1 Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2 Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-150				94-07-12 95-11-01

3.3V Hex inverter Schmitt trigger

74LVT14

NOTES

3.3V Hex inverter Schmitt trigger

74LVT14

DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
<i>Product Specification</i>	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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General description

The 74LVT14 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V. They are capable of transforming slowly changing input signals into sharply defined, jitter free output signals. In addition, they have greater noise margin than conventional inverters. Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive-going and negative-going input threshold (typically 600mV) is determined internally by resistor ratios and is insensitive to temperature and supply voltage variations.

Applications

- [AN2022: The Behavior Of Integrated Bus Hold Circuits](#) (date 01-Mar-96)
- [AN203_2: Test Fixtures for High Speed Logic](#) (date 02-Apr-98)
- [AN2301: Simulation Support for Philips' Advanced BiCMOS Products](#)
- [AN243: LVT \(Low Voltage Technology\) and ALVT \(Advanced LVT\)](#) (date 01-Jan-98)
- [AN246: Transmission Lines and Terminations with Philips Advanced Logic Families](#)

Datasheet

<u>Type number</u>	<u>Title</u>	<u>Publication release date</u>	<u>Datasheet status</u>	<u>Page count</u>	<u>File size (kB)</u>	<u>Datasheet</u>
74LVT14	3.3V Hex inverter Schmitt trigger	8/28/1996	Product specification	10	70	Download


❑ Blockdiagram(s)

Block diagram of
74LVT14D

❑ Parametrics

Type number	Package	Description	Propagation Delay(ns)	Voltage	No. of Pins	Power Dissipation Considerations	Logic Switching Levels	Output Drive Capability
74LVT14D	SOT108-1 (SO14)	3.3V Hex Inverter Schmitt-Trigger	4~6	Low	14	None	TTL	Medium
74LVT14DB	SOT337-1 (SSOP14)	3.3V Hex Inverter Schmitt-Trigger	4~6	Low	14	None	TTL	Medium
74LVT14PW	SOT402-1 (TSSOP14)	3.3V Hex Inverter Schmitt-Trigger	4~6	Low	14	None	TTL	Medium

❑ Products, packages, availability and ordering

Type number	North American type number	Ordering code (12NC)	Marking/Packing  IC packing info	Package	Device status	Buy online
74LVT14D	74LVT14D	9352 091 70112	Standard Marking * Tube	SOT108-1 (SO14)	Full production	order this <input type="checkbox"/>
	74LVT14D-T	9352 091 70118	Standard Marking * Reel Pack, SMD, 13"	SOT108-1 (SO14)	Full production	order this <input type="checkbox"/>
74LVT14DB	74LVT14DB	9352 091 80112	Standard Marking * Tube	SOT337-1 (SSOP14)	Full production	order this <input type="checkbox"/>
	74LVT14DB-T	9352 091 80118	Standard Marking * Reel Pack, SMD, 13"	SOT337-1 (SSOP14)	Full production	order this <input type="checkbox"/>
74LVT14PW	74LVT14PW	9352 091 90112	Standard Marking * Tube	SOT402-1 (TSSOP14)	Full production	order this <input type="checkbox"/>
	74LVT14PW-T	9352 091 90118	Standard Marking * Reel Pack, SMD, 13"	SOT402-1 (TSSOP14)	Full production	order this <input type="checkbox"/>

Products in the above table are all in production. Some variants are discontinued; [click here](#) for information on these variants.

Similar products

[74LVT14](#) links to the similar products page containing an overview of products that are similar in function or related to the type number(s) as listed on this page. The similar products page includes products from the same catalog tree(s), relevant selection guides and products from the same functional category.

Support & tools

[Innovative Low Voltage Logic Solutions](#)(date 01-Aug-00)

[Introduction to Advanced BiCMOS Logic Products](#)(date 01-Mar-98)

[Family specifications LVT, family characteristics](#)(date 01-Mar-98)

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