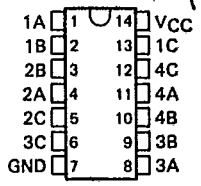
SN54HC4066, TLC4066I
SILICON-GATE CMOS QUADRUPLE BILATERAL ANALOG SWITCH

D2922, JANUARY 1986

- High Degree of Linearity
- High On-Off Output Voltage Ratio
- Low Crosstalk Between Switches
- Low On-State Impedance . . . Typically 30 Ohms at V_{CC} = 12 V
- Individual Switch Controls
- Extremely Low Input Current
- Functionally Interchangeable with National Semiconductor MM54/74HC4066, Motorola MC54/74HC4066, and RCA CD4066A

SN54HC4066 . . . J OR N PACKAGE
TLC4066I . . . D OR N PACKAGE
(TOP VIEW) T-51-11



description

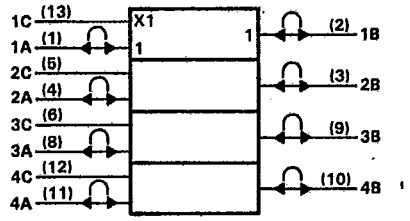
The TLC4066 is a silicon-gate CMOS quadruple analog switch integrated circuit designed to handle both analog and digital signals. Each switch permits signals with amplitudes up to 12 volts peak to be transmitted in either direction.

Each switch section has its own enable input control. A high-level voltage applied to this control terminal turns on the associated switch section.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

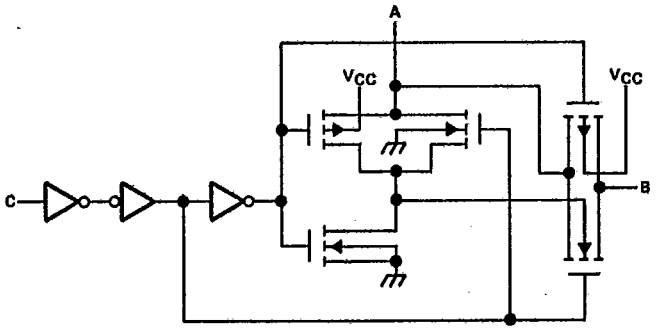
The SN54HC4066 is characterized for operation from −55°C to 125°C, and the TLC4066I is characterized from −40°C to 85°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range (see Note 1) ..... −0.5 V to 15 V
Control-input diode current ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
I/O port diode current ($V_I < 0$ or $V_{I/O} < V_{CC}$) ..... ±20 mA
On-state switch current ($V_{I/O} = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND pins ..... ±50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
D package ..... 950 mW
J package ..... 1025 mW
N package ..... 875 mW
Operating free-air temperature, T_A: SN54HC4066 ..... −55°C to 125°C
TLC4066I ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and N packages ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. For operation above 25°C free-air temperature, see Dissipation Derating Table.

DISSIPATION DERATING TABLE

Package	Maximum Power Dissipation			Derating Factor
	25°C	85°C	125°C	
D	950 mW	494 mW		7.6 mW/°C
J	1025 mW	533 mW	205 mW	8.2 mW/°C
N	875 mW	455 mW	175 mW	7.0 mW/°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		2†	5	12	V
I/O port voltage, $V_{I/O}$		0		V_{CC}	V
High-level input voltage, V_{IH}	V_{CC} = 2 V	1.5		V_{CC}	V
	V_{CC} = 4.5 V	3.15		V_{CC}	
	V_{CC} = 9 V	6.3		V_{CC}	
	V_{CC} = 12 V	8.4		V_{CC}	
Low-level input voltage, V_{IL}	V_{CC} = 2 V	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	
	V_{CC} = 9 V	0		1.8	
	V_{CC} = 12 V	0		2.4	
Input rise time, t_r	V_{CC} = 2 V			1000	ns
	V_{CC} = 4.5 V			500	
	V_{CC} = 9 V			400	
Input fall time, t_f	V_{CC} = 2 V			1000	ns
	V_{CC} = 4.5 V			500	
	V_{CC} = 9 V			400	
Operating free-air temperature, T_A	SN54HC4066	−55		125	°C
	TLC4066I	−40		85	

†With supply voltages at or near 2 volts, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	SN54HC4066			TLC4066I			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
r_{Son}	On-state switch resistance	I_S = 1 mA, V_A = 0 to V_{CC}, See Figure 1	4.5 V		100	220		100	200	Ω
			9 V		50	110		50	105	
			12 V		30	90		30	85	
		I_S = 1 mA, V_A = 0 or V_{CC}, See Figure 1	2 V		120	240		120	215	
			4.5 V		50	120		50	100	
			9 V		35	80		35	75	
			12 V		20	70		20	60	
	On-state switch resistance matching	V_A = 0 to V_{CC}, See Figure 1	4.5 V		10	20		10	20	Ω
			9 V		5	15		5	15	
			12 V		5	15		5	15	
I_I	Control input current	V_I = 0 or V_{CC}	2 V or 6 V			±1			±1	μA
I_{Soff}	Off-state switch leakage current	V_S = ±V_{CC}, See Figure 2	5.5 V		±10	±600		±10	±600	nA
			9 V		±15	±800		±15	±800	
			12 V		±20	±1000		±20	±1000	
I_{Son}	On-state switch leakage current	V_A = 0 or V_{CC}, See Figure 3	5.5 V		±10	±150		±10	±150	nA
			9 V		±15	±200		±15	±200	
			12 V		±20	±300		±20	±300	
I_{CC}	Supply current	V_I = 0 or V_{CC}, I_O = 0	5.5 V		2	40		2	20	μA
			9 V		8	160		8	80	
			12 V		16	320		16	160	
C_i	Input capacitance	A or B	2 V to 12 V		15			15		pF
		C			5	10		5	10	
C_f	Feedthrough capacitance	A to B	V_I = 0	2 V to 12 V	5			5		pF

†All typical values are at T_A = 25°C.

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switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	SN54HC4066			TLC4066I			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{pd}	Propagation delay time, A to B or B to A	See Figure 4	2 V		25	75		15	30	ns
			4.5 V		5	15		5	13	
			9 V		4	12		4	10	
			12 V		3	13		3	11	
t_{on}	Switch turn-on time	R_L = 1 kΩ, See Figures 5 and 6	2 V		32	150		32	125	ns
			4.5 V		8	30		8	25	
			9 V		6	18		6	15	
			12 V		5	15		5	13	
t_{off}	Switch turn-off time	R_L = 1 kΩ, See Figures 5 and 6	2 V		45	252		45	210	ns
			4.5 V		15	54		15	45	
			9 V		10	48		10	40	
			12 V		8	45		8	38	
f_{co}	Switch cutoff frequency (channel loss = 3 dB)		4.5 V		100			100		MHz
			9 V		120			120		
$V_{OCF(PP)}$	Control feedthrough voltage to any switch, peak to peak	See Figure 7	4.5 V		180				180	mV
	Frequency at which crosstalk attenuation between any two switches equals 50 dB	See Figure 8	4.5 V		1			1		MHz

†All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

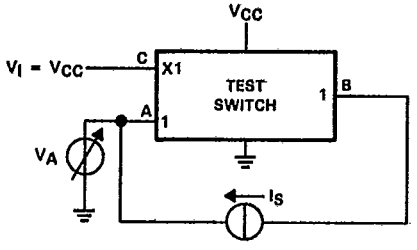
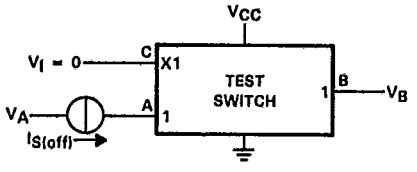


FIGURE 1. ON-STATE RESISTANCE TEST CIRCUIT



$V_S = V_A - V_B$
CONDITION 1: V_A = 0, $V_B = V_{CC}$
CONDITION 2: $V_A = V_{CC}$, V_B = 0

FIGURE 2. OFF-STATE SWITCH LEAKAGE CURRENT TEST CIRCUIT

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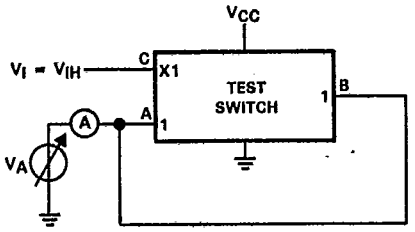
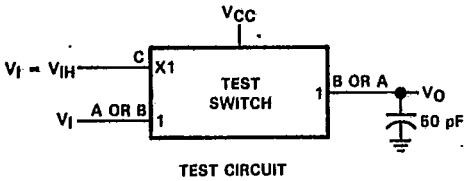
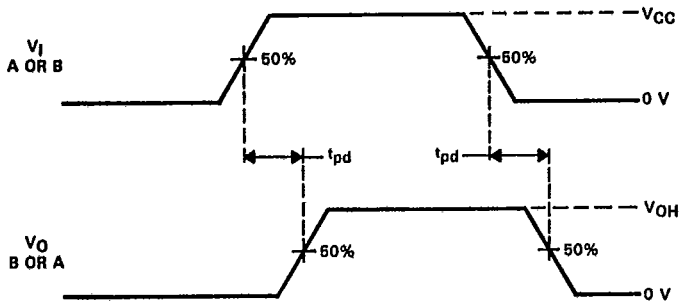


FIGURE 3. ON-STATE SWITCH LEAKAGE CURRENT TEST CIRCUIT



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 4. PROPAGATION DELAY TIME, SIGNAL INPUT TO SIGNAL OUTPUT

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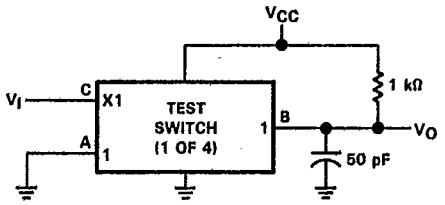
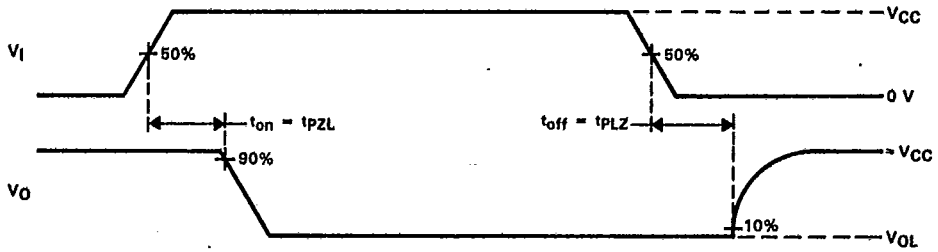
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 5. SWITCHING TIME (t_{PZL}, t_{PLZ}), CONTROL TO SIGNAL OUTPUT

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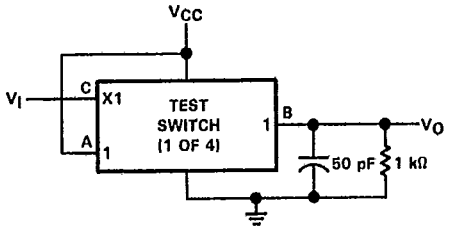
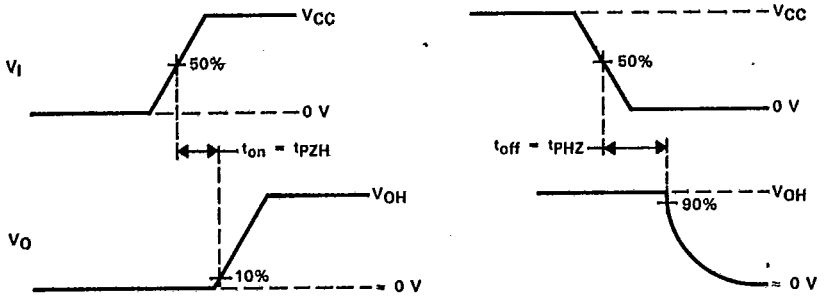


TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 6. SWITCHING TIME (t_{PZH}, t_{PHZ}), CONTROL TO SIGNAL OUTPUT

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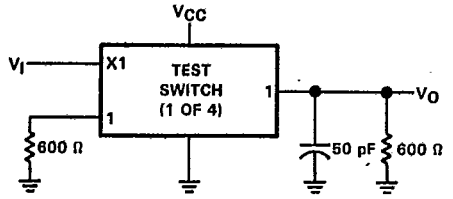
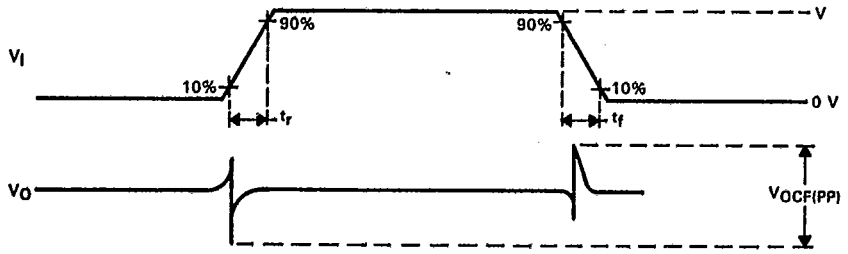
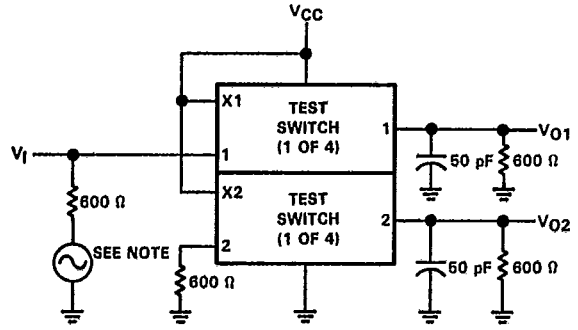


TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 7. CONTROL FEEDTHROUGH VOLTAGE



NOTE: ADJUST f for $a_X = \frac{V_{O2}}{V_{O1}} = 50$ dB.

FIGURE 8. CROSSTALK BETWEEN ANY TWO SWITCHES, TEST CIRCUIT

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