Rochester Electronics

Datasheet

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

HI-5040 thru HI-5051, HI-5046A and HI-5047A

August 1997

CMOS Analog Switches

Features

- Wide Analog Signal Range ..... ±15V
- Low "ON" Resistance (Typ) 25Ω
- High Current Capability (Typ) 80mA
- Break-Before-Make Switching
  - Turn-On Time (Typ) 370ns
  - Turn-Off Time (Typ) 280ns
- No Latch-Up
- Input MOS Gates are Protected from Electrostatic Discharge
- DTL, TTL, CMOS, PMOS Compatible

Applications

- High Frequency Switching
- Sample and Hold
- Digital Filters
- Operational Amplifier Gain Switching

Description

This family of CMOS analog switches offers low resistance switching performance for analog voltages up to the supply rails and for signal currents up to 80mA. "ON" resistance is low and stays reasonably constant over the full range of operating signal voltage and current. r_{ON} remains exceptionally constant for input voltages between +5V and -5V and currents up to 50mA. Switch impedance also changes very little over temperature, particularly between 0°C and 75°C. r_{ON} is nominally 25Ω for HI-5048 through HI-5051 and HI-5046A and HI-5047A and 50Ω for HI-5040 through HI-5047.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. Performance is further enhanced by Dielectric Isolation processing which insures latch-free operation with very low input and output leakage currents (0.8nA at 25°C). This family of switches also features very low power operation (1.5mW at 25°C).

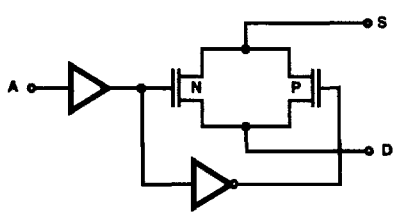
There are 14 devices in this switch series which are differentiated by type of switch action and value of R_{ON} (see Functional Description). All devices are available in 16 lead DIP packages. The HI-5040 and HI-5050 switches can directly replace IH-5040 series devices except IH5048, and are functionally compatible with the DG180 and DG190 family. Each switch type is available in the -55°C to 125°C and 0°C to 75°C performance grades.

Functional Description

PART NUMBER	TYPE	r_{ON}
HI-5040	SPST	50Ω
HI-5041	Dual SPST	50Ω
HI-5042	SPDT	50Ω
HI-5043	Dual SPDT	50Ω
HI-5044	DPST	50Ω
HI-5045	Dual DPST	50Ω
HI-5046	DPDT	50Ω
HI-5046A	DPDT	25Ω
HI-5047	4PST	50Ω
HI-5047A	4PST	25Ω
HI-5048	Dual SPST	25Ω
HI-5049	Dual DPST	25Ω
HI-5050	SPDT	25Ω
HI-5051	Dual SPDT	25Ω

Functional Block Diagram

TYPICAL DIAGRAM



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3127.1**

Ordering Information

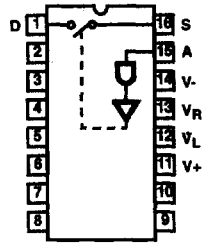
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI3-5040-5	0 to 75	16 Ld PDIP	E16.3
HI1-5040-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-5040-5	0 to 75	16 Ld CERDIP	F16.3
HI3-5041-5	0 to 75	16 Ld PDIP	E16.3
HI1-5041-5	0 to 75	16 Ld CERDIP	F16.3
HI1-5041-2	-55 to 125	16 Ld CERDIP	F16.3
HI3-5042-5	0 to 75	16 Ld PDIP	E16.3
HI1-5042-5	0 to 75	16 Ld CERDIP	F16.3
HI1-5042-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-5043-7	0 to 75 + 96 Hr. Burn-In	16 Ld CERDIP	F16.3
HI1-5043-2	-55 to 125	16 Ld CERDIP	F16.3
HI3-5043-5	0 to 75	16 Ld PDIP	E16.3
HI1-5043-5	0 to 75	16 Ld CERDIP	F16.3
HI1-5044-5	0 to 75	16 Ld CERDIP	F16.3
HI3-5044-5	0 to 75	16 Ld PDIP	E16.3
HI1-5045-5	0 to 75	16 Ld CERDIP	F16.3
HI1-5045-2	-55 to 125	16 Ld CERDIP	F16.3
HI3-5045-5	0 to 75	16 Ld PDIP	E16.3
HI1-5046-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-5046-5	0 to 75	16 Ld CERDIP	F16.3
HI3-5046-5	0 to 75	16 Ld PDIP	E16.3
HI3-5046A-5	0 to 75	16 Ld PDIP	E16.3
HI1-5046A-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-5046A-5	0 to 75	16 Ld CERDIP	F16.3
HI1-5047-5	0 to 75	16 Ld CERDIP	F16.3
HI1-5047-2	-55 to 125	16 Ld CERDIP	F16.3
HI3-5047-5	0 to 75	16 Ld PDIP	E16.3
HI1-5047A-5	0 to 75	16 Ld CERDIP	F16.3
HI1-5047A-2	-55 to 125	16 Ld CERDIP	F16.3
HI3-5047A-5	0 to 75	16 Ld PDIP	E16.3
HI1-5048-5	0 to 75	16 Ld CERDIP	F16.3
HI3-5048-5	0 to 75	16 Ld PDIP	E16.3
HI1-5048-2	-55 to 125	16 Ld CERDIP	F16.3

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1-5049-5	0 to 75	16 Ld CERDIP	F16.3
HI1-5049-2	-55 to 125	16 Ld CERDIP	F16.3
HI3-5049-5	0 to 75	16 Ld PDIP	E16.3
HI1-5050-5	0 to 75	16 Ld CERDIP	F16.3
HI1-5050-2	-55 to 125	16 Ld CERDIP	F16.3
HI3-5050-5	0 to 75	16 Ld PDIP	E16.3
HI1-5051-5	0 to 75	16 Ld CERDIP	F16.3
HI1-5051-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-5051-7	0 to 75 + 96 Hr. Burn-In	16 Ld CERDIP	F16.3
HI4P5051-5	0 to 75	20 Ld PLCC	N20.35
HI3-5051-5	0 to 75	16 Ld PDIP	E16.3
HI1-5040/883	-55 to 125	16 Ld CERDIP	F16.3
HI1-5041/883	-55 to 125	16 Ld CERDIP	F16.3
HI1-5042/883	-55 to 125	16 Ld CERDIP	F16.3
HI1-5043/883	-55 to 125	16 Ld CERDIP	F16.3
HI1-5044/883	-55 to 125	16 Ld CERDIP	F16.3
HI1-5045/883	-55 to 125	16 Ld CERDIP	F16.3
HI1-5046/883	-55 to 125	16 Ld CERDIP	F16.3
HI1-5046A/883	-55 to 125	16 Ld CERDIP	F16.3
HI1-5047/883	-55 to 125	16 Ld CERDIP	F16.3
HI1-5047A/883	-55 to 125	16 Ld CERDIP	F16.3
HI1-5048/883	-55 to 125	16 Ld CERDIP	F16.3
HI1-5049/883	-55 to 125	16 Ld CERDIP	F16.3
HI1-5050/883	-55 to 125	16 Ld CERDIP	F16.3
HI1-5051/883	-55 to 125	16 Ld CERDIP	F16.3
HI4-5043/883	-55 to 125	20 Lead CLCC	J20.A
HI4-5045/883	-55 to 125	20 Lead CLCC	J20.A
HI4-5051/883	-55 to 125	20 Lead CLCC	J20.A
HI9P5043-5	0 to 75	16 Ld SOIC	M16.15
HI9P5045-5	0 to 75	16 Ld SOIC	M16.15
HI9P5051-5	0 to 75	16 Ld SOIC	M16.15
HI9P5043-9	-40 to 85	16 Ld SOIC	M16.15
HI9P5051-9	-40 to 85	16 Ld SOIC	M16.15

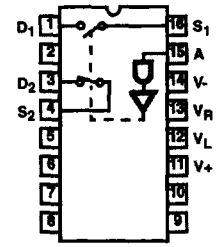
Pin Configurations Switch States are Logic "0" Input

SINGLE CONTROL

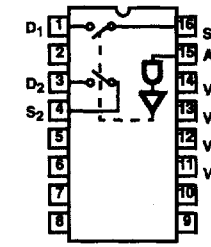
SPST
HI-5040 (50Ω)



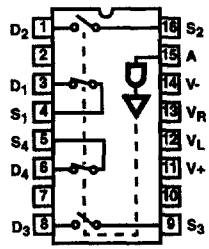
SPDT
HI-5042 (50Ω), HI-5050 (25Ω)



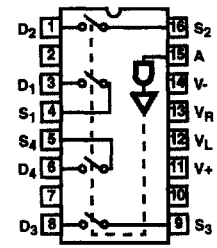
DPST
HI-5044 (50Ω)



DPDT
HI-5046 (50Ω), HI-5046A (25Ω)

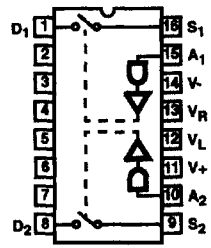


4PST
HI-5047 (50Ω), HI-5047A (25Ω)

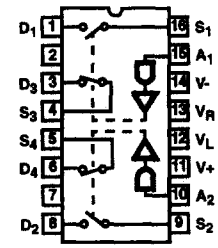


DUAL CONTROL

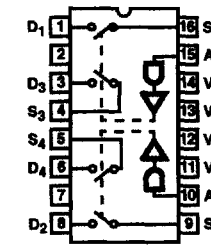
DUAL SPST
HI-5041 (50Ω)



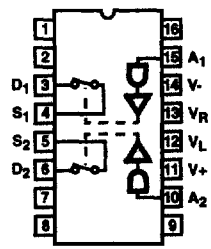
DUAL SPDT
HI-5043 (50Ω), HI-5051 (25Ω)



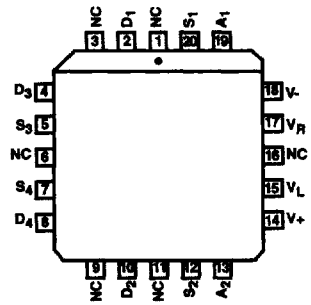
DUAL DPST
HI-5045 (50Ω), HI-5049 (25Ω)



DUAL SPST
HI-5048 (25Ω)



DUAL SPDT
HI-5043 (50Ω), HI-5051 (25Ω)

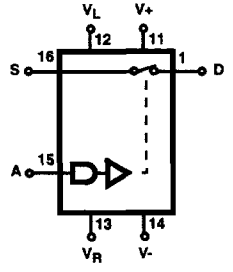


NOTE: Unused pins may be internally connected. Ground all unused pins.

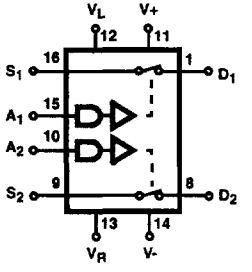
13 SWITCHES

Switch Functions Switch States are Logic "1" Input

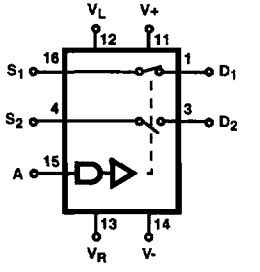
SPST
HI-5040 (50Ω)



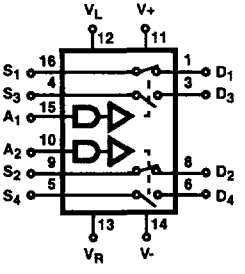
DUAL SPST
HI-5041 (50Ω)



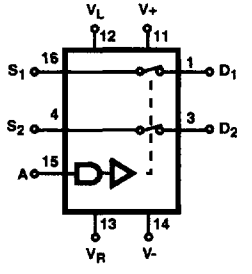
SPDT
HI-5042 (50Ω)



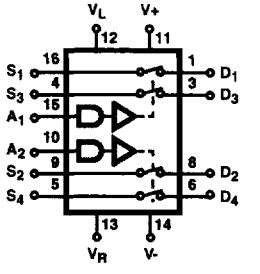
DUAL SPDT
HI-5043 (50Ω)



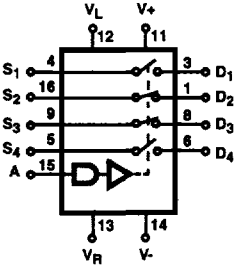
DPST
HI-5044 (50Ω)



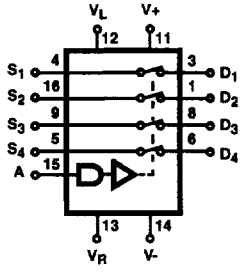
DUAL DPST
HI-5045 (50Ω)



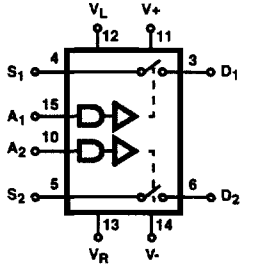
DPDT
HI-5046 (50Ω), HI-5046A (25Ω)



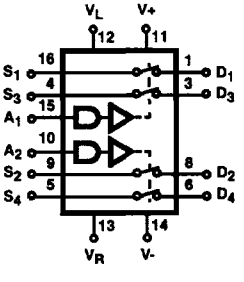
4PST
HI-5047 (50Ω), HI-5047A (25Ω)



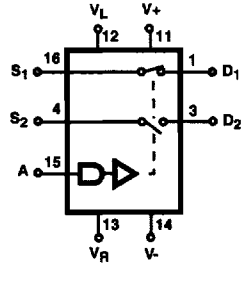
DUAL SPST
HI-5048 (25Ω)



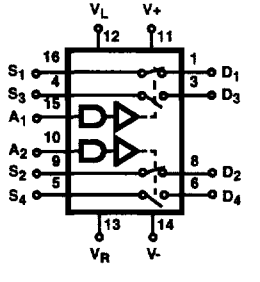
DUAL DPST
HI-5049 (25Ω)



SPDT
HI-5050 (25Ω)



DUAL SPDT
HI-5051 (25Ω)



Absolute Maximum Ratings

Supply Voltage (V+, V-) 36V
V_R to Ground ..... V+, V-
Digital and Analog Input Voltage ... $+V_{SUPPLY}$ +4V, $-V_{SUPPLY}$ -4V
Analog Current (S to D) Continuous 30mA
Analog Current (S to D) Peak 80mA

Operating Conditions

Temperature Range
HI-50XX-2 ..... -55°C to 125°C
HI-50XX-5, -7 ..... 0°C to 75°C
HI-50XX-9 ..... -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	85	32
SOIC Package	120	N/A
PDIP Package	100	N/A
PLCC Package	80	N/A
CLCC Package	65	14

Maximum Junction Temperature
Plastic Packages ..... 150°C
Ceramic Packages ..... 175°C
Maximum Storage Temperature ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(PLCC, SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Supplies = +15V, -15V; V_R = 0V; V_{AH} (Logic Level High) = 2.4V, V_{AL} (Logic Level Low) = +0.8V, V_L = +5V, Unless Otherwise Specified. For Test Conditions, Consult Performance Characteristics, Unused Pins are Grounded

PARAMETER	TEST CONDITIONS	TEMP (°C)	-55°C TO 125°C			0°C TO 75°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS									
t_{ON}, Switch On Time	(Note 5)	25	-	370	500	-	370	500	ns
t_{OFF}, Switch Off Time	(Note 5)	25	-	280	500	-	280	500	ns
Charge Injection	(Note 3)	25	-	5	20	-	5	-	mV
"Off Isolation"	(Note 4)	25	75	80	-	-	80	-	dB
"Crosstalk"	(Note 4)	25	80	88	-	-	88	-	dB
$C_{S(OFF)}$, Input Switch Capacitance		25	-	11	-	-	11	-	pF
$C_{D(OFF)}$, Output Switch Capacitance		25	-	11	-	-	11	-	pF
$C_{D(ON)}$, Output Switch Capacitance		25	-	22	-	-	22	-	pF
C_A, Digital Input Capacitance		25	-	5	-	-	5	-	pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance		25	-	0.5	-	-	0.5	-	pF
DIGITAL INPUT CHARACTERISTICS									
V_{AL}, Input Low Threshold		Full	-	-	0.8	-	-	0.8	V
V_{AH}, Input High Threshold		Full	2.4	-	-	2.4	-	-	V
I_A, Input Leakage Current (High or Low)		Full	-	0.01	1.0	-	0.01	1.0	µA
ANALOG SWITCH CHARACTERISTICS									
Analog Signal Range		Full	-15	-	+15	-15	-	+15	V
r_{ON}, On Resistance	(Note 2A)	25	-	50	75	-	50	75	Ω
		Full	-	-	150	-	-	150	Ω
r_{ON}, On Resistance	(Note 2B)	25	-	25	45	-	25	45	Ω
		Full	-	-	50	-	-	50	Ω
r_{ON}, Channel-to-Channel Match	(Note 2A)	25	-	2	10	-	2	10	Ω
r_{ON}, Channel-to-Channel Match	(Note 2B)	25	-	1	5	-	1	5	Ω

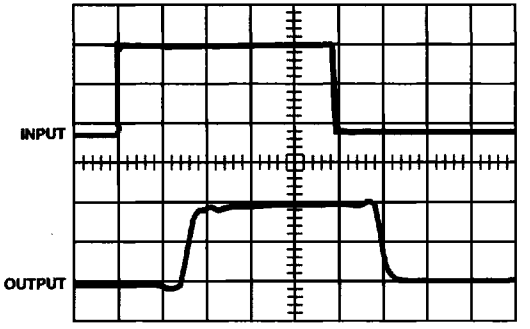
Electrical Specifications Supplies = +15V, -15V; V_R = 0V; V_{AH} (Logic Level High) = 2.4V, V_{AL} (Logic Level Low) = +0.8V, V_L = +5V, Unless Otherwise Specified. For Test Conditions, Consult Performance Characteristics, Unused Pins are Grounded **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	-55°C TO 125°C			0°C TO 75°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$I_{S(OFF)}$ = $I_{D(OFF)}$, Off Input or Output Leakage Current		25	-	0.8	2	-	0.8	2	nA
		Full	-	100	200	-	100	200	nA
$I_{D(ON)}$, On Leakage Current		25	-	0.01	2	-	0.01	2	nA
		Full	-	2	200	-	2	200	nA
POWER REQUIREMENTS									
P_D, Quiescent Power Dissipation		25	-	1.5	-	-	1.5	-	mW
I+, I-, I_L, I_R		25	-	-	0.2	-	-	0.3	mA
I+, +15V Quiescent Current	(Note 5)	Full	-	-	0.3	-	-	0.5	mA
I-, -15V Quiescent Current	(Note 5)	Full	-	-	0.3	-	-	0.5	mA
I_L, +5V Quiescent Current	(Note 5)	Full	-	-	0.3	-	-	0.5	mA
I_R, Ground Quiescent Current	(Note 5)	Full	-	-	0.3	-	-	0.5	mA

NOTES:

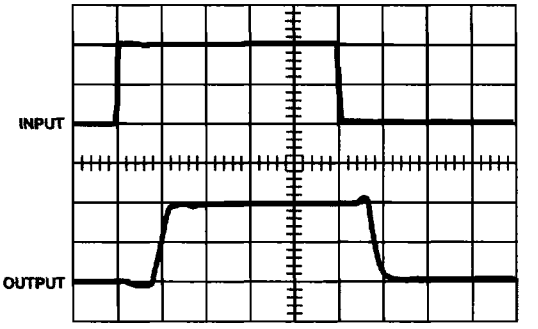
2. V_{OUT} = ±10V, I_{OUT} = ∓1mA
   A). For HI-5040 thru HI-5047
   B). For HI-5048 thru HI-5051, HI-5046A/5047A.
3. V_{IN} = 0V, C_L = 10,000pF.
4. R_L = 100Ω, f = 100kHz, V_{IN} = 2.0V_{P-P}, C_L = 5pF.
5. V_{AL} = 0V, V_{AH} = 5V.

Switching Waveforms



Top: TTL Input (1V/Div.)
V_{AH} = 5V, V_{AL} = 0V
Bottom: Output (2V/Div.)
Horizontal: 200ns/Div.

FIGURE 1.



Top: CMOS Input (5V/Div.)
V_{AH} = 10V, V_{AL} = 0V
Bottom: Output (5V/Div.)
Horizontal: 200ns/Div.

FIGURE 2.

Typical Performance Curves and Test Circuits

$T_A = 25^oC$, V+ = +15V, V- = -15V, V_L = +5V, V_R = 0V, V_{AH} = 3V and V_{AL} = 0.8V, Unless Otherwise Specified

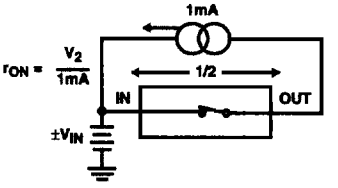


FIGURE 3. "ON" RESISTANCE vs ANALOG SIGNAL LEVEL, SUPPLY VOLTAGE AND TEMPERATURE

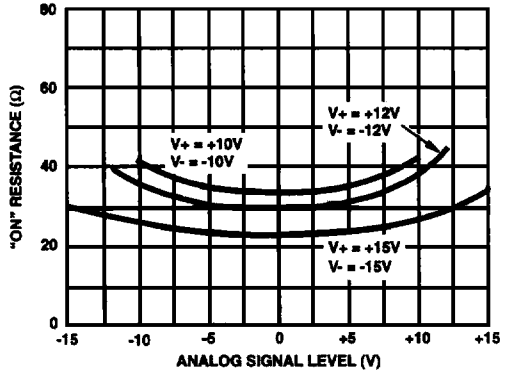


FIGURE 4. "ON" RESISTANCE vs ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE

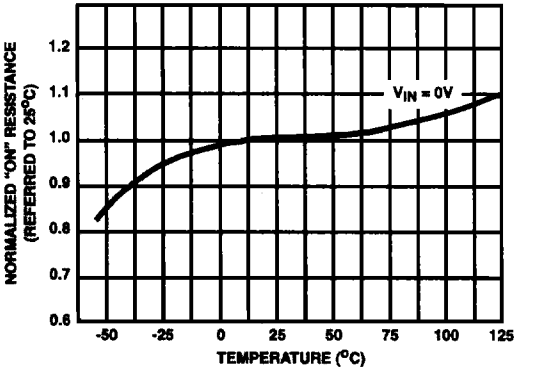
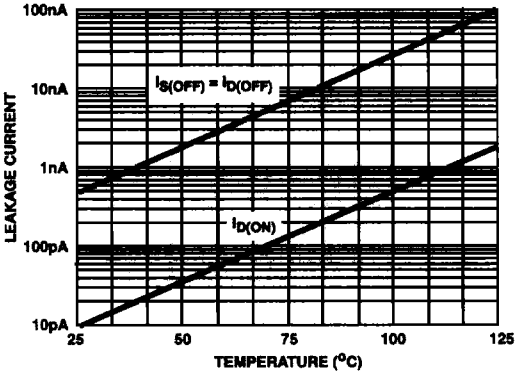
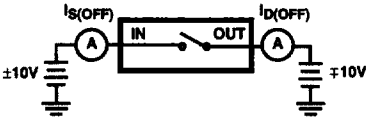


FIGURE 5. NORMALIZED "ON" RESISTANCE vs TEMPERATURE



OFF LEAKAGE CURRENT vs TEMPERATURE



ON LEAKAGE CURRENT vs TEMPERATURE

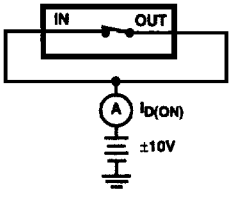
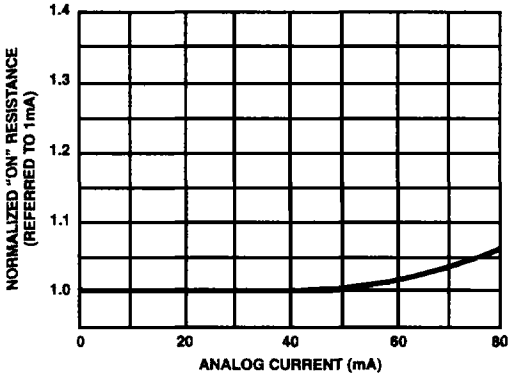


FIGURE 6. ON/OFF LEAKAGE CURRENT vs TEMPERATURE

Typical Performance Curves and Test Circuits

$T_A = 25^oC$, V+ = +15V, V- = -15V, V_L = +5V, V_R = 0V, V_{AH} = 3V and V_{AL} = 0.8V, Unless Otherwise Specified **(Continued)**



"ON" RESISTANCE vs ANALOG CURRENT

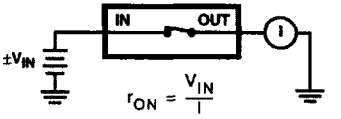
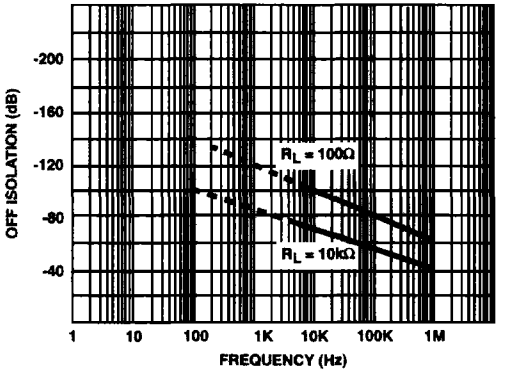
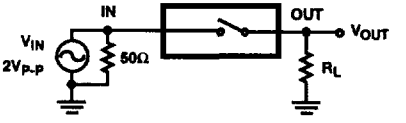


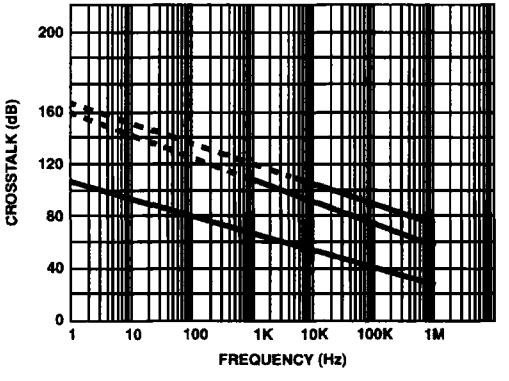
FIGURE 7. NORMALIZED "ON" RESISTANCE vs ANALOG CURRENT

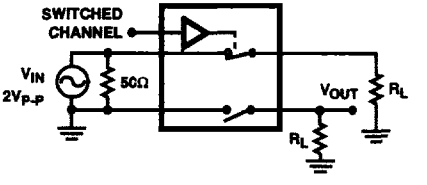




$$\text{OFF ISOLATION} = 20\,\text{Log}\left(\frac{V_{IN}}{V_{OUT}}\right)$$

FIGURE 8. "OFF" ISOLATION vs FREQUENCY



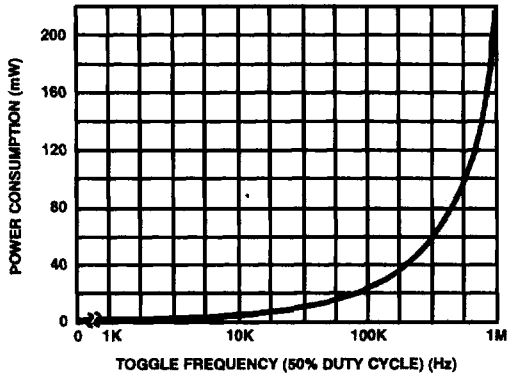


$$\text{CROSSTALK} = 20\,\text{Log}\left(\frac{V_{IN}}{V_{OUT}}\right)$$

FIGURE 9. CROSSTALK vs FREQUENCY

Typical Performance Curves and Test Circuits

$T_A = 25^oC$, V+ = +15V, V- = -15V, V_L = +5V, V_R = 0V, V_{AH} = 3V and V_{AL} = 0.8V, Unless Otherwise Specified **(Continued)**



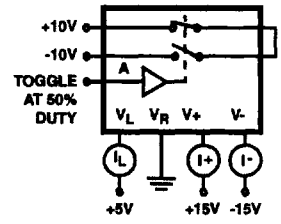


FIGURE 10. POWER CONSUMPTION vs FREQUENCY

Switching Characteristics

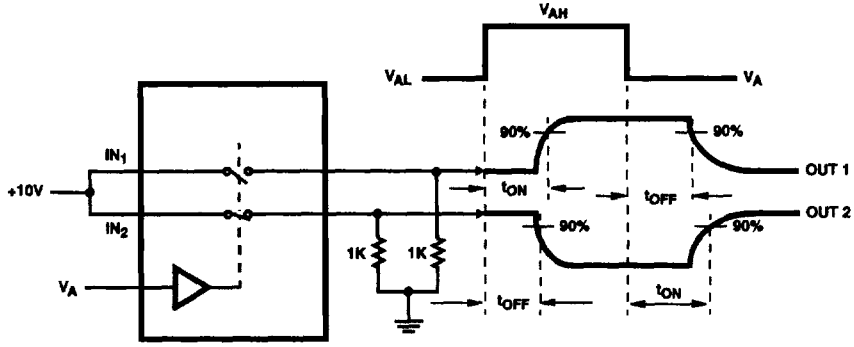


FIGURE 11. ON/OFF SWITCH TIME vs LOGIC LEVEL

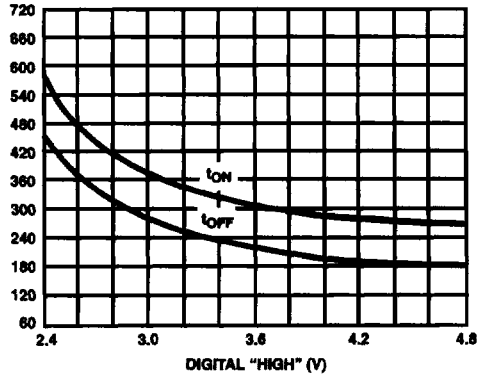


FIGURE 12. SWITCHING TIMES FOR POSITIVE DIGITAL TRANSITION

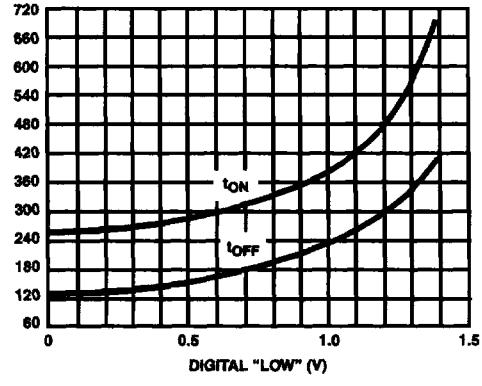
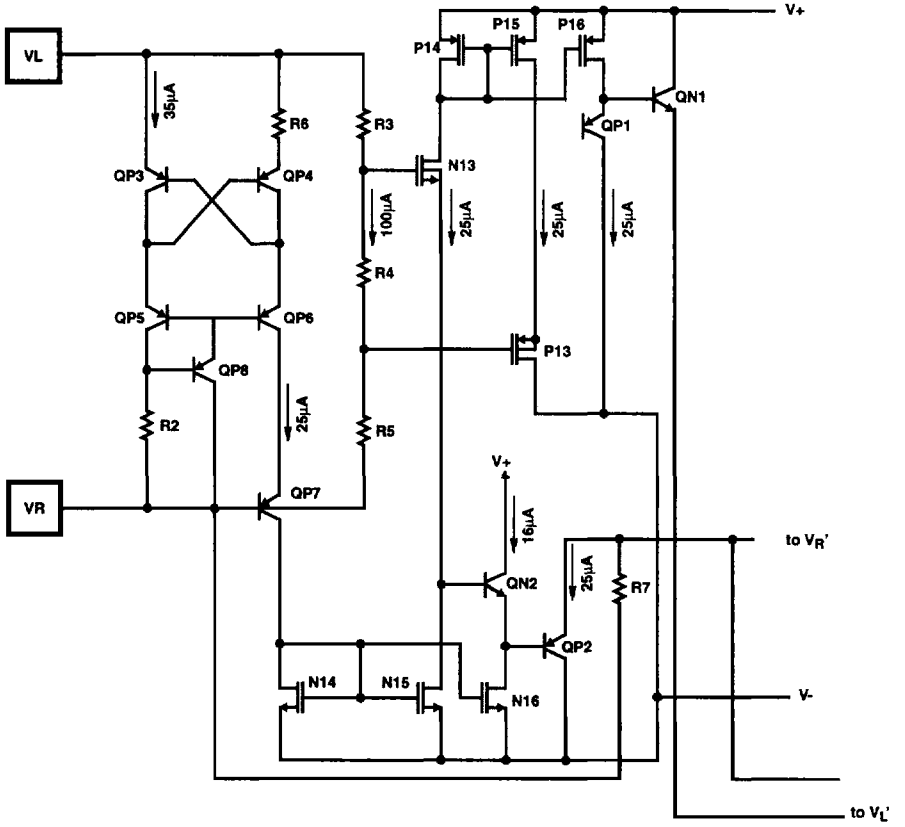


FIGURE 13. SWITCHING TIMES FOR NEGATIVE DIGITAL TRANSITION

Switching Characteristics (Continued)



NOTE: Connect V+ to V_L for minimizing power consumption when driving from CMOS circuits.

FIGURE 14. TTL/CMOS REFERENCE CIRCUIT (NOTE)

Switching Characteristics (Continued)

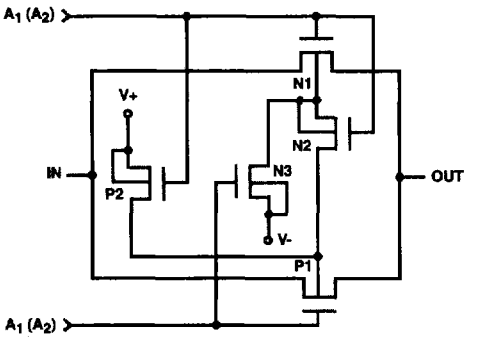
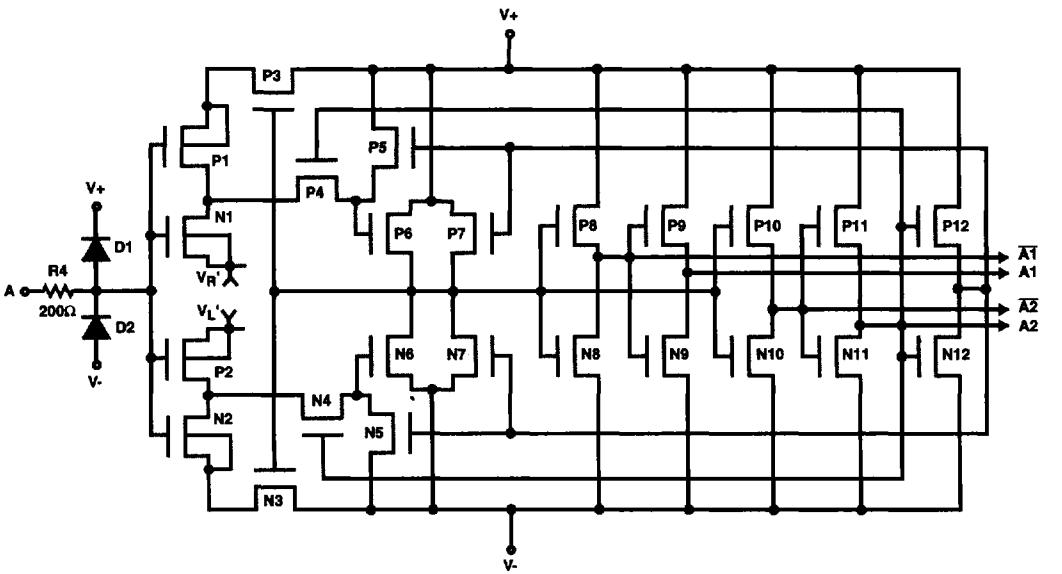


FIGURE 15. SWITCH CELL



NOTES:

1. All N-Channel bodies to V-, all P-Channel bodies to V+ except as shown.
2. For further information refer to Application Notes AN520, AN521, AN531, AN532 and AN557.

FIGURE 16. DIGITAL INPUT BUFFER AND LEVEL SHIFTER