Features

128Kx8 bit CMOS Static Random Access Memory

- Fast Access Times: 12, 15, 17, 20, 25, 35, 45, & 55ns
- $\overline{E}$ and $\overline{G}$ Functions for Bus Control
- 2V Data Retention (EDI88128LPS)
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

Thru-hole and Surface Mount Packages

Jedec Pinout

- 32 Pin Dual-in-line Packages
  Ceramic DIP, 400 mils Wide, No. 102
  Ceramic DIP, 600 mils Wide, No. 9
- 32 Lead Ceramic ZIP, No. 100
- 32 Lead Ceramic SOJ, No. 140
- 32 Pad Ceramic LCC, No. 141
- 32 Lead Ceramic Flatpack, No. 142

Single +5V (±10%) Supply Operation

*Industrial Temperature Range

128Kx8 Monolithic High Speed CMOS Static RAM

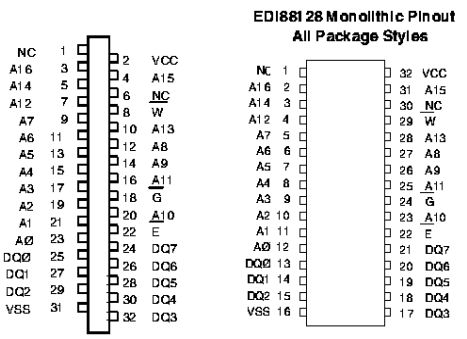
The EDI88128CS is a high speed, high performance, megabit density monolithic Static RAM organized as 128Kx8 bits.

The device has eight bi-directional input-output lines to provide simultaneous access to all bits in a word. An automatic power down feature permits the on-chip circuitry to enter a very low standby mode and be brought back into operation at a speed equal to the address access time.

A Low Power version, EDI88128LPS, includes a 2V Data Retention Function for battery back-up operation.

Military product available compliant to of MIL-PRF-38535.

Pin Configurations and Block Diagram

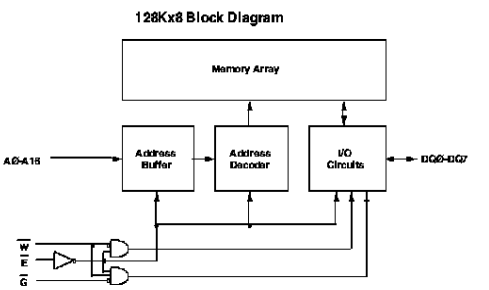


EDI88128 Monolithic Pinout
All Package Styles

Pin Names

AØ-A16	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQØ-DQ7	Common Data Input/Output
VCC	Power(+5V±10%)
VSS	Ground
NC	No Connection

128Kx8 Block Diagram



Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Military	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Power Dissipation	2 Watts
Output Current	40 mA
Junction Temperature, TJ	175°C

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	VCC+0.5	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

(note: For TEHQZ, TGHQZ and TWLQZ, Figure 2)

Figure 1

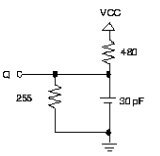
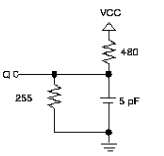


Figure 2



DC Electrical Characteristics

Parameter	Sym	Conditions		Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA	12-17ns	–		300	mA
			20ns	–		225	mA
			25-55ns	–		200	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ ≥VIH, VIL≥VIN≥VIH	17-55ns	–		25	mA
			12-15ns			60	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$≥VCC-0.2	CS17-55ns	–	3	10	mA
		VIN≥VCC-0.2V or VIN≤0.2V	CS12-15ns	–	–	15	mA
			LPS	–	--	5	mA
Input Leakage Current	ILI	VIN = 0V to VCC		–	–	±5	µA
Output Leakage Current	ILO	VI/O = 0V to VCC		–	–	±10	µA
Output High Voltage	VOH	IOH = -4.0mA		2.4	–	–	V
Output Low Voltage	VOL	IOL = 8.0mA		–	–	0.4	V

*Typical TA=25°C, VCC=5.0V

Truth Table

G	E	W	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max		Unit
		LCC	ZIP, CSOJ, DIP, Flatpack	
Address Lines	CI	6	12	pF
Data Lines	CD/Q	8	14	pF

These parameters are sampled, not 100% tested.

AC Characteristics Read Cycle

	Symbol		12ns		15ns		17ns		20ns		
Parameter	**JEDEC**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Read Cycle Time	TAVAV	TRC	12		15		17		20		ns
Address Access Time	TAVQV	TAA		12		15		17		20	ns
Chip Enable Access Time	TELQV	TACS		12		15		17		20	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		7		8		8		10	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		7		6		6		8	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		0		ns
Output Disable to Output in High Z (1)	TGHQZ	TOHZ		7		6		6		8	ns
Chip Enable to Power Up (1)	TELICCH	TPU	0		0		0		0		ns
Chip Enable to Power Down (1)	TEHICCL	TPD		12		15		17		20	ns

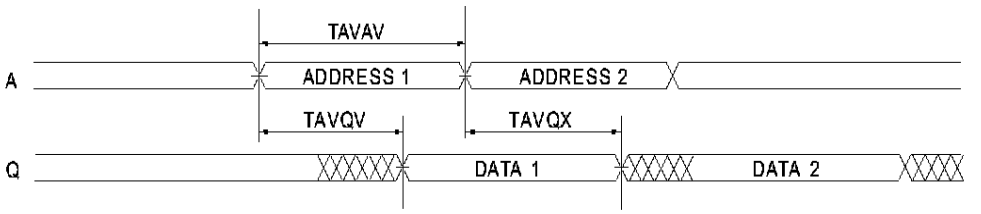
* Commercial, Industrial Temp Only
Note 1: Parameter guaranteed, but not tested.

AC Characteristics Read Cycle

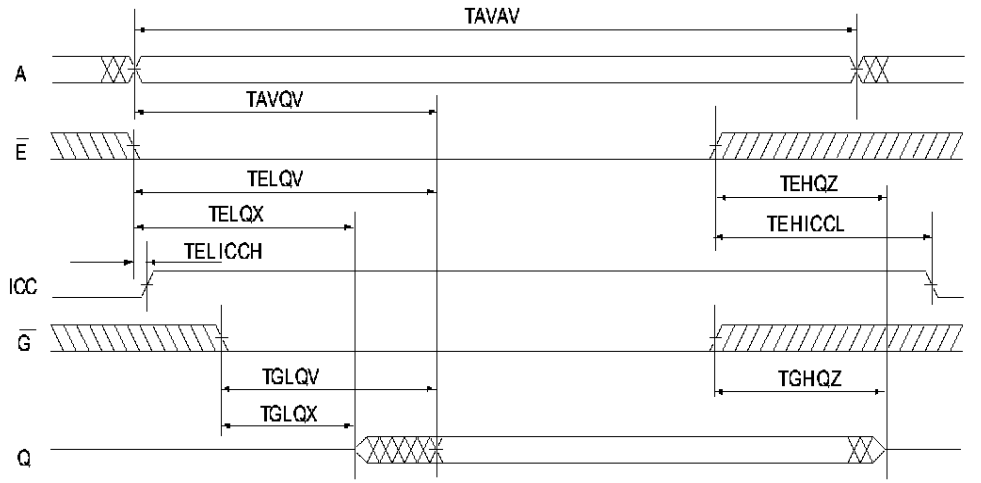
	Symbol		25ns		35ns		45ns		55ns		
Parameter	**JEDEC**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Read Cycle Time	TAVAV	TRC	25		35		45		55		ns
Address Access Time	TAVQV	TAA		25		35		45		55	ns
Chip Enable Access Time	TELQV	TACS		25		35		45		55	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		12		20		25		25	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		10		20		25		25	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		0		ns
Output Disable to Output in High Z (1)	TGHQZ	TOHZ		10		20		25		25	ns
Chip Enable to Power Up (1)	TELICCH	TPU	0		0		0		0		ns
Chip Enable to Power Down (1)	TEHICCL	TPD		25		35		45		55	ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1 - W High; G, E Low



Read Cycle 2 - W High

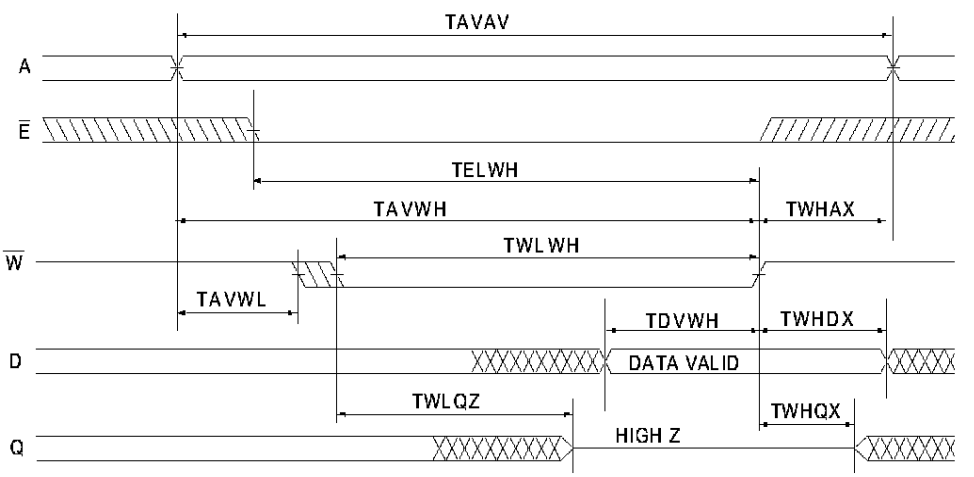


AC Characteristics Write Cycle

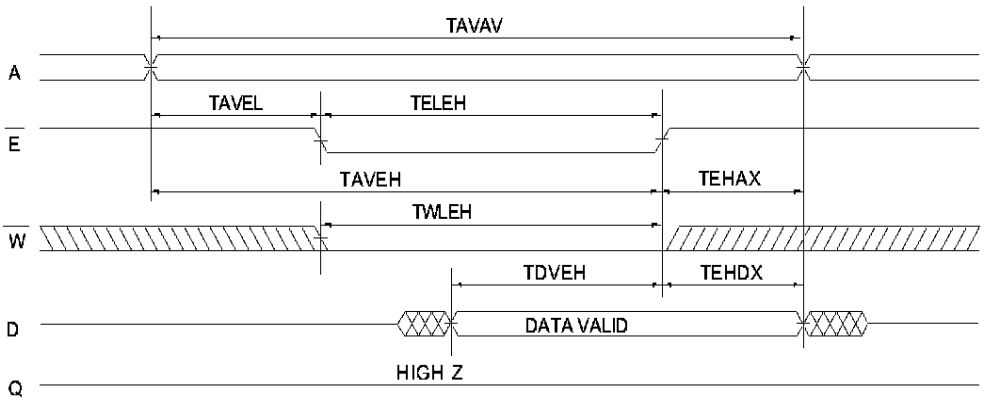
	Symbol		12ns	15ns	17ns	20ns	25ns	35ns	45ns	55ns	
Parameter	JEDEC	Alt	Min Max	Min Max	Min Max	Min Max	Min Max	Min Max	Min Max	Min Max	Units
Write Cycle Time	TAVAV	TWC	12	15	17	20	25	35	45	55	ns
Chip Enable to	TELWH	TCW	11	12	13	15	20	30	35	40	ns
End of Write	TELEH	TCW	11	12	13	15	20	30	35	40	ns
Address Setup	TAVWL	TAS	0	0	0	0	0	0	0	0	ns
Time	TAVEL	TAS	0	0	0	0	0	0	0	0	ns
Address Valid to	TAVWH	TAW	11	12	13	15	20	30	35	40	ns
End of Write	TAVEH	TAW	11	12	13	15	20	30	35	40	ns
Write Pulse Width	TWLWH	TWP	11	12	13	15	20	30	35	40	ns
	TWLEH	TWP	11	12	13	15	20	30	35	40	ns
Write Recovery	TWHAX	TWR	5	0	0	0	0	0	0	0	ns
Time	TEHAX	TWR	5	0	0	0	0	0	0	0	ns
Data Hold Time	TWHDX	TDH	0	0	0	0	0	0	0	0	ns
	TEHDX	TDH	0	0	0	0	0	0	0	0	ns
Write to Output	TWLQZ	TWHZ	0 7	0 8	0 8	0 10	0 10	0 15	0 20	0 20	ns
in High Z (1)			8								
Data to Write	TDVWH	TDW	8	7	7	8	15	20	25	25	ns
Time	TDVEH	TDW		7	7	8	15	20	25	25	ns
Output Active from	TWHQX	TWLZ	5	3	3	3	3	3	3	3	ns
End of Write (1)											

* Commercial, Industrial Temp Only
Note 1: Parameter guaranteed, but not tested.

Write Cycle 1 - W Controlled



Write Cycle 2 - E Controlled



Data Retention Characteristics

(TA = -55°C to +125°C), (TA = -40°C to +85°C)

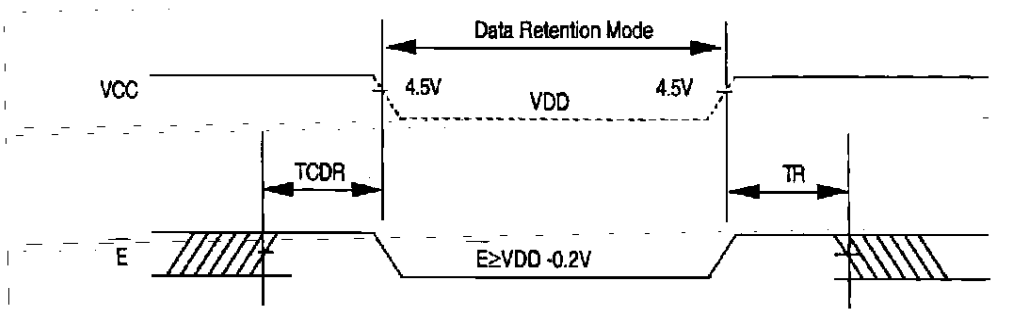
Low Power (LPS) Version Only

Characteristic	Sym	Test Conditions	Min	Typ	Max	Unit
Data Retention Voltage	VDD	VDD = 2.0V	2	–	–	V
Data Retention Quiescent Current	ICCDR	$\overline{E} \geq$ VDD-0.2V	–	500	750	µA
Chip Disable to Data Retention Time(1)	TCDR	VIN ≥ VDD -0.2V	0	–	–	ns
Operation Recovery Time (1)	TR	or VIN ≤ 0.2V	TAVAV*		–	ns

Note 1: Parameter guaranteed, but not tested.

*Read Cycle Time

Data Retention E Controlled



Ordering Information

Part No. Standard Power	Speed ns	Package No.
EDI88128CS15CI	15	9
EDI88128CS17CI	17	9
EDI88128CS17CB	17	9
EDI88128CS20CB	20	9
EDI88128CS25CB	25	9
EDI88128CS35CB	35	9
EDI88128CS45CB	45	9
EDI88128CS55CB	55	9
EDI88128CS15FI	15	142
EDI88128CS17FI	17	142
EDI88128CS17FB	17	142
EDI88128CS20FB	20	142
EDI88128CS25FB	25	142
EDI88128CS35FB	35	142
EDI88128CS45FB	45	142
EDI88128CS55FB	55	142
EDI88128CS15LI	15	141
EDI88128CS17LI	17	141
EDI88128CS17LB	17	141
EDI88128CS20LB	20	141
EDI88128CS25LB	25	141
EDI88128CS35LB	35	141
EDI88128CS45LB	45	141
EDI88128CS55LB	55	141
EDI88128CS15NI	15	140
EDI88128CS17NI	17	140
EDI88128CS17NB	17	140
EDI88128CS20NB	20	140
EDI88128CS25NB	25	140
EDI88128CS35NB	35	140
EDI88128CS45NB	45	140
EDI88128CS55NB	55	140
EDI88128CS15TI	15	102
EDI88128CS17TI	17	102
EDI88128CS12TB	12	102
EDI88128CS15TB	15	102
EDI88128CS17TB	17	102
EDI88128CS20TB	20	102
EDI88128CS25TB	25	102
EDI88128CS35TB	35	102
EDI88128CS45TB	45	102
EDI88128CS55TB	55	102
EDI88128CS15ZI	15	100
EDI88128CS17ZI	17	100
EDI88128CS17ZB	17	100
EDI88128CS20ZB	20	100
EDI88128CS25ZB	25	100
EDI88128CS35ZB	35	100
EDI88128CS45ZB	45	100
EDI88128CS55ZB	55	100

Part No. Low Power	Speed ns	Package No.
EDI88128LPS15CI	15	9
EDI88128LPS17CI	17	9
EDI88128LPS17CB	17	9
EDI88128LPS20CB	20	9
EDI88128LPS25CB	25	9
EDI88128LPS35CB	35	9
EDI88128LPS45CB	45	9
EDI88128LPS55CB	55	9
EDI88128LPS15FI	15	142
EDI88128LPS17FI	17	142
EDI88128LPS17FB	17	142
EDI88128LPS20FB	20	142
EDI88128LPS25FB	25	142
EDI88128LPS35FB	35	142
EDI88128LPS45FB	45	142
EDI88128LPS55FB	55	142
EDI88128LPS15LI	15	141
EDI88128LPS17LI	17	141
EDI88128LPS17LB	17	141
EDI88128LPS20LB	20	141
EDI88128LPS25LB	25	141
EDI88128LPS35LB	35	141
EDI88128LPS45LB	45	141
EDI88128LPS55LB	55	141
EDI88128LPS15NI	15	140
EDI88128LPS17NI	17	140
EDI88128LPS17NB	17	140
EDI88128LPS20NB	20	140
EDI88128LPS25NB	25	140
EDI88128LPS35NB	35	140
EDI88128LPS45NB	45	140
EDI88128LPS55NB	55	140
EDI88128LPS15TI	15	102
EDI88128LPS17TI	17	102
EDI88128LPS17TB	17	102
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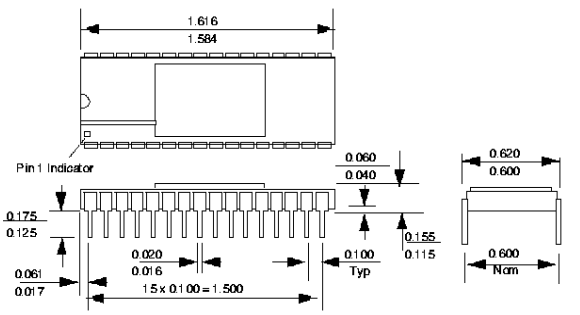
EDI88128LPS17ZI	17	100
EDI88128LPS17ZB	17	100
EDI88128LPS20ZB	20	100
EDI88128LPS25ZB	25	100
EDI88128LPS35ZB	35	100
EDI88128LPS45ZB	45	100
EDI88128LPS55ZB	55	100

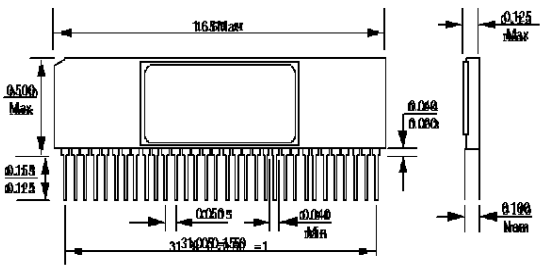
* For Commercial, Industrial or Military grade product C, I or M respectively, replaces B in part number, e.g. EDI88128CS25CB becomes EDI88128CS25CI (Industrial).

Package Description

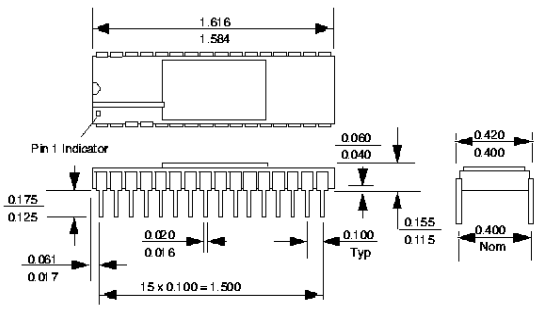
Package No. 9
32 Pin Sidebrazed Ceramic Dual-in-line Package 600 mils wide



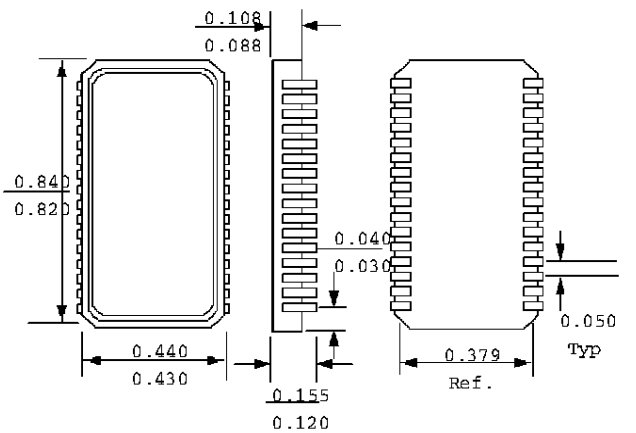
Package No. 100
32 Pin Ceramic ZIP



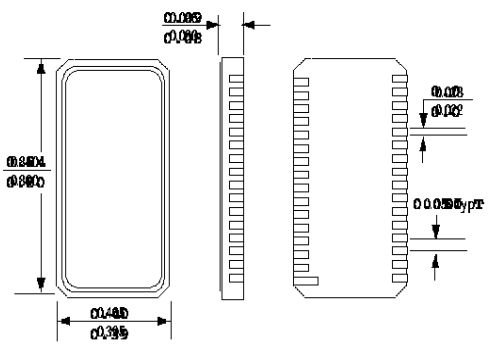
Package No. 102
32 Pin Sidebrazed Ceramic Dual-in-line-Package 400 mils wide



Package No. 140
32 Pin Ceramic SOJ
J-Leaded Package



Package No. 141
32 Pin Ceramic LCC



Package No. 142
32 Pin Ceramic Flatpack