DATA SHEET

74AC16240/74ACT16240

16-bit buffer/line driver; inverting (3-State)

Product specification

1997 Sep 15

Philips
Semiconductors

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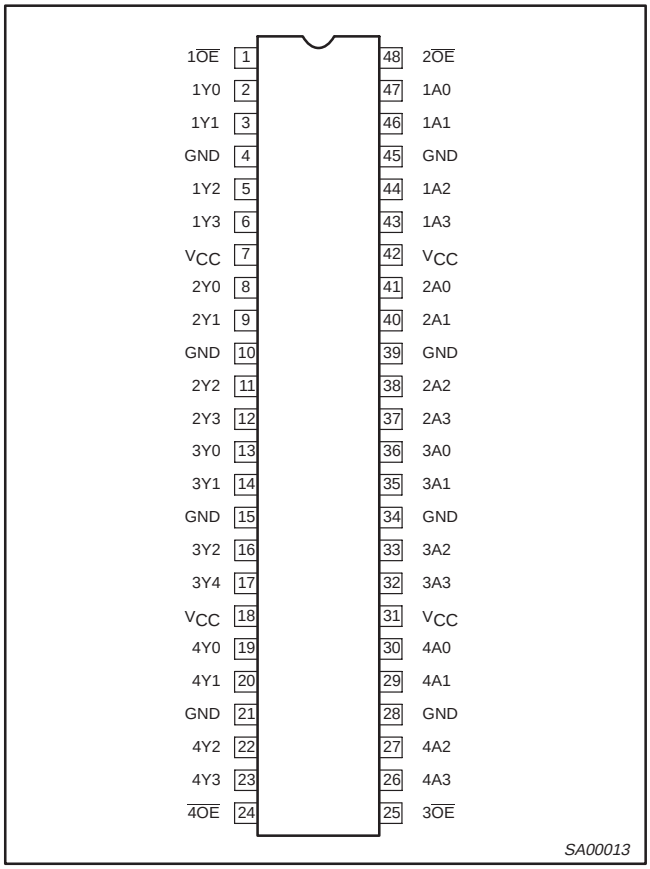
16-bit inverting buffer/line driver (3-State)

74AC16240
74ACT16240

FEATURES

- 74ACT16240 has TTL-compatible inputs
- 74AC16240 has CMOS-compatible inputs
- 3-State outputs source/sink 24mA
- 3-State outputs drive bus lines or buffer memory address registers
- Distributed power and ground pins for minimum noise and ground bounce
- Meets or exceeds JEDEC standard for 74AC(T)XX family

PIN CONFIGURATION



DESCRIPTION

The 74AC16240/74ACT16240 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an inverting 16-bit buffer that is ideal for driving bus lines. The device features four Output Enables (1$\overline{OE}$, 2$\overline{OE}$, 3$\overline{OE}$, 4$\overline{OE}$), each controlling four of the 3-State outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL			UNIT
			AC		ACT	
			V_{CC} = 3.3V	V_{CC} = 5.0V	V_{CC} = 5.0V	
t_{PHL}/t_{PLH}	Propagation delay nAx to nYx; nYx to nAx	C_L = 50pF	3.0	2.0	3.5	ns
C_I	Input capacitance		4.5			pF
C_{PD}	Power dissipation capacitance	V_I = GND to V_{CC}[1] outputs enabled outputs disabled	29 6		31 4	pF

NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW): $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF; f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74AC16240 DL 74ACT16240 DL	7AC16240 DL 7AT16240 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74AC16240 DGG 74ACT16240 DGG	7AC16240 DGG 7AT16240 DGG	SOT362-1

PIN DESCRIPTION

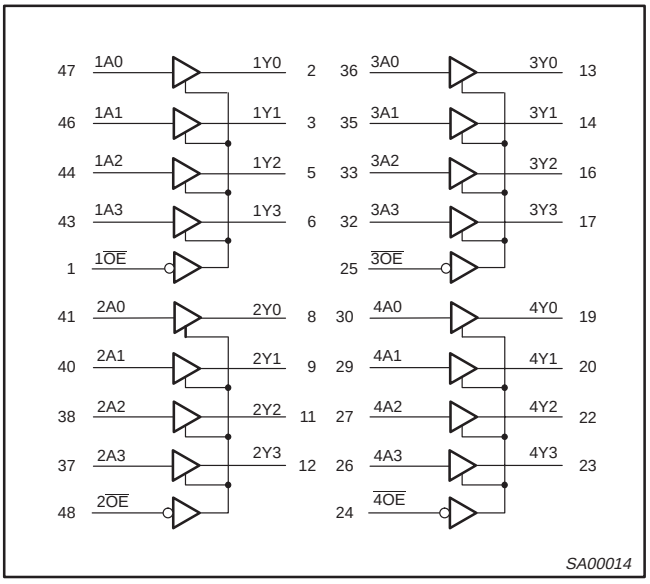
PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1A0-1A3 2A0-2A3 3A0-3A3 4A0-4A3	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1$\overline{Y}$0-1$\overline{Y}$3 2$\overline{Y}$0-2$\overline{Y}$3 3$\overline{Y}$0-3$\overline{Y}$3 4$\overline{Y}$0-4$\overline{Y}$3	Data outputs
1, 48, 25, 24	1$\overline{OE}$, 2$\overline{OE}$, 3$\overline{OE}$, 4$\overline{OE}$	Output enables
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

FUNCTION TABLE

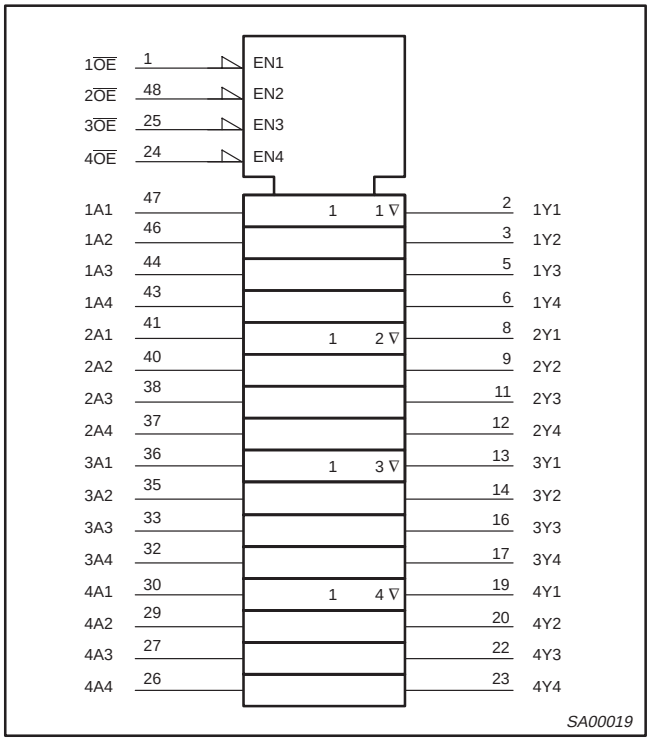
Inputs		Outputs
n$\overline{OE}$	nAx	n$\overline{Y}$x
L	L	H
L	H	L
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage for 'AC	2.0	6.0	V
V_{CC}	DC supply voltage for 'ACT	4.5	5.5	V
V_{IN}	DC input voltage range	0	V_{CC}	V
V_O	DC output voltage range	0	V_{CC}	V
T_{amb}	Operating free-air temperature range	–40	+85	°C
$\Delta V/\Delta t$	Minimum input edge rate — AC devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125		mV/ns
	— ACT devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125		

ABSOLUTE MAXIMUM RATINGS[1]

in accordance with the Absolute Maximum Rating System (IEC134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	V_{IN} = –0.5V	–20	mA
		V_{IN} = V_{CC} + 0.5V	+20	
V_{IN}	DC input voltage		–0.5 to V_{CC} +0.5	V
I_{OK}	DC output diode current	V_O = –0.5V	–20	mA
		V_O = V_{CC} + 0.5V	+20	
V_O	DC output voltage		–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current		± 50	mA
I_{CC}, I_{GND}	DC V_{CC} or GND current per output		± 50	mA
I_{CC}, I_{GND}	DC V_{CC} or GND current		± 200	mA
T_{stg}	Storage temperature range		–65 to 150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	500 500	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS FOR THE AC FAMILY

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	V_{CC} (V)	LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{OUT} = 0.1V or (V_{CC} – 0.1V)	3.0	2.1	1.5		V
			4.5	3.15	2.25		
			5.5	3.85	2.75		
V_{IL}	LOW level Input voltage	V_{OUT} = 0.1V or (V_{CC} – 0.1V)	3.0		1.5	0.9	V
			4.5		2.25	1.35	
			5.5		2.75	1.65	
V_{OH}	HIGH level output voltage	I_{OUT} = –50 μA	3.0	2.9	2.99		V
			4.5	4.4	4.49		
			5.5	5.4	5.49		
		V_{IN} = V_{IL} or V_{IH}, I_{OH} = –12mA[1]	3.0	2.46			V
		V_{IN} = V_{IL} or V_{IH}, I_{OH} = –24mA[1]	4.5	3.76			
		V_{IN} = V_{IL} or V_{IH}, I_{OH} = –24mA[1]	5.5	4.76			
V_{OL}	LOW level output voltage	I_{OUT} = 50 μA	3.0		0.01	0.1	V
			4.5		0.01	0.1	
			5.5		0.01	0.1	
		V_{IN} = V_{IL} or V_{IH}, I_{OL} = 12mA[1]	3.0			0.44	V
		V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24mA[1]	4.5			0.44	
		V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24mA[1]	5.5			0.44	
I_{IN}	Input leakage current	V_{IN} = V_{CC}, GND	5.5			±1.0	μA
I_{OZ}	3-State output OFF-state current	V_{IN} = V_{IL}, V_{IH} V_{OUT} = V_{CC}, GND	5.5			±2.5	μA
I_{OLD}	Dynamic output current[2]	V_{OLD} = 1.65V max	5.5	75			mA
I_{OHD}	Dynamic output current[2]	V_{OHD} = 3.85V min	5.5			–75	mA
I_{CC}	Quiescent supply current	V_{IN} = V_{CC} or GND	5.5			80	μA

NOTES:
1. All outputs loaded
2. Maximum test duration 2.0 ms; one output loaded at a time

DC ELECTRICAL CHARACTERISTICS FOR THE ACT FAMILY

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	V_{CC} (V)	LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{OUT} = 0.1V or (V_{CC} – 0.1V)	4.5	2.0	1.5		V
			5.5	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{OUT} = 0.1V or (V_{CC} – 0.1V)	4.5		1.5	0.8	V
			5.5		1.5	0.8	
V_{OH}	HIGH level output voltage	I_{OUT} = –50 μA	4.5	4.4	4.49		V
			5.5	5.4	5.49		
		V_{IN} = V_{IL} or V_{IH}, I_{OH} = –24mA[1]	4.5	3.76	3.86		V
		V_{IN} = V_{IL} or V_{IH}, I_{OH} = –24mA[1]	5.5	4.76	4.86		
V_{OL}	LOW level output voltage	I_{OUT} = 50 μA	4.5		0.01	0.1	V
			5.5		0.01	0.1	
		V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24mA[1]	4.5			0.44	V
		V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24mA[1]	5.5			0.44	
I_{IN}	Input leakage current	V_{IN} = V_{CC}, GND	5.5			±1.0	μA
I_{OZ}	3-State output OFF-state current	V_{IN} = V_{IL}, V_{IH} V_{OUT} = V_{CC}, GND	5.5			±2.5	μA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{IN} = V_{CC} – 2.1V Other inputs at V_{CC} or GND; I_{OUT} = 0	5.5			1.0	mA
I_{OLD}	Dynamic output current[2]	V_{OLD} = 1.65V max	5.5	75			mA
I_{OHD}	Dynamic output current[2]	V_{OHD} = 3.85V min	5.5			–75	mA
I_{CC}	Quiescent supply current	V_{IN} = V_{CC} or GND	5.5			80	μA

NOTES:
1. All outputs loaded
2. Maximum test duration 2.0ms, one output loaded at a time

AC CHARACTERISTICS FOR 74AC16240

GND = 0V; $t_r = t_f$ = 2.5ns; C_L = 50pF; R_L = 500Ω; .

SYMBOL	PARAMETER	V_{CC}[1]	LIMITS					UNIT	WAVEFORM
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C			
			MIN	TYP	MAX	MIN	MAX		
t_{PLH}	Propagation delay nAx to nYx	3.3 5.0	2.0 1.5	3.2 2.3	85.5	1.5 1.0	9 6	ns	1
t_{PHL}	Propagation delay nAx to nYx	3.3 5.0	2.0 1.5	2.7 1.9	8 5.5	1.5 1.0	9 6	ns	1
t_{PZH}	3-State output enable time $\overline{OE}$ to nAx	3.3 5.0	2.0 1.5	4.1 2.8	9.5 6.5	1.5 1.0	11 7.5	ns	2
t_{PZL}	3-State output enable time $\overline{OE}$ to nAx	3.3 5.0	2.0 1.5	4.0 2.7	9.5 6.5	1.5 1.0	11 7.5	ns	2
t_{PHZ}	3-State output disable time $\overline{OE}$ to nAx	3.3 5.0	2.0 1.5	3.3 2.3	9 6	1.5 1.0	10 7	ns	2
t_{PLZ}	3-State output disable time $\overline{OE}$ to nAx	3.3 5.0	2.0 1.5	3.9 2.7	9 6	1.5 1.0	10 7	ns	2

NOTE:
1. Voltage range 3.3V is V_{CC} = 3.3V ± 0.3V
   Voltage range 5.0V is V_{CC} = 5.0V ± 0.5V

AC CHARACTERISTICS FOR 74ACT16240

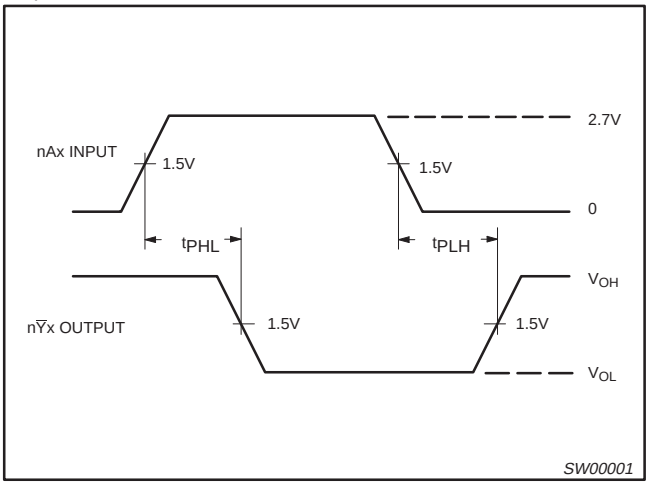
GND = 0V; $t_r = t_f$ = 2.5ns; C_L = 50pF; R_L = 500Ω; .

SYMBOL	PARAMETER	V_{CC}[1]	LIMITS					UNIT	WAVEFORM
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C			
			MIN	TYP	MAX	MIN	MAX		
t_{PLH}	Propagation delay nAx to nYx	5.0	1.5	3.5	8	1.0	9	ns	1
t_{PHL}	Propagation delay nAx to nYx	5.0	1.5	3.5	8	1.0	9	ns	1
t_{PZH}	3-State output enable time $\overline{OE}$ to nAx	5.0	1.5	4.1	8	1.0	9	ns	2
t_{PZL}	3-State output enable time $\overline{OE}$ to nAx	5.0	1.5	4.1	8	1.0	9	ns	2
t_{PHZ}	3-State output disable time $\overline{OE}$ to nAx	5.0	1.5	3.9	7.5	1.0	8.5	ns	2
t_{PLZ}	3-State output disable time $\overline{OE}$ to nAx	5.0	1.5	4.3	7.5	1.0	8.5	ns	2

NOTE:
1. Voltage range 5.0V is V_{CC} = 5.0V ± 0.5V

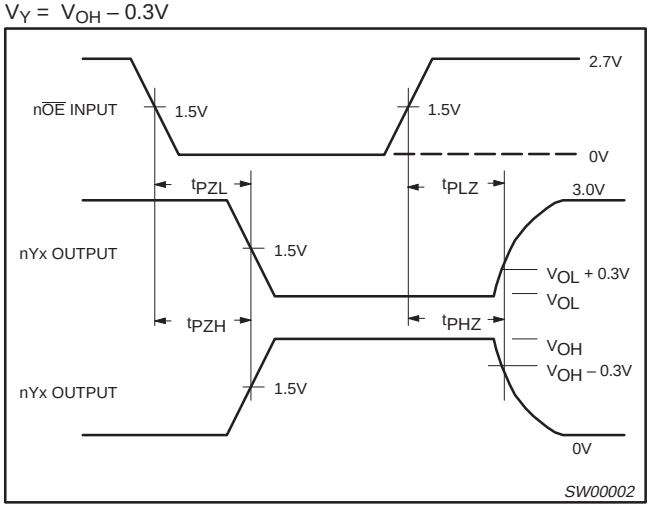
AC WAVEFORMS

V_m = 50% V_{CC} for 'AC devices; 1.5V for 'ACT devices
V_m = 50% V_{CC} for 'AC/'ACT devices
V_{OL} and V_{OH} are the typical output voltage drops that occur with the output load.



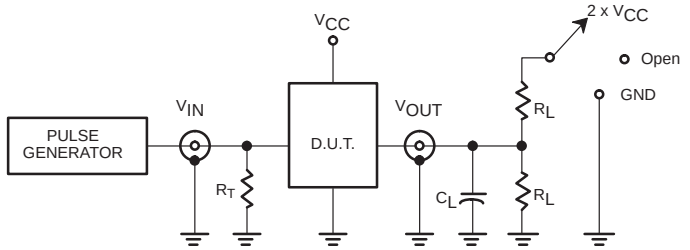
Waveform 1. Input (nAx) to Output (nȲx) Propagation Delays

$V_X = V_{OL} + 0.3V$
$V_Y = V_{OH} – 0.3V$



Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

FAMILY	V_{IN} Input Requirements	V_m Input	V_m Output
AC	GND to V_{CC}	50% V_{CC}	50% V_{CC}
ACT	GND to 3.0V	1.5V	50% V_{CC}

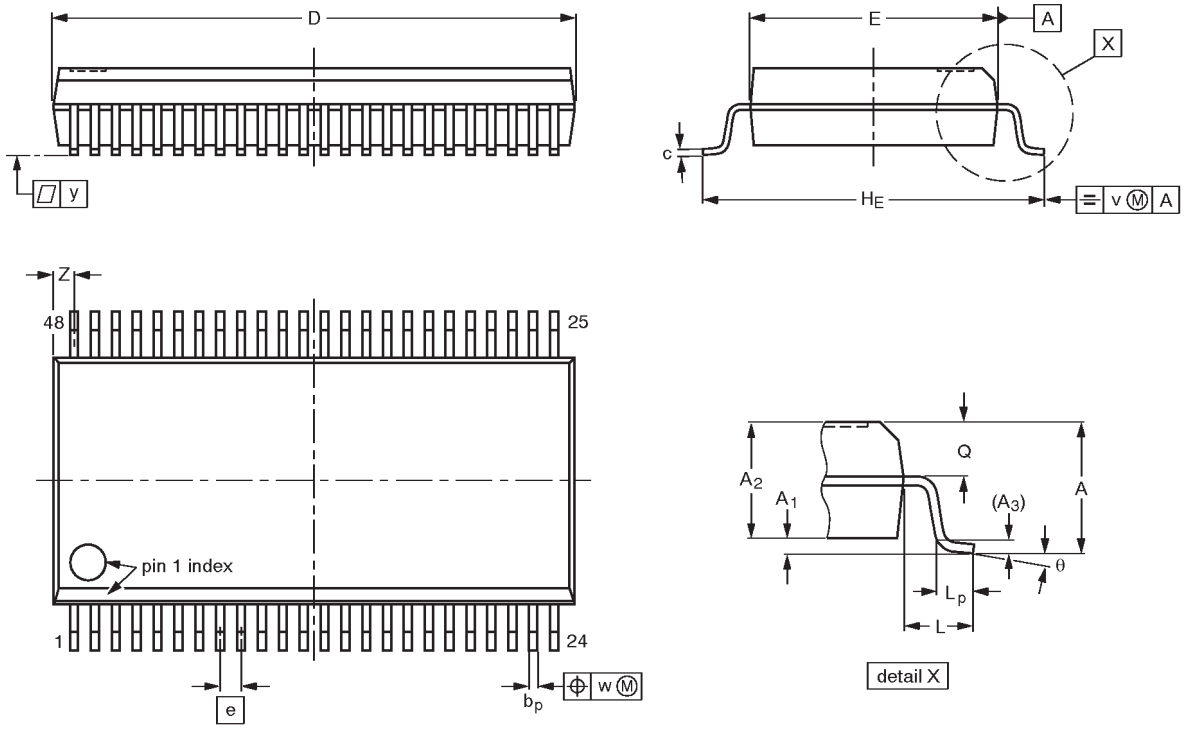
DEFINITIONS

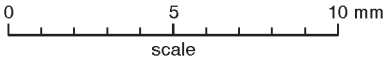
R_L = Load resistor; see AC Characteristics for value.
C_L = Load capacitance, see AC characteristics
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SV00302

Waveform 3. Load circuitry for switching times.

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm **SOT370-1**





DIMENSIONS (mm are the original dimensions)

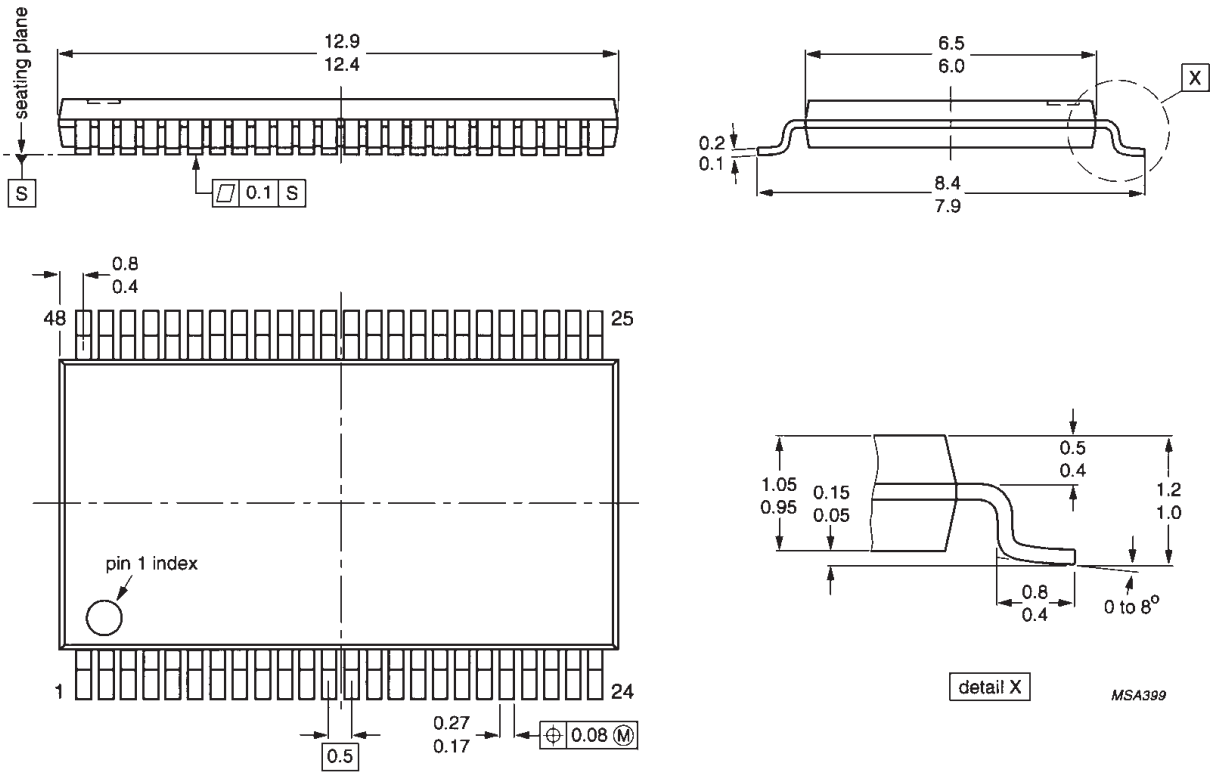
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118AA				~~93-11-02~~ 95-02-04

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm **SOT362-1**



Dimensions in mm.

NOTES

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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