

1.4 MHz, Low Power General Purpose, 1.8V Operational Amplifiers

General Description

The LMV611/LMV612/LMV614 are single, dual, and quad low voltage, low power Operational Amplifiers. They are designed specifically for low voltage general purpose applications. Other important product characteristics are, rail-to-rail input/output, low supply voltage of 1.8V and wide temperature range. The LMV611/LMV612/LMV614 input common mode extends 200mV beyond the supplies and the output can swing rail-to-rail unloaded and within 30mV with 2kohm load at 1.8V supply. The LMV611/2/4 achieves a gain bandwidth of 1.4MHz while drawing 100 uA (typ) quiescent current.

The industrial-plus temperature range of -40°C to 125°C allows the LMV611/LMV612/LMV614 to accommodate a broad range of extended environment applications.

The LMV611 is offered in the tiny 5-Pin SC70 package, the LMV612 in space saving 8-Pin MSOP and SOIC, and the LMV614 in 14-Pin TSSOP and SOIC. These small package amplifiers offer an ideal solution for applications requiring minimum PCB footprint. Applications with area constrained PC board requirements include portable and battery operated electronics.

Features

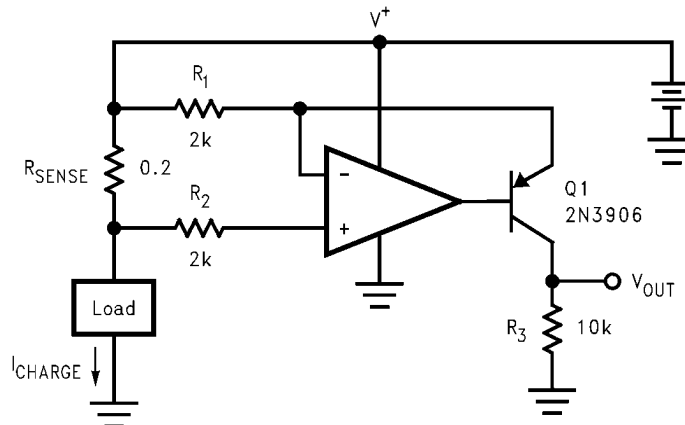
(Typical 1.8V Supply Values; Unless Otherwise Noted)

- Guaranteed 1.8V, 2.7V and 5V specifications
- Output swing
 - w/600Ω load 80mV from rail
 - w/2kΩ load 30mV from rail
- V_{CM} 200mV beyond rails
- Supply current (per channel) 100μA
- Gain bandwidth product 1.4MHz
- Maximum V_{OS} 4.0mV
- Temperature range -40°C to 125°C

Applications

- Consumer communication
- Consumer computing
- PDAs
- Audio pre-amp
- Portable/battery-powered electronic equipment
- Supply current monitoring
- Battery monitoring

Typical Application



$$V_{\text{OUT}} = \frac{R_{\text{SENSE}} \cdot R_3}{R_1} \cdot I_{\text{Charge}} = 1\Omega \cdot I_{\text{Charge}}$$

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Machine Model	200V
Human Body Model	2000V
Supply Voltage (V ⁺ -V ⁻)	6V
Differential Input Voltage	± Supply Voltage
Voltage at Input/Output Pins	V ⁺ +0.3V, V ⁻ -0.3V
Storage Temperature Range	-65°C to 150°C
Junction Temperature (Note 4)	150°C

For soldering specifications:

see product folder at www.national.com and
www.national.com/ms/MS/MS-SOLDERING.pdf

Operating Ratings (Note 1)

Supply Voltage Range	1.8V to 5.5V
Temperature Range	-40°C to 125°C
Thermal Resistance (θ _{JA})	
5-Pin SC70	414°C/W
5-Pin SOT23	265°C/W
8-Pin MSOP	235°C/W
8-Pin SOIC	175°C/W
14-Pin TSSOP	155°C/W
14-Pin SOIC	127°C/W

1.8V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V⁺ = 1.8V, V⁻ = 0V, V_{CM} = V⁺/2, V_O = V⁺/2 and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes. See (Note 10)

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units	
V _{OS}	Input Offset Voltage	LMV611 (Single)		1	4	mV	
		LMV612 (Dual) LMV614 (Quad)		1	5.5	mV	
TCV _{OS}	Input Offset Voltage Average Drift			5.5		μV/°C	
I _B	Input Bias Current			15		nA	
I _{OS}	Input Offset Current			13		nA	
I _S	Supply Current (per channel)			103	185	μA	
CMRR	Common Mode Rejection Ratio	LMV611, 0 ≤ V _{CM} ≤ 0.6V 1.4V ≤ V _{CM} ≤ 1.8V (Note 8)	60	78		dB	
		LMV612 and LMV614 0 ≤ V _{CM} ≤ 0.6V 1.4V ≤ V _{CM} ≤ 1.8V (Note 8)	55	76			
		-0.2V ≤ V _{CM} ≤ 0V 1.8V ≤ V _{CM} ≤ 2.0V	50	72			
PSRR	Power Supply Rejection Ratio	1.8V ≤ V ⁺ ≤ 5V		100		dB	
CMVR	Input Common-Mode Voltage Range	For CMRR Range ≥ 50dB	T _A = 25°C	V ⁻ -0.2	-0.2 to 2.1	V ⁺ +0.2	V
			T _A = -40°C to 85°C	V ⁻		V ⁺	
			T _A = 125°C	V ⁻ +0.2		V ⁺ -0.2	
A _V	Large Signal Voltage Gain LMV611 (Single)	R _L = 600Ω to 0.9V, V _O = 0.2V to 1.6V, V _{CM} = 0.5V	77	101		dB	
		R _L = 2kΩ to 0.9V, V _O = 0.2V to 1.6V, V _{CM} = 0.5V	80	105			
	Large Signal Voltage Gain LMV612 (Dual) LMV614 (Quad)	R _L = 600Ω to 0.9V, V _O = 0.2V to 1.6V, V _{CM} = 0.5V	75	90		dB	
		R _L = 2kΩ to 0.9V, V _O = 0.2V to 1.6V, V _{CM} = 0.5V	78	100			
V _O	Output Swing	R _L = 600Ω to 0.9V V _{IN} = ±100mV	1.65	1.72	0.105	V	
		R _L = 2kΩ to 0.9V V _{IN} = ±100mV	1.75	1.77	0.035		
		R _L = 600Ω to 0.9V V _{IN} = ±100mV		0.077	0.024		

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
I_O	Output Short Circuit Current (Note 3)	Sourcing, $V_O = 0V$ $V_{IN} = 100mV$		8		mA
		Sinking, $V_O = 1.8V$ $V_{IN} = -100mV$		9		

1.8V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ C$. $V^+ = 1.8V$, $V^- = 0V$, $V_{CM} = V^+/2$, $V_O = V^+/2$ and $R_L > 1 M\Omega$.

Boldface limits apply at the temperature extremes. See (Note 10)

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
SR	Slew Rate	(Note 7)		0.35		V/ μs
GBW	Gain-Bandwidth Product			1.4		MHz
ϕ_m	Phase Margin			67		deg
G_m	Gain Margin			7		dB
e_n	Input-Referred Voltage Noise	$f = 10 \text{ kHz}$, $V_{CM} = 0.5V$		60		$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	$f = 10 \text{ kHz}$		0.08		$\frac{pA}{\sqrt{Hz}}$
THD	Total Harmonic Distortion	$f = 1kHz$, $A_V = +1$ $R_L = 600\Omega$, $V_{IN} = 1 V_{PP}$		0.023		%
	Amp-to-Amp Isolation	(Note 9)		123		dB

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. $V^+ = 2.7\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V^+/2$, $V_O = V^+/2$ and $R_L > 1\text{ M}\Omega$. **Boldface** limits apply at the temperature extremes. See (Note 10)

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units	
V_{OS}	Input Offset Voltage	LMV611 (Single)		1	4	mV	
		LMV612 (Dual) LMV614 (Quad)		1	5.5	mV	
TCV_{OS}	Input Offset Voltage Average Drift			5.5		$\mu\text{V}/^\circ\text{C}$	
I_{B}	Input Bias Current			15		nA	
I_{OS}	Input Offset Current			8		nA	
I_{S}	Supply Current (per channel)			105	190	μA	
CMRR	Common Mode Rejection Ratio	LMV611, $0 \leq V_{\text{CM}} \leq 1.5\text{V}$ $2.3\text{V} \leq V_{\text{CM}} \leq 2.7\text{V}$ (Note 8)	60	81		dB	
		LMV612 and LMV614 $0 \leq V_{\text{CM}} \leq 1.5\text{V}$ $2.3\text{V} \leq V_{\text{CM}} \leq 2.7\text{V}$ (Note 8)	55	80			
		$-0.2\text{V} \leq V_{\text{CM}} \leq 0\text{V}$ $2.7\text{V} \leq V_{\text{CM}} \leq 2.9\text{V}$	50	74			
PSRR	Power Supply Rejection Ratio	$1.8\text{V} \leq V^+ \leq 5\text{V}$ $V_{\text{CM}} = 0.5\text{V}$		100		dB	
V_{CM}	Input Common-Mode Voltage Range	For CMRR Range $\geq 50\text{dB}$	$T_A = 25^\circ\text{C}$	$V^- - 0.2$	-0.2 to 3.0	$V^+ + 0.2$	V
			$T_A = -40^\circ\text{C}$ to 85°C	V^-		V^+	
			$T_A = 125^\circ\text{C}$	$V^- + 0.2$		$V^+ - 0.2$	
A_V	Large Signal Voltage Gain LMV611 (Single)	$R_L = 600\Omega$ to 1.35V , $V_O = 0.2\text{V}$ to 2.5V	87	104		dB	
		$R_L = 2\text{k}\Omega$ to 1.35V , $V_O = 0.2\text{V}$ to 2.5V	92	110			
	Large Signal Voltage Gain LMV612 (Dual) LMV614 (Quad)	$R_L = 600\Omega$ to 1.35V , $V_O = 0.2\text{V}$ to 2.5V	78	90		dB	
		$R_L = 2\text{k}\Omega$ to 1.35V , $V_O = 0.2\text{V}$ to 2.5V	81	100			
V_O	Output Swing	$R_L = 600\Omega$ to 1.35V $V_{\text{IN}} = \pm 100\text{mV}$		2.55	2.62		V
						0.083	
		$R_L = 2\text{k}\Omega$ to 1.35V $V_{\text{IN}} = \pm 100\text{mV}$		2.65	2.675		
					0.025	0.04	
I_O	Output Short Circuit Current (Note 3)	Sourcing, $V_O = 0\text{V}$ $V_{\text{IN}} = 100\text{mV}$		30		mA	
		Sinking, $V_O = 0\text{V}$ $V_{\text{IN}} = -100\text{mV}$		25			

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. $V^+ = 2.7\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = 1.0\text{V}$, $V_O = 1.35\text{V}$ and $R_L > 1\text{ M}\Omega$.

Boldface limits apply at the temperature extremes. See (Note 10)

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
SR	Slew Rate	(Note 7)		0.4		V/ μs
GBW	Gain-Bandwidth Product			1.4		MHz
Φ_m	Phase Margin			70		deg
G_m	Gain Margin			7.5		dB
e_n	Input-Referred Voltage Noise	$f = 10\text{ kHz}$, $V_{\text{CM}} = 0.5\text{V}$		57		$\frac{\text{nV}}{\sqrt{\text{Hz}}}$
i_n	Input-Referred Current Noise	$f = 10\text{ kHz}$		0.08		$\frac{\text{pA}}{\sqrt{\text{Hz}}}$
THD	Total Harmonic Distortion	$f = 1\text{ kHz}$, $A_V = +1$ $R_L = 600\Omega$, $V_{\text{IN}} = 1V_{\text{PP}}$		0.022		%
	Amp-to-Amp Isolation	(Note 9)		123		dB

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V^+/2$, $V_O = V^+/2$ and $R_L > 1\text{M}\Omega$. **Boldface** limits apply at the temperature extremes. See (Note 10)

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units	
V_{OS}	Input Offset Voltage	LMV611 (Single)		1	4	mV	
		LMV612 (Dual) LMV614 (Quad)		1	5.5	mV	
TCV_{OS}	Input Offset Voltage Average Drift			5.5		$\mu\text{V}/^\circ\text{C}$	
I_{B}	Input Bias Current			14	35	nA	
I_{OS}	Input Offset Current			9		nA	
I_{S}	Supply Current (per channel)			116	210	μA	
CMRR	Common Mode Rejection Ratio	$0 \leq V_{\text{CM}} \leq 3.8\text{V}$	60	86		dB	
		$4.6\text{V} \leq V_{\text{CM}} \leq 5.0\text{V}$ (Note 8)					
		$-0.2\text{V} \leq V_{\text{CM}} \leq 0\text{V}$ $5.0\text{V} \leq V_{\text{CM}} \leq 5.2\text{V}$	50	78			
PSRR	Power Supply Rejection Ratio	$1.8\text{V} \leq V^+ \leq 5\text{V}$ $V_{\text{CM}} = 0.5\text{V}$		100		dB	
CMVR	Input Common-Mode Voltage Range	For CMRR Range $\geq 50\text{dB}$	$T_A = 25^\circ\text{C}$	V- -0.2	-0.2 to 5.3	V+ +0.2	V
			$T_A = -40^\circ\text{C}$ to 85°C	V-		V+	
			$T_A = 125^\circ\text{C}$	V- +0.3		V+ -0.3	
A_V	Large Signal Voltage Gain LMV611 (Single)	$R_L = 600\Omega$ to 2.5V, $V_O = 0.2\text{V}$ to 4.8V	88	102		dB	
		$R_L = 2\text{k}\Omega$ to 2.5V, $V_O = 0.2\text{V}$ to 4.8V	94	113			
	Large Signal Voltage Gain LMV612 (Dual) LMV614 (Quad)	$R_L = 600\Omega$ to 2.5V, $V_O = 0.2\text{V}$ to 4.8V	81	90		dB	
		$R_L = 2\text{k}\Omega$ to 2.5V, $V_O = 0.2\text{V}$ to 4.8V	85	100			
V_O	Output Swing	$R_L = 600\Omega$ to 2.5V $V_{\text{IN}} = \pm 100\text{mV}$	4.855	4.890		V	
		$R_L = 2\text{k}\Omega$ to 2.5V $V_{\text{IN}} = \pm 100\text{mV}$	4.945	4.967	0.160		
				0.037	0.065		
I_O	Output Short Circuit Current (Note 3)	LMV611, Sourcing, $V_O = 0\text{V}$ $V_{\text{IN}} = 100\text{mV}$		100		mA	
		Sinking, $V_O = 5\text{V}$ $V_{\text{IN}} = -100\text{mV}$		65			

5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V^+/2$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}\Omega$. **Boldface** limits apply at the temperature extremes. See (Note 10)

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
SR	Slew Rate	(Note 7)		0.42		V/ μs
GBW	Gain-Bandwidth Product			1.5		MHz
Φ_m	Phase Margin			71		deg
G_m	Gain Margin			8		dB

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
e_n	Input-Referred Voltage Noise	$f = 10 \text{ kHz}$, $V_{CM} = 1V$		50		$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	$f = 10 \text{ kHz}$		0.08		$\frac{pA}{\sqrt{Hz}}$
THD	Total Harmonic Distortion	$f = 1\text{kHz}$, $A_V = +1$ $R_L = 600\Omega$, $V_O = 1V_{PP}$		0.022		%
	Amp-to-Amp Isolation	(Note 9)		123		dB

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC). Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Note 5: Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

Note 6: All limits are guaranteed by testing or statistical analysis.

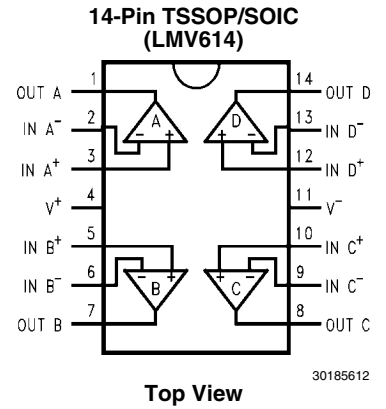
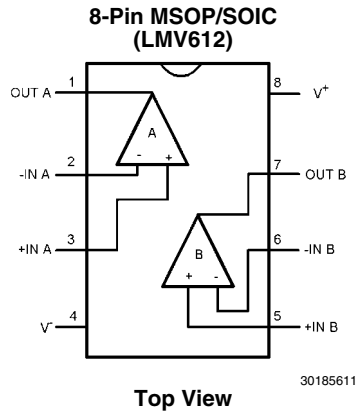
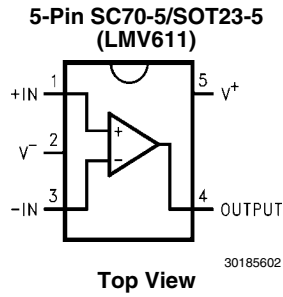
Note 7: Connected as voltage follower with input step from V^- to V^+ . Number specified is the slower of the positive and negative slew rates.

Note 8: For guaranteed temperature ranges, see Input Common-Mode Voltage Range specifications.

Note 9: Input referred, $R_L = 100k\Omega$ connected to $V+/2$. Each amp excited in turn with 1kHz to produce $V_O = 3V_{PP}$ (For Supply Voltages $<3V$, $V_O = V^+$).

Note 10: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. See Applications section for information of temperature derating of the device. Absolute Maximum Ratings indicated junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

Connection Diagrams



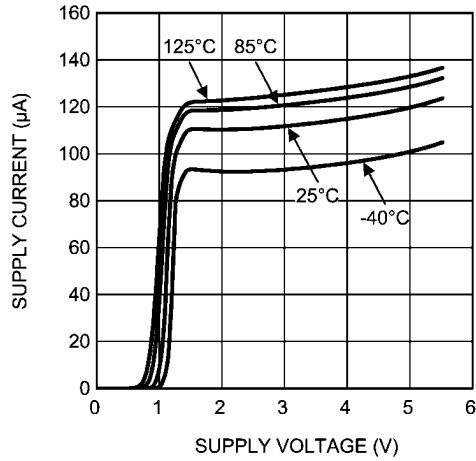
Ordering Information

Package	Part Number	Packaging Marking	Transport Media	NSC Drawing
5-Pin SC70	LMV611MG	AVA	1k Units Tape and Reel	MAA05A
	LMV611MGX		3k Units Tape and Reel	
5-Pin SOT23	LMV611MF	AE9A	1k Units Tape and Reel	MF05A
	LMV611MFX		3k Units Tape and Reel	
8-Pin MSOP	LMV612MM	AD9A	1k Units Tape and Reel	MUA08A
	LMV612MMX		3.5k Units Tape and Reel	
8-Pin SOIC	LMV612MA	LMV612MA	Rails	M08A
	LMV612MAX		2.5k Units Tape and Reel	
14-Pin TSSOP	LMV614MT	LMV614MT	Rails	MTC14
	LMV614MTX		2.5k Units Tape and Reel	
14-Pin SOIC	LMV614MA	LMV614MA	Rails	M14A
	LMV614MAX		2.5k Units Tape and Reel	

Typical Performance Characteristics

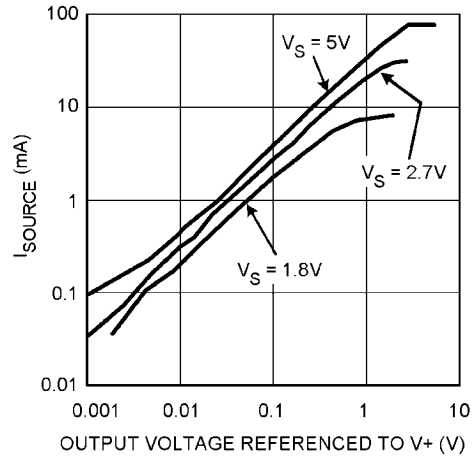
Unless otherwise specified, $V_S = +5V$, single supply, $T_A = 25^\circ C$.

Supply Current vs. Supply Voltage (LMV611)



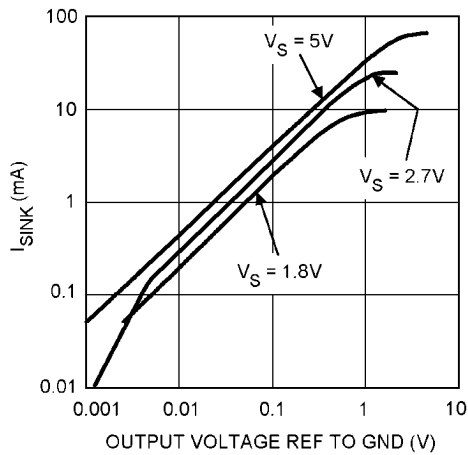
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Sourcing Current vs. Output Voltage



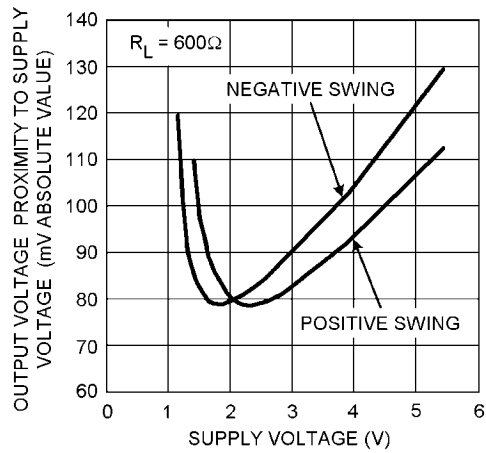
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Sinking Current vs. Output Voltage



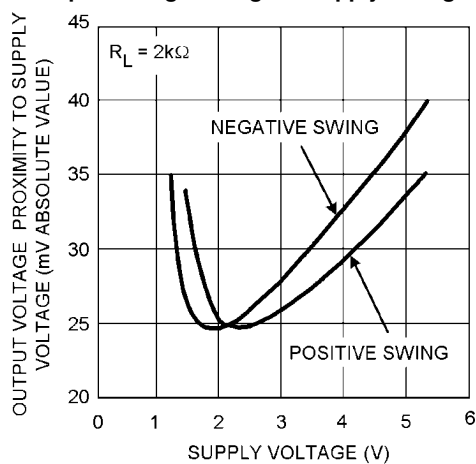
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Output Voltage Swing vs. Supply Voltage



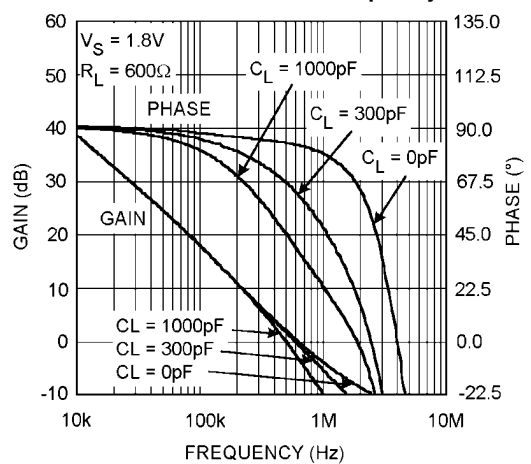
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Output Voltage Swing vs. Supply Voltage

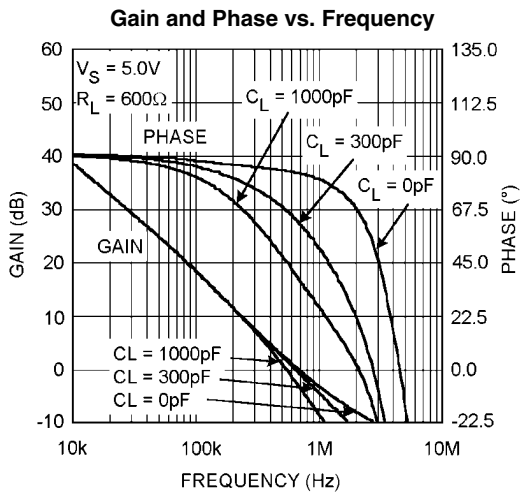


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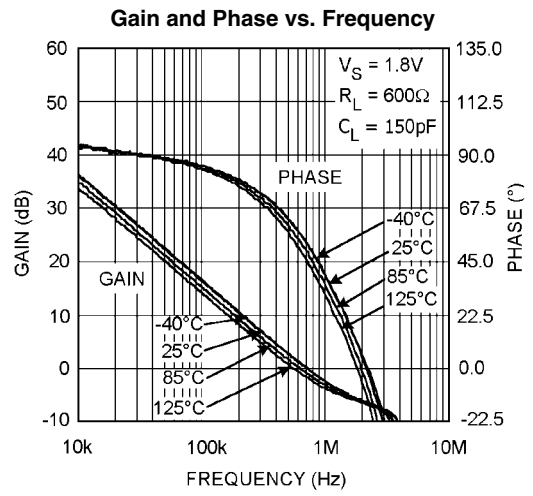
Gain and Phase vs. Frequency



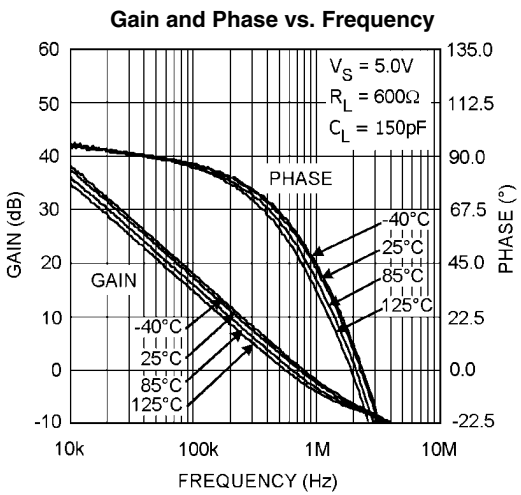
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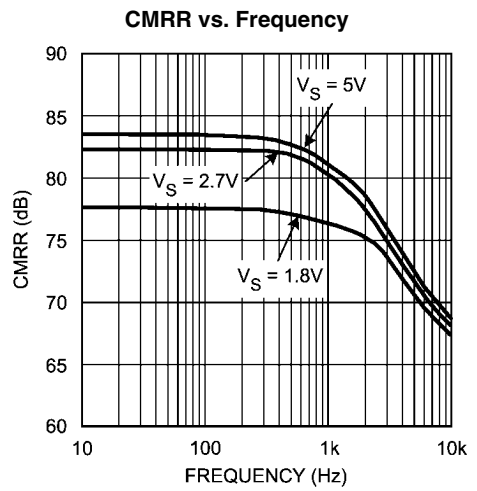
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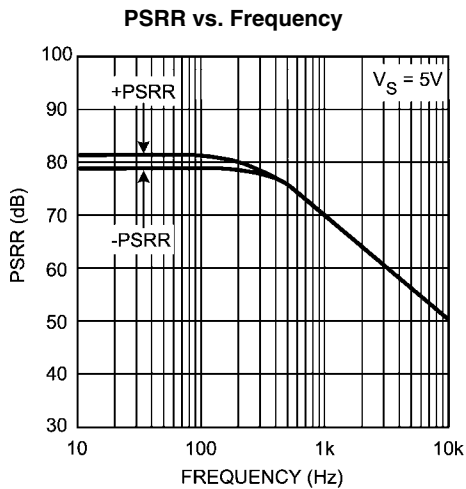
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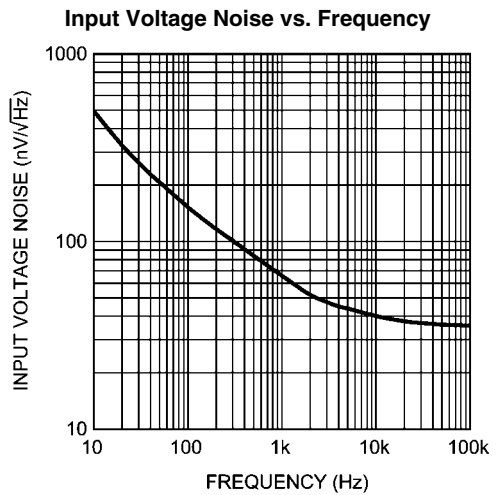
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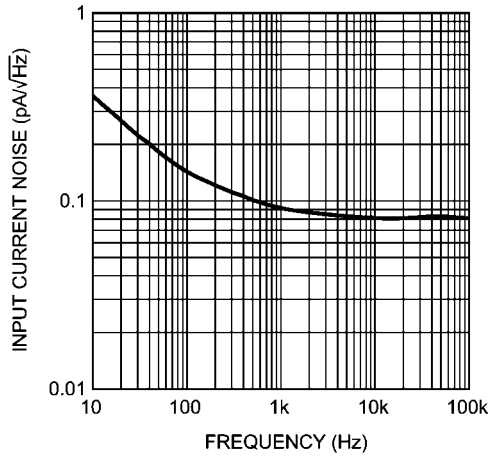


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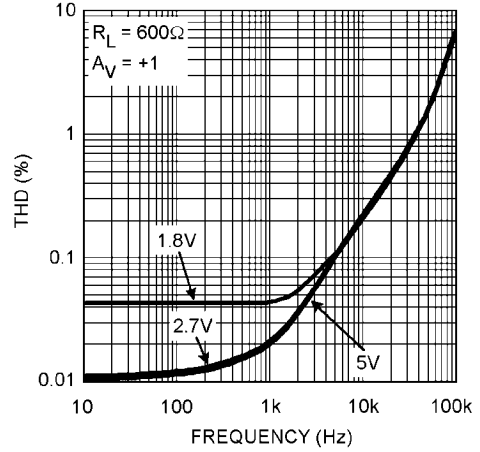
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Input Current Noise vs. Frequency



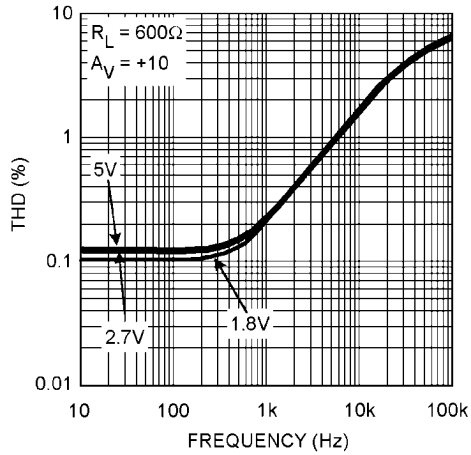
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THD vs. Frequency



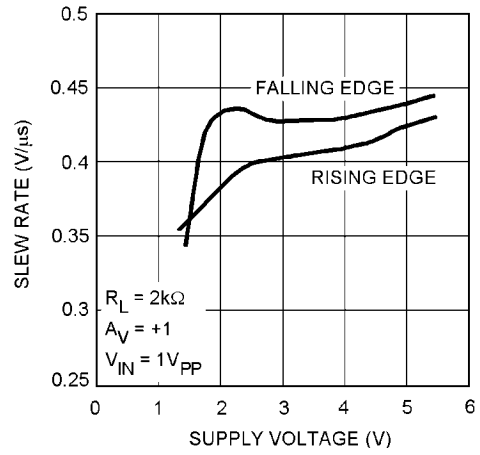
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THD vs. Frequency



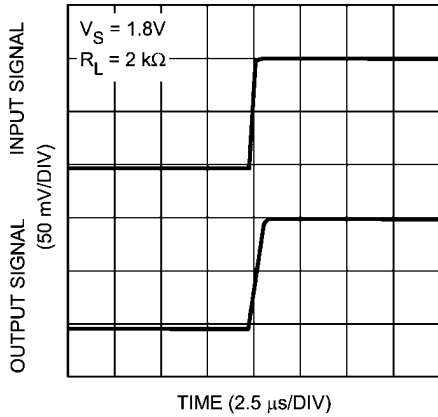
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Slew Rate vs. Supply Voltage



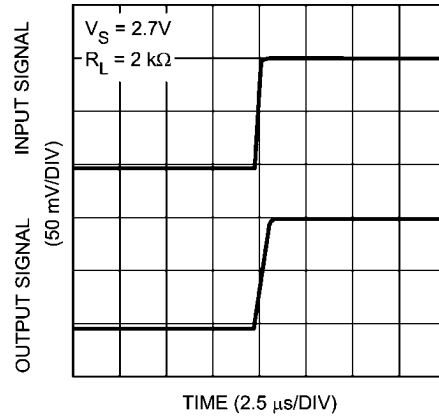
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Small Signal Non-Inverting Response



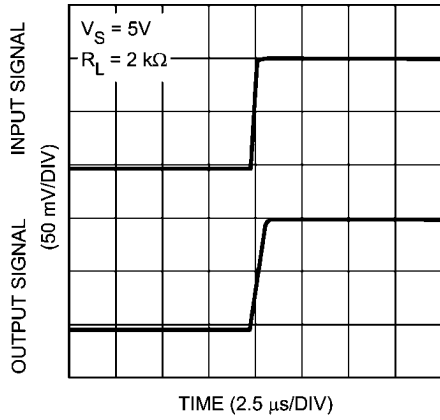
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Small Signal Non-Inverting Response



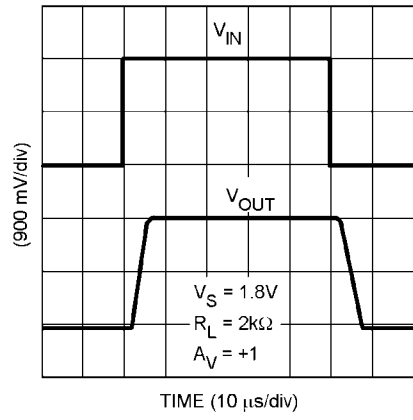
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Small Signal Non-Inverting Response



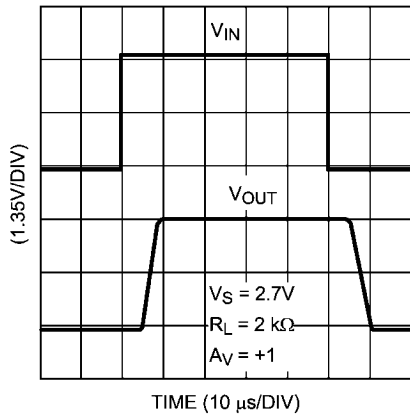
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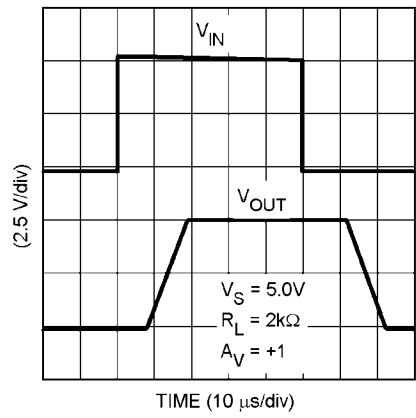
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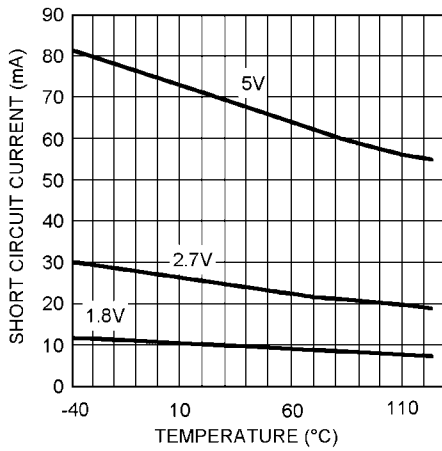
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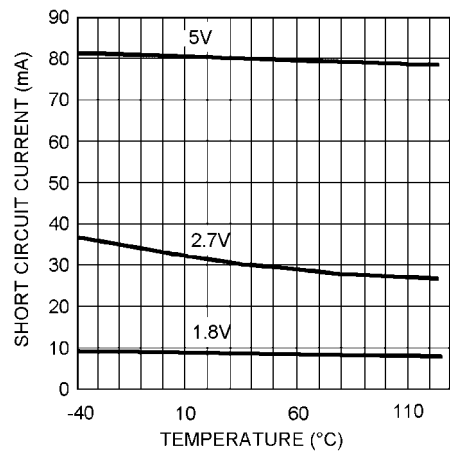
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Short Circuit Current vs. Temperature (Sinking)



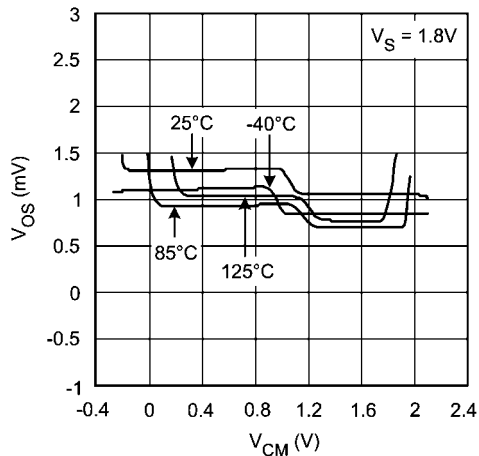
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Short Circuit Current vs. Temperature (Sourcing)



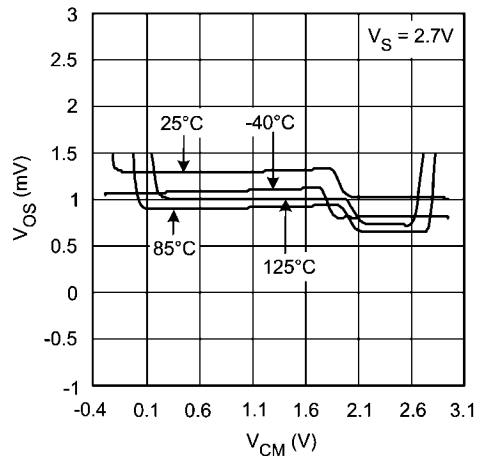
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Offset Voltage vs. Common Mode Range



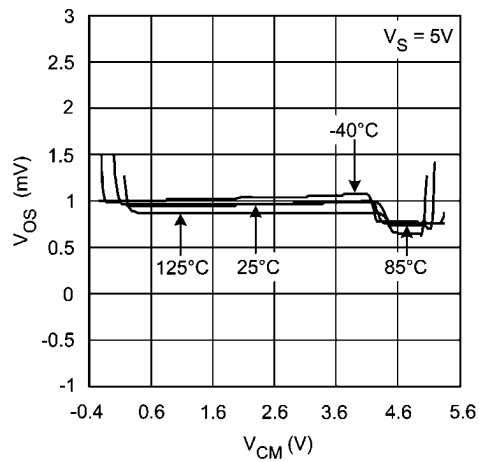
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Offset Voltage vs. Common Mode Range



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Offset Voltage vs. Common Mode Range



30185638

Application Note

INPUT AND OUTPUT STAGE

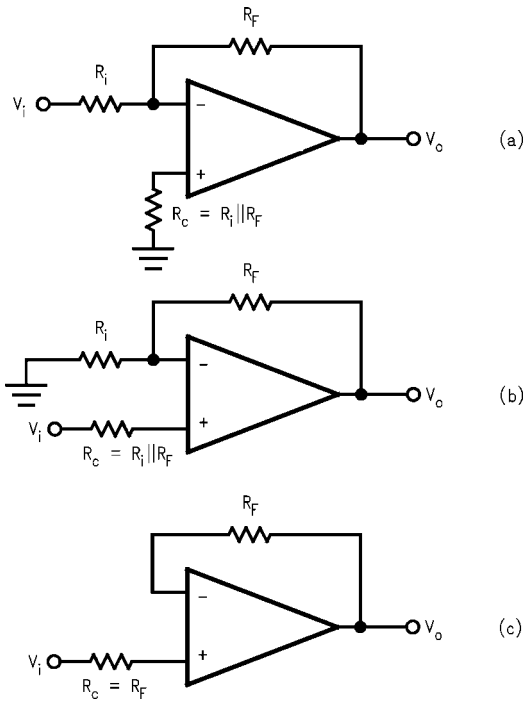
The rail-to-rail input stage of this family provides more flexibility for the designer. The LMV611/LMV612/LMV614 use a complimentary PNP and NPN input stage in which the PNP stage senses common mode voltage near V^- and the NPN stage senses common mode voltage near V^+ . The transition from the PNP stage to NPN stage occurs 1V below V^+ . Since both input stages have their own offset voltage, the offset of the amplifier becomes a function of the input common mode voltage and has a crossover point at 1V below V^+ .

This V_{OS} crossover point can create problems for both DC and AC coupled signals if proper care is not taken. Large input signals that include the V_{OS} crossover point will cause distortion in the output signal. One way to avoid such distortion is to keep the signal away from the crossover. For example, in a unity gain buffer configuration and with $V_S = 5V$, a 5V peak-to-peak signal will contain input-crossover distortion while a 3V peak-to-peak signal centered at 1.5V will not contain input-crossover distortion as it avoids the crossover point. Another way to avoid large signal distortion is to use a gain of -1 circuit which avoids any voltage excursions at the input terminals of the amplifier. In that circuit, the common mode DC voltage can be set at a level away from the V_{OS} cross-over point. For small signals, this transition in V_{OS} shows up as a V_{CM} de-

pendent spurious signal in series with the input signal and can effectively degrade small signal parameters such as gain and common mode rejection ratio. To resolve this problem, the small signal should be placed such that it avoids the V_{OS} crossover point. In addition to the rail-to-rail performance, the output stage can provide enough output current to drive 600Ω loads. Because of the high current capability, care should be taken not to exceed the $150^\circ C$ maximum junction temperature specification.

INPUT BIAS CURRENT CONSIDERATION

The LMV611/LMV612/LMV614 family has a complementary bipolar input stage. The typical input bias current (I_B) is 15nA. The input bias current can develop a significant offset voltage. This offset is primarily due to I_B flowing through the negative feedback resistor, R_F . For example, if I_B is 50nA and R_F is $100k\Omega$, then an offset voltage of 5mV will develop ($V_{OS} = I_B \times R_F$). Using a compensation resistor (R_C), as shown in [Figure 1](#), cancels this effect. But the input offset current (I_{OS}) will still contribute to an offset voltage in the same manner.



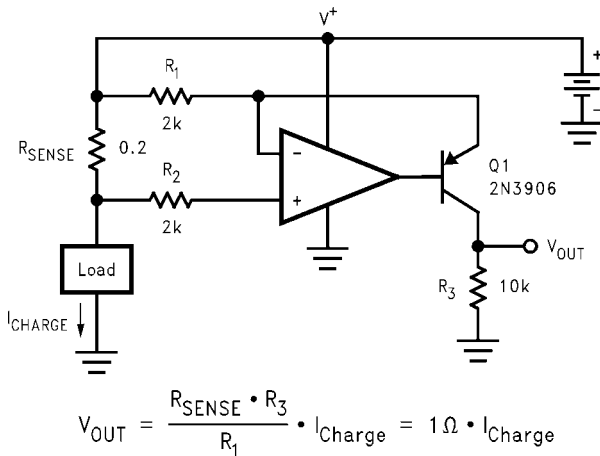
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FIGURE 1. Canceling the Offset Voltage due to Input Bias Current

Typical Applications

HIGH SIDE CURRENT SENSING

The high side current sensing circuit (Figure 2) is commonly used in a battery charger to monitor charging current to prevent over charging. A sense resistor R_{SENSE} is connected to the battery directly. This system requires an op amp with rail-to-rail input. The LMV611/LMV612/LMV614 are ideal for this application because its common mode input range goes up to the rail.



30185616

FIGURE 2. High Side Current Sensing

HALF-WAVE RECTIFIER WITH RAIL-TO-GROUND OUTPUT SWING

Since the LMV611/LMV612/LMV614 input common mode range includes both positive and negative supply rails and the output can also swing to either supply, achieving half-wave rectifier functions in either direction is an easy task. All that is needed are two external resistors; there is no need for diodes or matched resistors. The half wave rectifier can have either positive or negative going outputs, depending on the way the circuit is arranged.

In Figure 3 the circuit is referenced to ground, while in Figure 4 the circuit is biased to the positive supply. These configurations implement the half wave rectifier since the LMV611/LMV612/LMV614 can not respond to one-half of the incoming waveform. It can not respond to one-half of the incoming because the amplifier can not swing the output beyond either rail therefore the output disengages during this half cycle. During the other half cycle, however, the amplifier achieves a half wave that can have a peak equal to the total supply voltage. R_1 should be large enough not to load the LMV611/LMV612/LMV614.

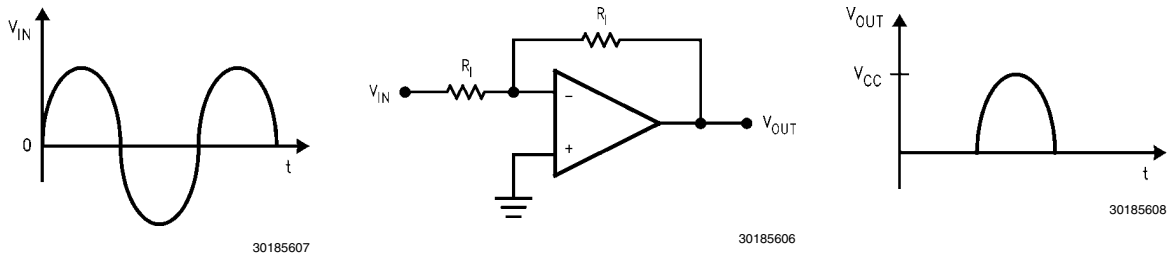


FIGURE 3. Half-Wave Rectifier with Rail-To-Ground Output Swing Referenced to Ground

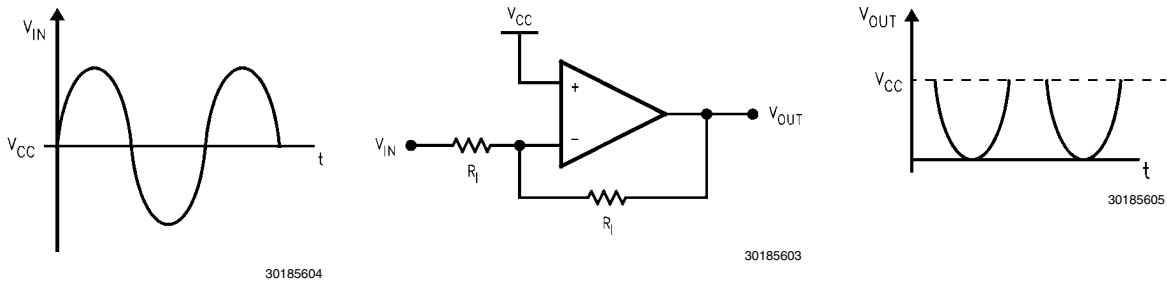


FIGURE 4. Half-Wave Rectifier with Negative-Going Output Referenced to V_{CC}

INSTRUMENTATION AMPLIFIER WITH RAIL-TO-RAIL INPUT AND OUTPUT

Some manufactures make a non-“rail-to-rail”-op amp rail-to-rail by using a resistive divider on the inputs. The resistors divide the input voltage to get a rail-to-rail input range. The problem with this method is that it also divides the signal, so in order to get the obtained gain, the amplifier must have a higher closed loop gain. This raises the noise and drift by the internal gain factor and lowers the input impedance. Any mismatch in these precision resistors reduces the CMRR as well. The LMV611/LMV612/LMV614 is rail-to-rail and therefore doesn't have these disadvantages.

Using three of the LMV611/LMV612/LMV614 amplifiers, an instrumentation amplifier with rail-to-rail inputs and outputs can be made as shown in [Figure 5](#).

In this example, amplifiers on the left side act as buffers to the differential stage. These buffers assure that the input impedance is very high and require no precision matched resistors in the input stage. They also assure that the difference amp is driven from a voltage source. This is necessary to maintain the CMRR set by the matching R_1 - R_2 with R_3 - R_4 . The gain is set by the ratio of R_2/R_1 and R_3 should equal R_1 and R_4 equal R_2 . With both rail-to-rail input and output ranges,

the input and output are only limited by the supply voltages. Remember that even with rail-to-rail outputs, the output can not swing past the supplies so the combined common mode voltages plus the signal should not be greater that the supplies or limiting will occur. For additional applications, see National Semiconductor application notes AN-29, AN-31, AN-71, and AN-127.

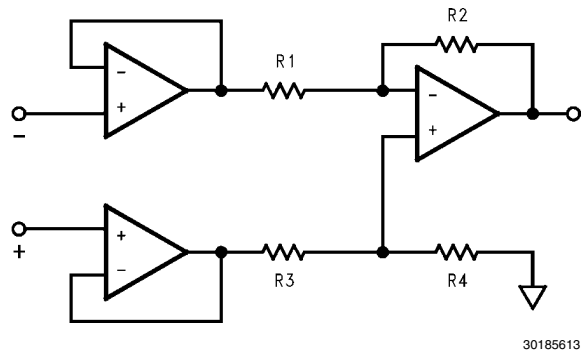
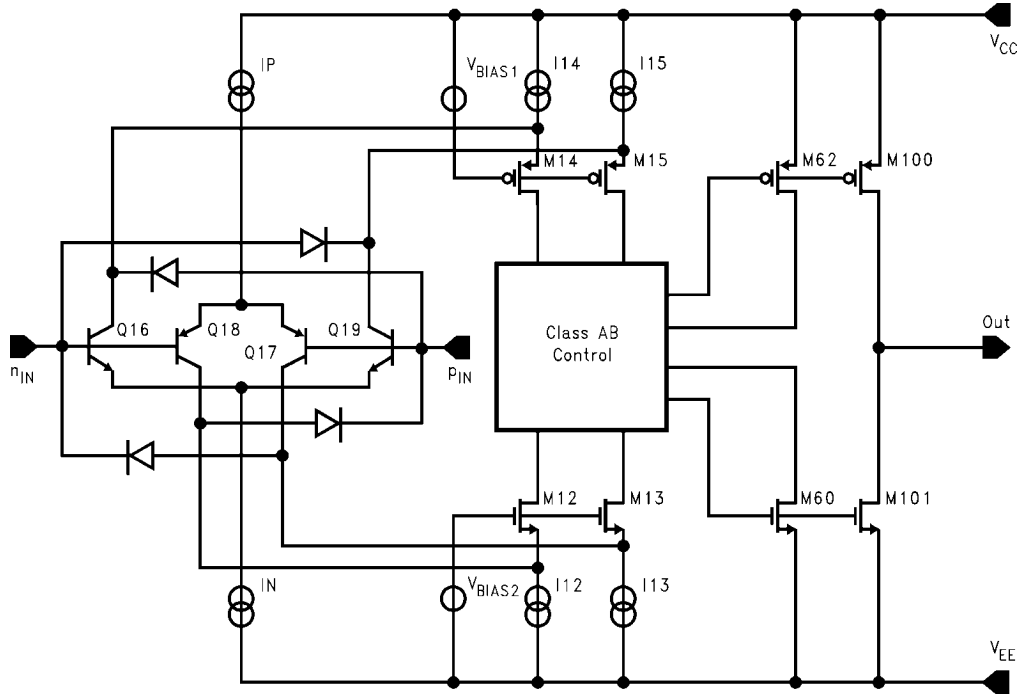


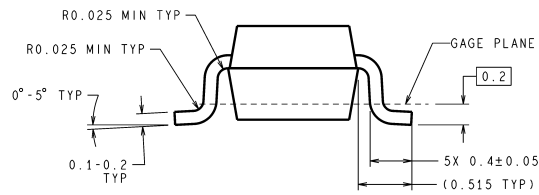
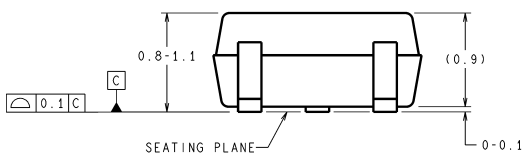
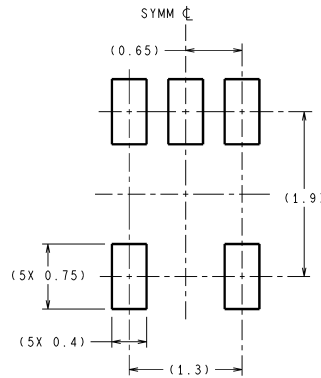
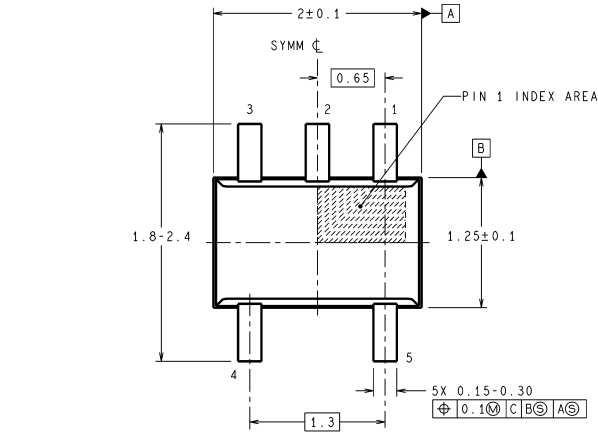
FIGURE 5. Rail-to-rail Instrumentation Amplifier

Simplified Schematic



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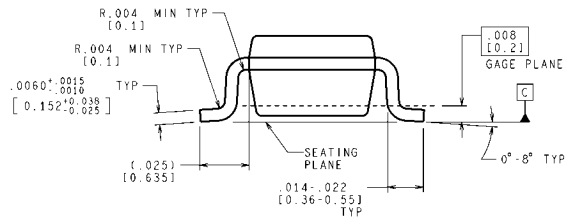
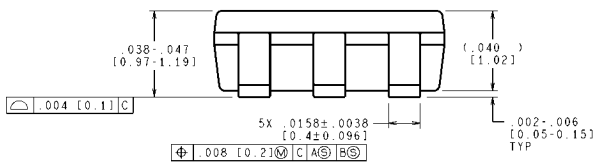
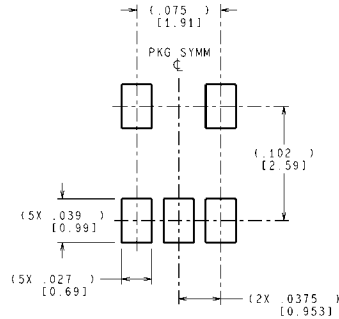
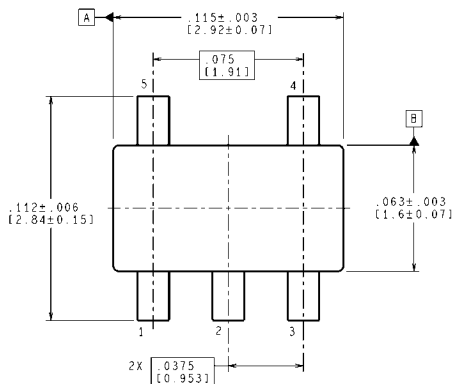
Physical Dimensions inches (millimeters) unless otherwise noted



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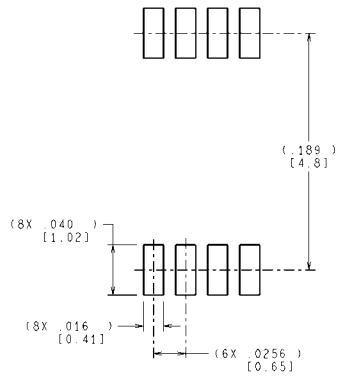
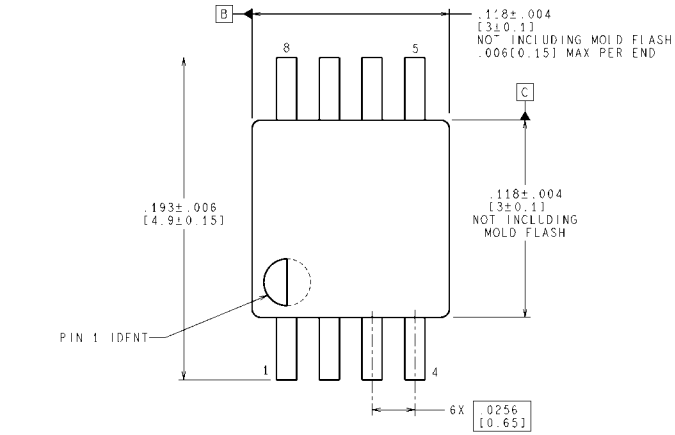
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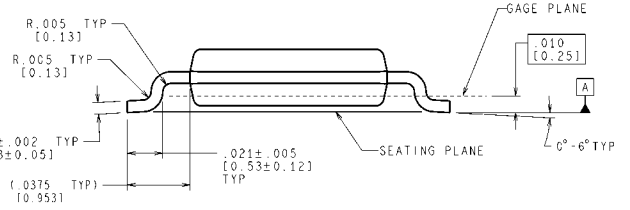
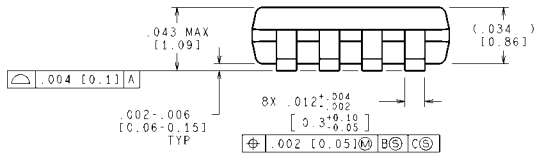
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MF05A (Rev D)

5-Pin SOT23
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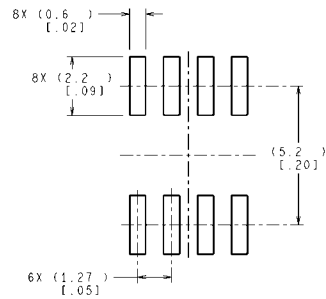
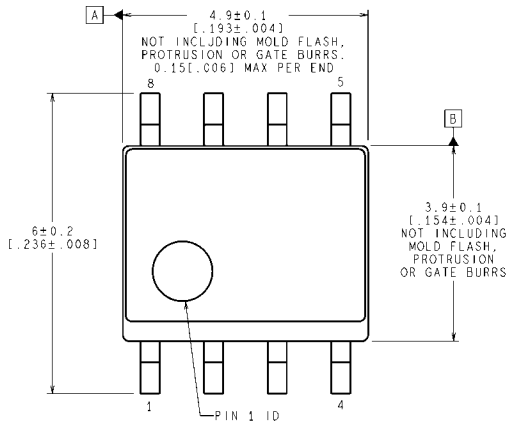
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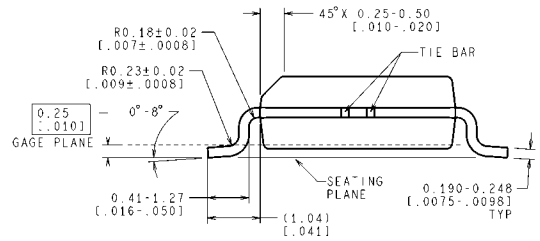
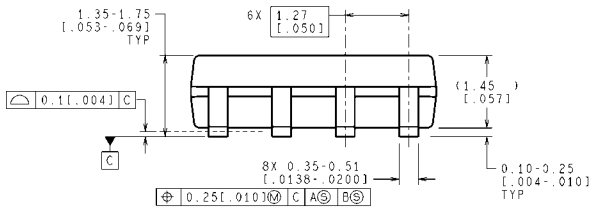
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MUA08A (Rev F)

**8-Pin MSOP
 NS Package Number MUA08A**



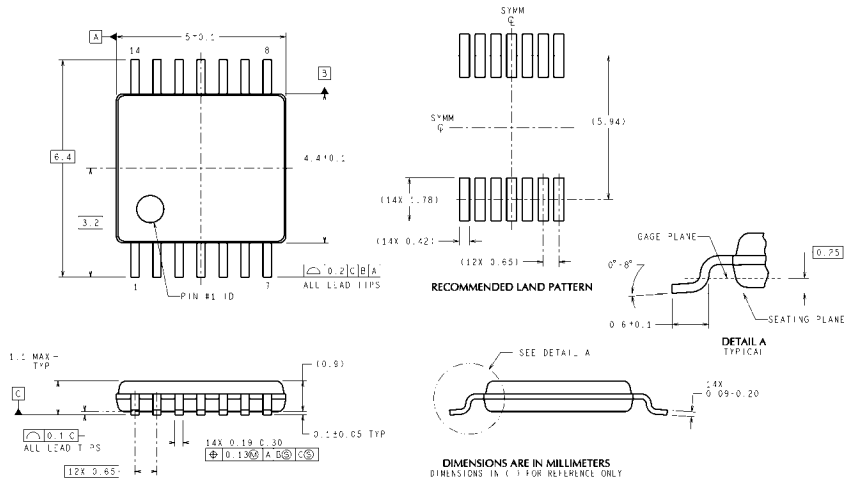
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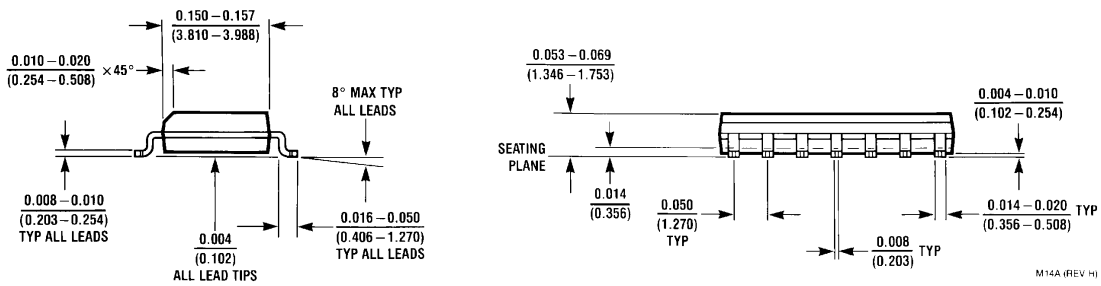
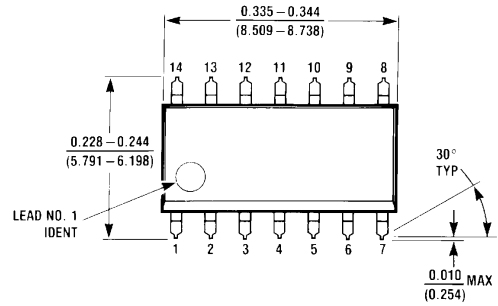
M08A (Rev M)

**8-Pin SOIC
 NS Package Number M08A**



14-Pin TSSOP
NS Package Number MTC14

MTC14 (Rev D)



14-Pin SOIC
NS Package Number M14A

Notes

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