

# M5M418160BJ, TP-6, -7, -6S, -7S

FAST PAGE MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

## DESCRIPTION

This is a family of 1048576-word by 16-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer aluminum process combined with triple-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

## FEATURES

Type name	RAS access time (max. ns)	CAS access time (max. ns)	Address access time (max. ns)	OE access time (max. ns)	Cycle time (min. ns)	Power dissipation (typ. mW)
M5M418160BXX-6, -6S	60	15	30	15	110	680
M5M418160BXX-7, -7S	70	20	35	20	130	590

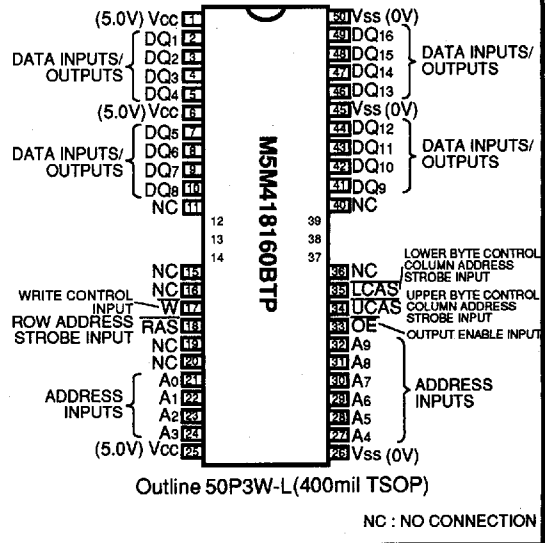
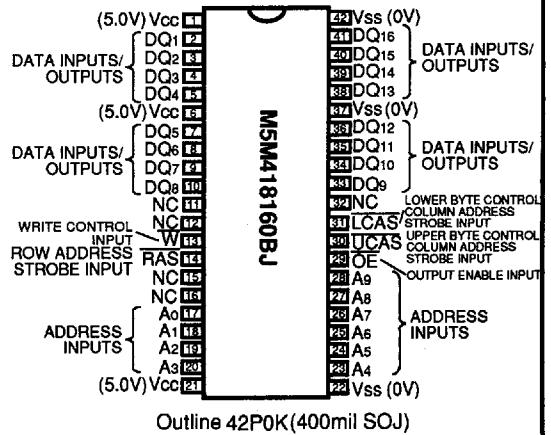
XX=J, TP

- Standard 42pin SOJ, 50pin TSOP
- Single 5.0V ± 10% supply
- Low stand-by power dissipation  
5.5mW (Max) ..... CMOS Input level
- Low operating power dissipation  
M5M418160Bxx -6, -6S ..... 940.0mW (Max)  
M5M418160Bxx -7, -7S ..... 830.0mW (Max)
- Fast-page mode, Read-modify-write, RAS-only refresh, CAS before RAS refresh, Hidden refresh capabilities
- Early-write mode and OE to control output buffer impedance
- All inputs, output TTL compatible and low capacitance
- 1024 refresh cycles every 16.4ms (A<sub>0</sub> ~A<sub>9</sub>)

## APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

## PIN CONFIGURATION ( TOP VIEW )



NC : NO CONNECTION

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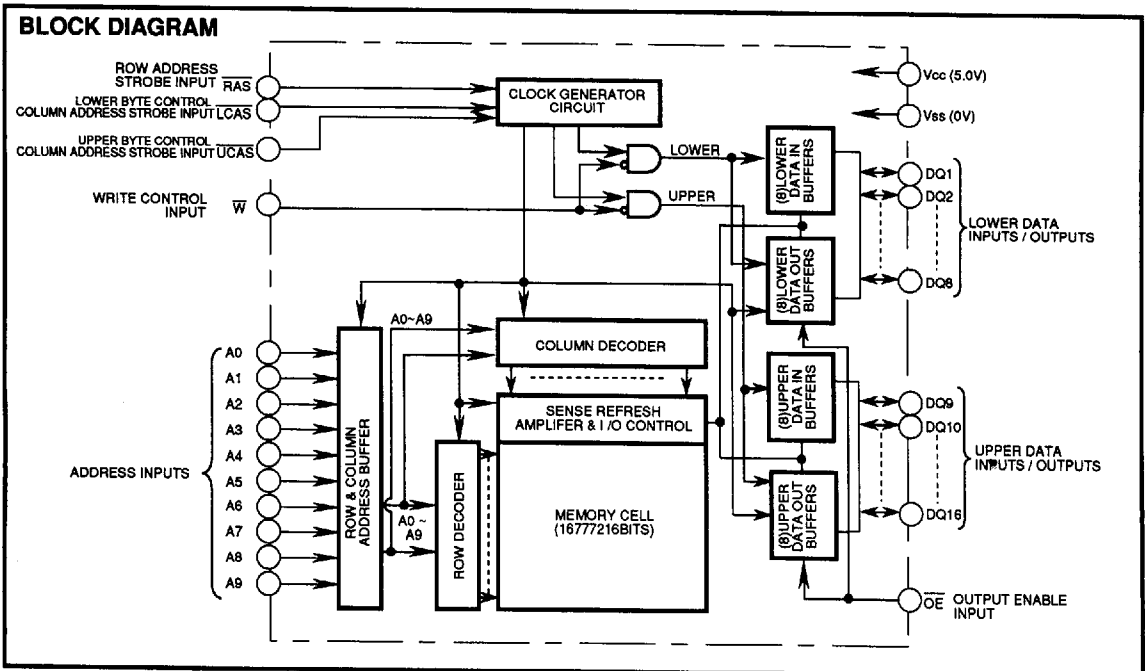
**FUNCTION**

The M5M418160BJ,TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode,  $\overline{\text{RAS}}$ -only refresh, and delayed-write. The input conditions for each are shown in Table 1.

**Table 1 Input conditions for each mode**

Operation	Inputs					Input/Output	
	RAS	LCAS	$\overline{\text{UCAS}}$	$\overline{\text{W}}$	$\overline{\text{OE}}$	DQ1-DQ8	DQ9-DQ16
Lower byte Read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte Read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word Read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower Byte Write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper Byte Write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
$\overline{\text{RAS}}$ -only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Lower Byte Hidden refresh	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper Byte Hidden refresh	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Stand-by	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : Invalid, APD : applied, OPN : open



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**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Rated	Unit
V <sub>CC</sub>	Supply voltage	With respect to V <sub>SS</sub>	-1~7	V
V <sub>I</sub>	Input voltage		-1~7	V
V <sub>O</sub>	Output voltage		-1~7	V
I <sub>O</sub>	Output current		50	mA
P <sub>d</sub>	Power dissipation	T <sub>a</sub> =25°C	1000	mW
T <sub>opr</sub>	Operating temperature		0 ~ 70	°C
T <sub>stg</sub>	Storage temperature		-65 ~ 150	°C

**RECOMMENDED OPERATING CONDITIONS** (T<sub>a</sub>=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>SS</sub>	Supply voltage	0	0	0	V
V <sub>IH</sub>	High-level input voltage, all inputs	2.4		6.0	V
V <sub>IL</sub>	Low-level input voltage, all inputs	-1		0.8	V

Note 1 : All voltage values are with respect to V<sub>SS</sub>.

**ELECTRICAL CHARACTERISTICS** (T<sub>a</sub>=0~70°C, V<sub>CC</sub>=5.0V ± 10%, V<sub>SS</sub>=0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> =-5mA	2.4		V <sub>CC</sub>	V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> =4.2mA	0		0.4	V
I <sub>OZ</sub>	Off-state output current	Q floating, 0V ≤ V <sub>OUT</sub> ≤ 5.5V	-10		10	μA
I <sub>I</sub>	Input current	0V ≤ V <sub>IH</sub> ≤ 6V, Other inputs pins=0V	-10		10	μA
I <sub>CC1</sub> (AV)	Average supply current from V <sub>CC</sub> operating (Note 3,4,5)	M5M418160B-6,-6S	R <sub>AS</sub> , C <sub>AS</sub> cycling t <sub>RC</sub> =t <sub>WC</sub> =min, output open		170	mA
		M5M418160B-7,-7S	R <sub>AS</sub> =C <sub>AS</sub> =V <sub>IH</sub> , output open		150	
I <sub>CC2</sub>	Supply current from V <sub>CC</sub> , stand-by (Note 6)	M5M418160B-6,-7	R <sub>AS</sub> =C <sub>AS</sub> ≥ V <sub>CC</sub> -0.2V, output open		1	mA
		M5M418160B-6S,-7S	R <sub>AS</sub> =C <sub>AS</sub> ≥ V <sub>CC</sub> -0.2V, output open		0.3	
I <sub>CC3</sub> (AV)	Average supply current from V <sub>CC</sub> refreshing (Note 3,5)	M5M418160B-6,-6S	R <sub>AS</sub> cycling, C <sub>AS</sub> =V <sub>IH</sub> t <sub>RC</sub> =min, output open		170	mA
		M5M418160B-7,-7S			150	
I <sub>CC4</sub> (AV)	Average supply current from V <sub>CC</sub> Fast-Page-Mode (Note 3,4,5)	M5M418160B-6,-6S	R <sub>AS</sub> =V <sub>IL</sub> , C <sub>AS</sub> cycling t <sub>RC</sub> =min, output open		85	mA
		M5M418160B-7,-7S			75	
I <sub>CC6</sub> (AV)	Average supply current from V <sub>CC</sub> C <sub>AS</sub> before R <sub>AS</sub> refresh mode (Note 3)	M5M418160B-6,-6S	C <sub>AS</sub> before R <sub>AS</sub> refresh cycling t <sub>RC</sub> =min, output open		170	mA
		M5M418160B-7,-7S			150	

Note 2: Current flowing into an IC is positive, out is negative.

3: I<sub>CC1</sub>(AV), I<sub>CC3</sub>(AV) and I<sub>CC4</sub>(AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4: I<sub>CC1</sub>(AV) and I<sub>CC4</sub>(AV) are dependent on output loading. Specified values are obtained with the output open.

5: Column Address can be changed once or less while R<sub>AS</sub>=V<sub>IL</sub> and LCAS/UCAS=V<sub>IH</sub>.

**CAPACITANCE** (T<sub>a</sub>=0~70°C, V<sub>CC</sub>=5.0V ± 10%, V<sub>SS</sub>=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C <sub>I</sub> (A)	Input capacitance, address inputs	V <sub>I</sub> =V <sub>SS</sub> f=1MHz V <sub>I</sub> =25mVrms			5	pF
C <sub>I</sub> (OE)	Input capacitance, OE input				7	pF
C <sub>I</sub> (W)	Input capacitance, W input				7	pF
C <sub>I</sub> (RAS)	Input capacitance, RAS input				7	pF
C <sub>I</sub> (CAS)	Input capacitance, CAS input				7	pF
C <sub>I/O</sub>	Input/Output capacitance, data ports				8	pF

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**SWITCHING CHARACTERISTICS** (Ta=0~70°C, Vcc=5.0V ± 10%, Vss=0V, unless otherwise noted, see notes 8,13,14)

Symbol	Parameter	Limits				Unit
		M5M418160B-6,-6S		M5M418160B-7,-7S		
		Min	Max	Min	Max	
tCAC	Access time from $\overline{\text{CAS}}$ (Note7,8)		15		20	ns
tRAC	Access time from $\overline{\text{RAS}}$ (Note7,9)		60		70	ns
tAA	Column address access time (Note 7,10)		30		35	ns
tCPA	Access time from $\overline{\text{CAS}}$ precharge (Note 7,11)		35		40	ns
tOEA	Access time from $\overline{\text{OE}}$ (Note 7)		15		20	ns
tCLZ	Output low impedance time from $\overline{\text{CAS}}$ low (Note 7)	5		5		ns
tOFF	Output disable time after $\overline{\text{CAS}}$ high (Note 12)	0	15	0	15	ns
tOEZ	Output disable time after $\overline{\text{OE}}$ high (Note 12)	0	15	0	15	ns

- Note 6: An initial pause of 500  $\mu\text{s}$  is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a  $\overline{\text{RAS}}$  clock such as  $\overline{\text{RAS}}$ -Only refresh).  
 Note the  $\overline{\text{RAS}}$  may be cycled during the initial pause. And any 8  $\overline{\text{RAS}}$  or  $\overline{\text{RAS}}/\overline{\text{CAS}}$  cycles are required after prolonged periods (greater than 16.4 ms) of  $\overline{\text{RAS}}$  inactivity before proper device operation is achieved.  
 7: Measured with a load circuit equivalent to 100pF, V<sub>OH</sub>=2.4V(I<sub>OH</sub>=-5mA) and V<sub>OL</sub>=0.4V(I<sub>OL</sub>=4.2mA).  
 8: Assumes that t<sub>RCO</sub> ≥ t<sub>RCO(max)</sub> and t<sub>ASC</sub> ≥ t<sub>ASC(max)</sub>.  
 9: Assumes that t<sub>RCO</sub> ≤ t<sub>RCO(max)</sub> and t<sub>RAD</sub> ≤ t<sub>RAD(max)</sub>. If t<sub>RCO</sub> or t<sub>RAD</sub> is greater than the maximum recommended value shown in this table, t<sub>RAC</sub> will increase by amount that t<sub>RCO</sub> exceeds the value shown.  
 10: Assumes that t<sub>RAD</sub> ≥ t<sub>RAD(max)</sub> and t<sub>ASC</sub> ≤ t<sub>ASC(max)</sub>.  
 11: Assumes that t<sub>CP</sub> ≤ t<sub>CP(max)</sub> and t<sub>ASC</sub> ≥ t<sub>ASC(max)</sub>.  
 12: t<sub>OFF(max)</sub> and t<sub>OEZ(max)</sub> defines the time at which the output achieves the high impedance state ( I<sub>OH</sub> ± 10  $\mu\text{A}$  ) and is not reference to V<sub>OH(min)</sub> or V<sub>OL(max)</sub>.

**TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and Fast-Page Mode Cycles)**

(Ta=0~70°C, Vcc=5.0V ± 10%, Vss=0V, unless otherwise noted, see notes 13,14)

Symbol	Parameter	Limits				Unit	
		M5M418160B-6,-6S		M5M418160B-7,-7S			
		Min	Max	Min	Max		
tREF	Refresh cycle time	-6, -7	16.4		16.4	ms	
tREF	Refresh cycle time	-6S, -7S	128		128	ms	
tRP	$\overline{\text{RAS}}$ high pulse width		40		50	ns	
tRCD	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ low (Note15)		20	45	20	50	ns
tCRP	Delay time, $\overline{\text{CAS}}$ high to $\overline{\text{RAS}}$ low		10		10	ns	
tRPC	Delay time, $\overline{\text{RAS}}$ high to $\overline{\text{CAS}}$ low		0		0	ns	
tCPN	$\overline{\text{CAS}}$ high pulse width		10		10	ns	
tRAD	Column address delay time from $\overline{\text{RAS}}$ low (Note16)		15	30	15	35	ns
tASR	Row address setup time before $\overline{\text{RAS}}$ low		0		0	ns	
tASC	Column address setup time before $\overline{\text{CAS}}$ low (Note17)		0	10	0	10	ns
tRAH	Row address hold time after $\overline{\text{RAS}}$ low		10		10	ns	
tCAH	Column address hold time after $\overline{\text{CAS}}$ low		15		15	ns	
tDZC	Delay time, data to $\overline{\text{CAS}}$ low (Note18)		0		0	ns	
tDZO	Delay time, data to $\overline{\text{OE}}$ low (Note18)		0		0	ns	
tCDD	Delay time, $\overline{\text{CAS}}$ high to data (Note19)		15		15	ns	
tOOD	Delay time, $\overline{\text{OE}}$ high to data (Note19)		15		15	ns	
t <sub>r</sub>	Transition time (Note20)		1	50	1	50	ns

- Note 13: The timing requirements are assumed t<sub>r</sub> = 5ns.  
 14: V<sub>IH(min)</sub> and V<sub>IL(max)</sub> are reference levels for measuring timing of input signals.  
 15: t<sub>RCO(max)</sub> is specified as a reference point only. If t<sub>RCO</sub> is less than t<sub>RCO(max)</sub>, access time is t<sub>RAC</sub>. If t<sub>RCO</sub> is greater than t<sub>RCO(max)</sub>, access time is controlled exclusively by t<sub>CAC</sub> or t<sub>AA</sub>. t<sub>RCO(min)</sub> is specified as t<sub>RCO(min)</sub> = t<sub>RAH(min)</sub> + 2t<sub>r</sub> + t<sub>ASC(min)</sub>.  
 16: t<sub>RAD(max)</sub> is specified as a reference point only. If t<sub>RAD</sub> ≥ t<sub>RAD(max)</sub> and t<sub>ASC</sub> ≤ t<sub>ASC(max)</sub>, access time is controlled exclusively by t<sub>AA</sub>.  
 17: t<sub>ASC(max)</sub> is specified as a reference point only. If t<sub>RCO</sub> ≥ t<sub>RCO(max)</sub> and t<sub>ASC</sub> ≥ t<sub>ASC(max)</sub>, access time is controlled exclusively by t<sub>CAC</sub>.  
 18: Either t<sub>DZC</sub> or t<sub>DZO</sub> must be satisfied.  
 19: Either t<sub>CDD</sub> or t<sub>OOD</sub> must be satisfied.  
 20: t<sub>r</sub> is measured between V<sub>IH(min)</sub> and V<sub>IL(max)</sub>.

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## Read and Refresh Cycles

Symbol	Parameter	Limits				Unit
		M5M418160B-6,-6S		M5M418160B-7,-7S		
		Min	Max	Min	Max	
trc	Read cycle time	110		130		ns
trAS	$\overline{\text{RAS}}$ low pulse width	60	10000	70	10000	ns
tcAS	$\overline{\text{CAS}}$ low pulse width	15	10000	20	10000	ns
tCSH	$\overline{\text{CAS}}$ hold time after $\overline{\text{RAS}}$ low	60		70		ns
trSH	$\overline{\text{RAS}}$ hold time after $\overline{\text{CAS}}$ low	15		20		ns
trCS	Read Setup time before $\overline{\text{CAS}}$ low	0		0		ns
trCH	Read hold time after $\overline{\text{CAS}}$ high (Note 21)	0		0		ns
trRH	Read hold time after $\overline{\text{RAS}}$ high (Note 21)	10		10		ns
trAL	Column address to $\overline{\text{RAS}}$ hold time	30		35		ns
toCH	$\overline{\text{CAS}}$ hold time after $\overline{\text{OE}}$ low	15		20		ns
toRH	$\overline{\text{RAS}}$ hold time after $\overline{\text{OE}}$ low	15		20		ns

Note 21: Either trCH or trRH must be satisfied for a read cycle.

## Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits				Unit
		M5M418160B-6,-6S		M5M418160B-7,-7S		
		Min	Max	Min	Max	
twc	Write cycle time	110		130		ns
trAS	$\overline{\text{RAS}}$ low pulse width	60	10000	70	10000	ns
tcAS	$\overline{\text{CAS}}$ low pulse width	15	10000	20	10000	ns
tCSH	$\overline{\text{CAS}}$ hold time after $\overline{\text{RAS}}$ low	60		70		ns
trSH	$\overline{\text{RAS}}$ hold time after $\overline{\text{CAS}}$ low	15		20		ns
twCS	Write setup time before $\overline{\text{CAS}}$ low (Note 23)	0		0		ns
twCH	Write hold time after $\overline{\text{CAS}}$ low	10		10		ns
tcWL	$\overline{\text{CAS}}$ hold time after $\overline{\text{W}}$ low	15		20		ns
trWL	$\overline{\text{RAS}}$ hold time after $\overline{\text{W}}$ low	15		20		ns
tWP	Write pulse width	10		10		ns
tDS	Data setup time before $\overline{\text{CAS}}$ low or $\overline{\text{W}}$ low	0		0		ns
toH	Data hold time after $\overline{\text{CAS}}$ low or $\overline{\text{W}}$ low	10		15		ns
toEH	$\overline{\text{OE}}$ hold time after $\overline{\text{W}}$ low	15		20		ns

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**Read-Write and Read-Modify-Write Cycles**

Symbol	Parameter	Limits				Unit
		M5M418160B-6,-6S		M5M418160B-7,-7S		
		Min	Max	Min	Max	
t <sub>RWC</sub>	Read write/read modify write cycle time (Note22)	155		180		ns
t <sub>RAS</sub>	RAS low pulse width	105	10000	120	10000	ns
t <sub>CAS</sub>	CAS low pulse width	60	10000	70	10000	ns
t <sub>CSH</sub>	CAS hold time after RAS low	105		120		ns
t <sub>RSH</sub>	RAS hold time after CAS low	60		70		ns
t <sub>RCS</sub>	Read setup time before CAS low	0		0		ns
t <sub>CWD</sub>	Delay time, CAS low to W low (Note23)	40		45		ns
t <sub>RWD</sub>	Delay time, RAS low to W low (Note23)	85		95		ns
t <sub>AWD</sub>	Delay time, address to W low (Note23)	55		60		ns
t <sub>CWL</sub>	CAS hold time after W low	15		20		ns
t <sub>RWL</sub>	RAS hold time after W low	15		20		ns
t <sub>WP</sub>	Write pulse width	10		10		ns
t <sub>DS</sub>	Data setup time before W low	0		0		ns
t <sub>DH</sub>	Data hold time after W low	10		15		ns
t <sub>OEH</sub>	OE hold time after W low	15		15		ns

Note 22: t<sub>RWC</sub> is specified as t<sub>RWC(min)</sub>=t<sub>RAC(max)</sub>+t<sub>ODD(min)</sub>+t<sub>RWL(min)</sub>+t<sub>RP(min)</sub>+5t<sub>T</sub>.

23: t<sub>WCS</sub>, t<sub>CWD</sub>, t<sub>RWD</sub> and t<sub>AWD</sub> and t<sub>CPWD</sub> are specified as reference points only. If t<sub>WCS</sub> ≥ t<sub>WCS(min)</sub> the cycle is an early write cycle and the DQpins will remain high impedance throughout the entire cycle. If t<sub>CWD</sub> ≥ t<sub>CWD(min)</sub>, t<sub>RWD</sub> ≥ t<sub>RWD(min)</sub>, t<sub>AWD</sub> ≥ t<sub>AWD(min)</sub> and t<sub>CPWD</sub> ≥ t<sub>CPWD(min)</sub> (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until CAS or OE goes back to V<sub>IH</sub>) is indeterminate.

**Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 24)**

Symbol	Parameter	Limits				Unit
		M5M418160B-6,-6S		M5M418160B-7,-7S		
		Min	Max	Min	Max	
t <sub>PC</sub>	Fast page mode read/write cycle time	40		45		ns
t <sub>PRWC</sub>	Fast page mode read write/read modify write cycle time	85		95		ns
t <sub>RAS</sub>	RAS low pulse width for read write cycle (Note25)	100	125000	115	125000	ns
t <sub>CP</sub>	CAS high pulse width (Note26)	10	15	10	15	ns
t <sub>CPRH</sub>	RAS hold time after CAS precharge	35		40		ns
t <sub>CPWD</sub>	Delay time, CAS precharge to W low (Note23)	60		65		ns

Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

25: t<sub>RAS(min)</sub> is specified as two cycles of CAS input are performed.

26: t<sub>CP(max)</sub> is specified as a reference point only.

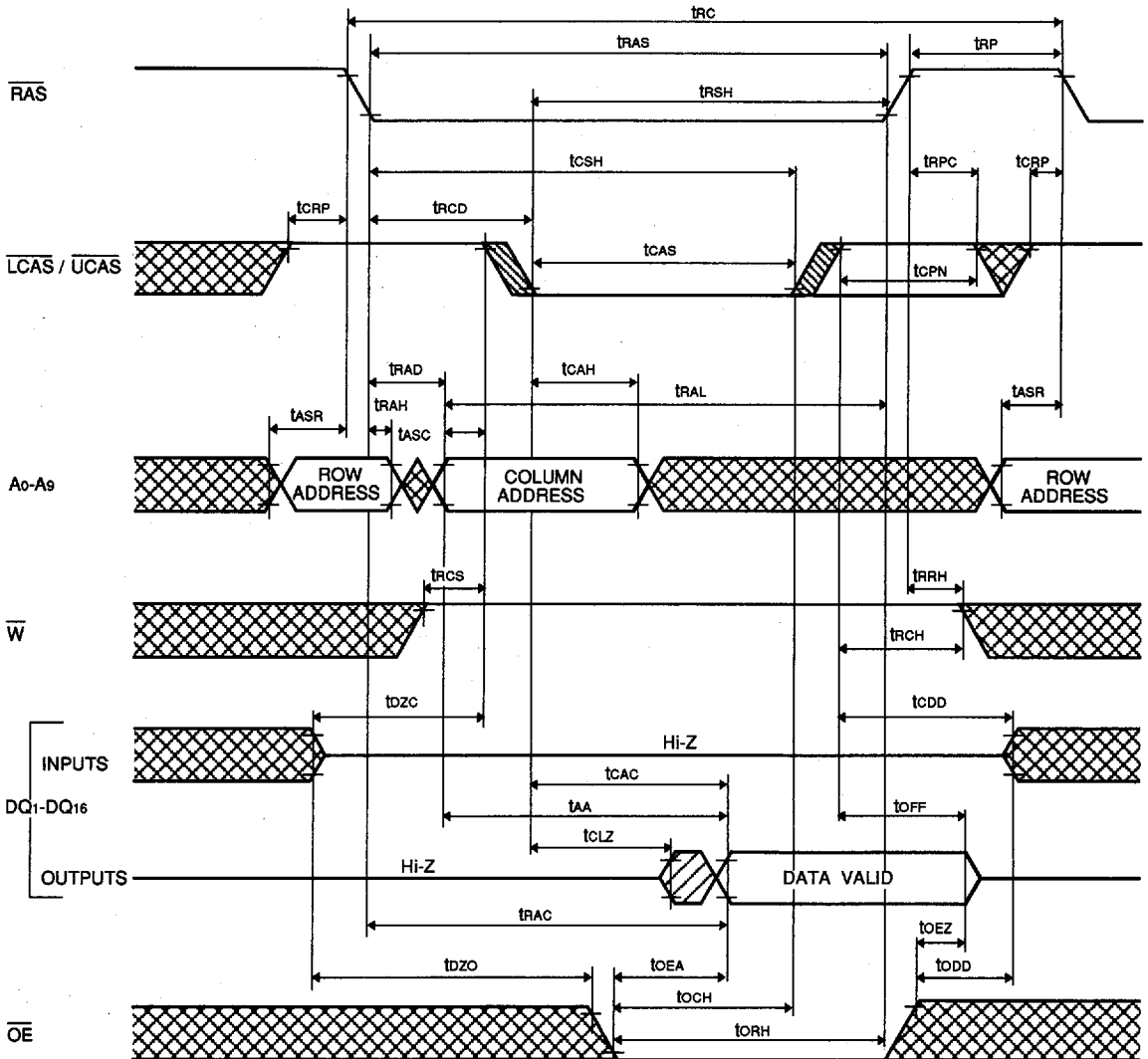
**CAS before RAS Refresh Cycle (Note 27)**




Symbol	Parameter	Limits				Unit
		M5M418160B-6,-6S		M5M418160B-7,-7S		
		Min	Max	Min	Max	
t <sub>CSR</sub>	CAS setup time before RAS low	10		10		ns
t <sub>CHR</sub>	CAS hold time after RAS low	10		15		ns

Note 27: Eight or more CAS before RAS cycles instead of eight RAS cycles are necessary for proper operation of CAS before RAS refresh mode.

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Timing Diagrams (Note 28)  
Read Cycle



- Note 28
-  Indicates the don't care input.  
 $V_{IH(min.)} \leq V_{IN} \leq V_{IH(max.)}$  or  $V_{IL(min.)} \leq V_{IN} \leq V_{IL(max.)}$
  -  Indicates the invalid output.
  -  Indicates the skew of the two inputs.

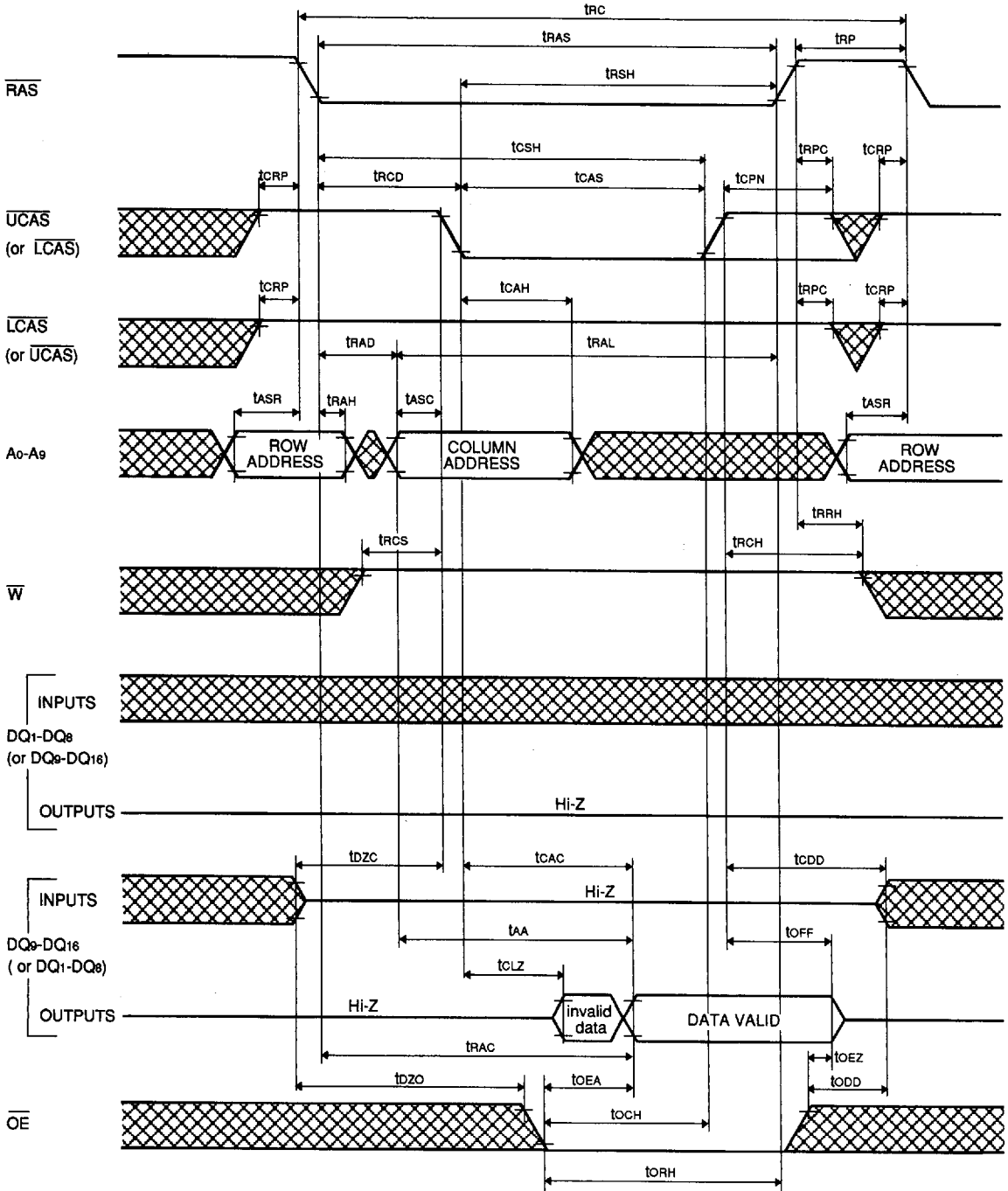
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Upper / (Lower) Byte Read Cycle



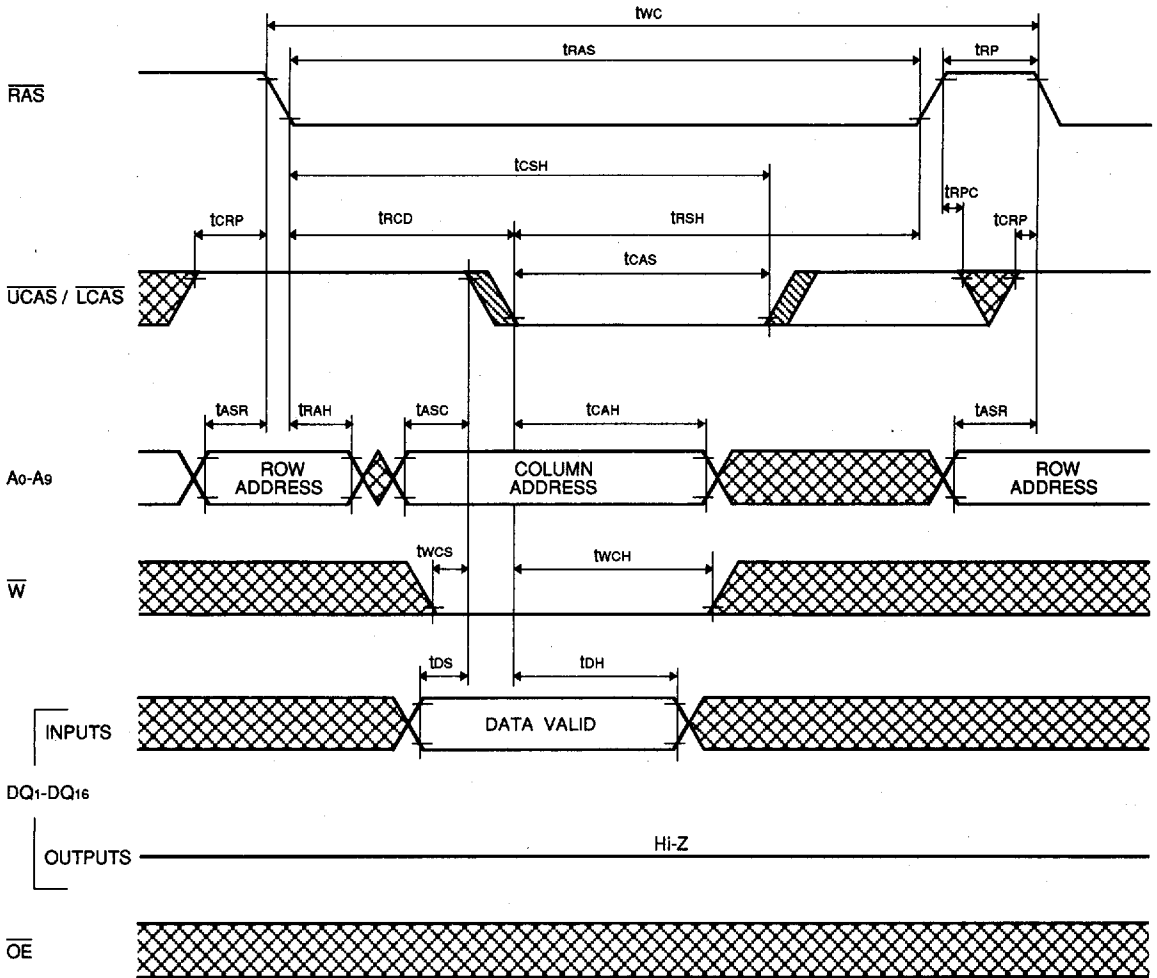
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FAST PAGE MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

Write Cycle ( Early write )

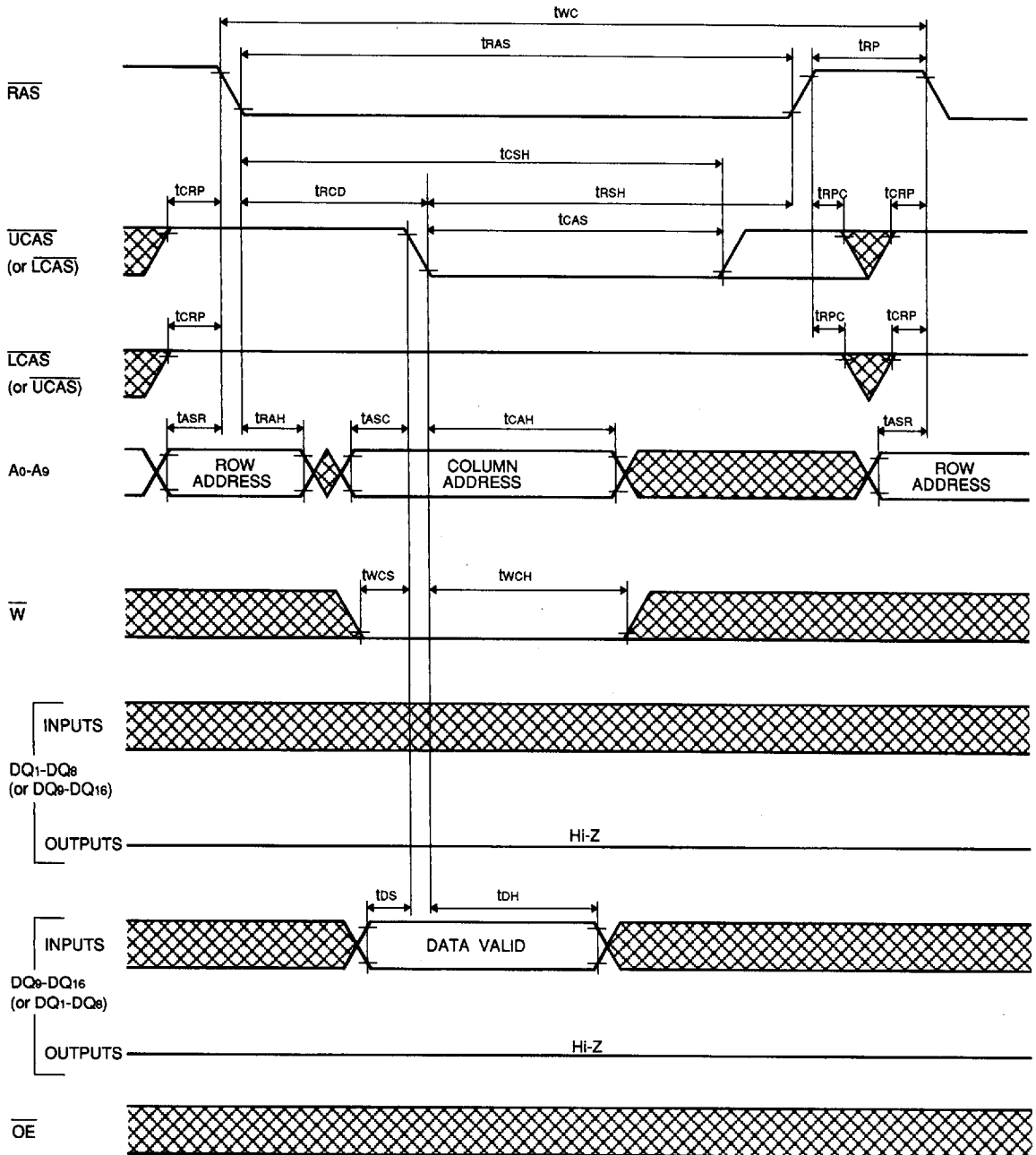


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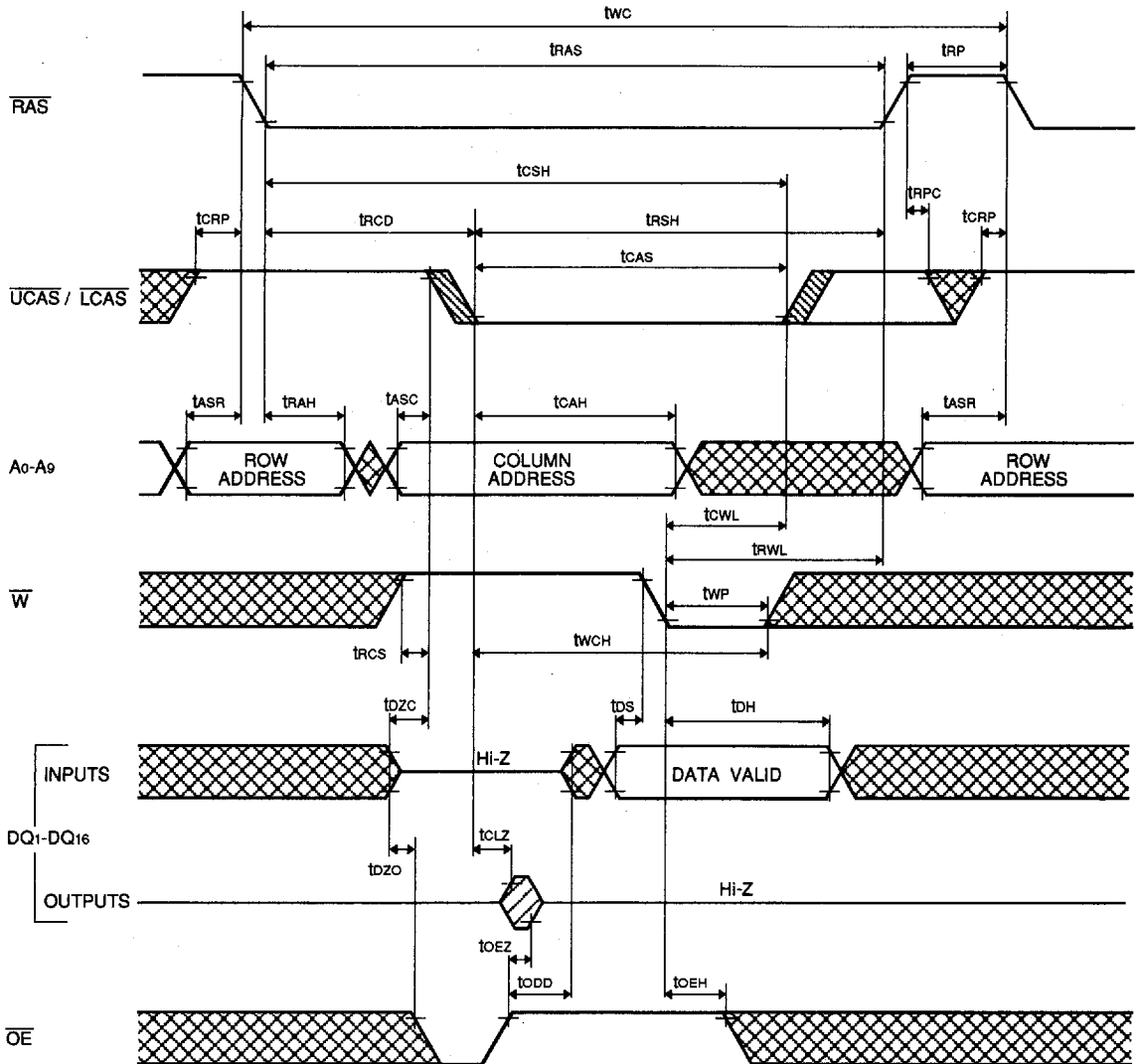
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Upper/(Lower) Byte Write Cycle (Early write)



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Write Cycle ( Delayed write )

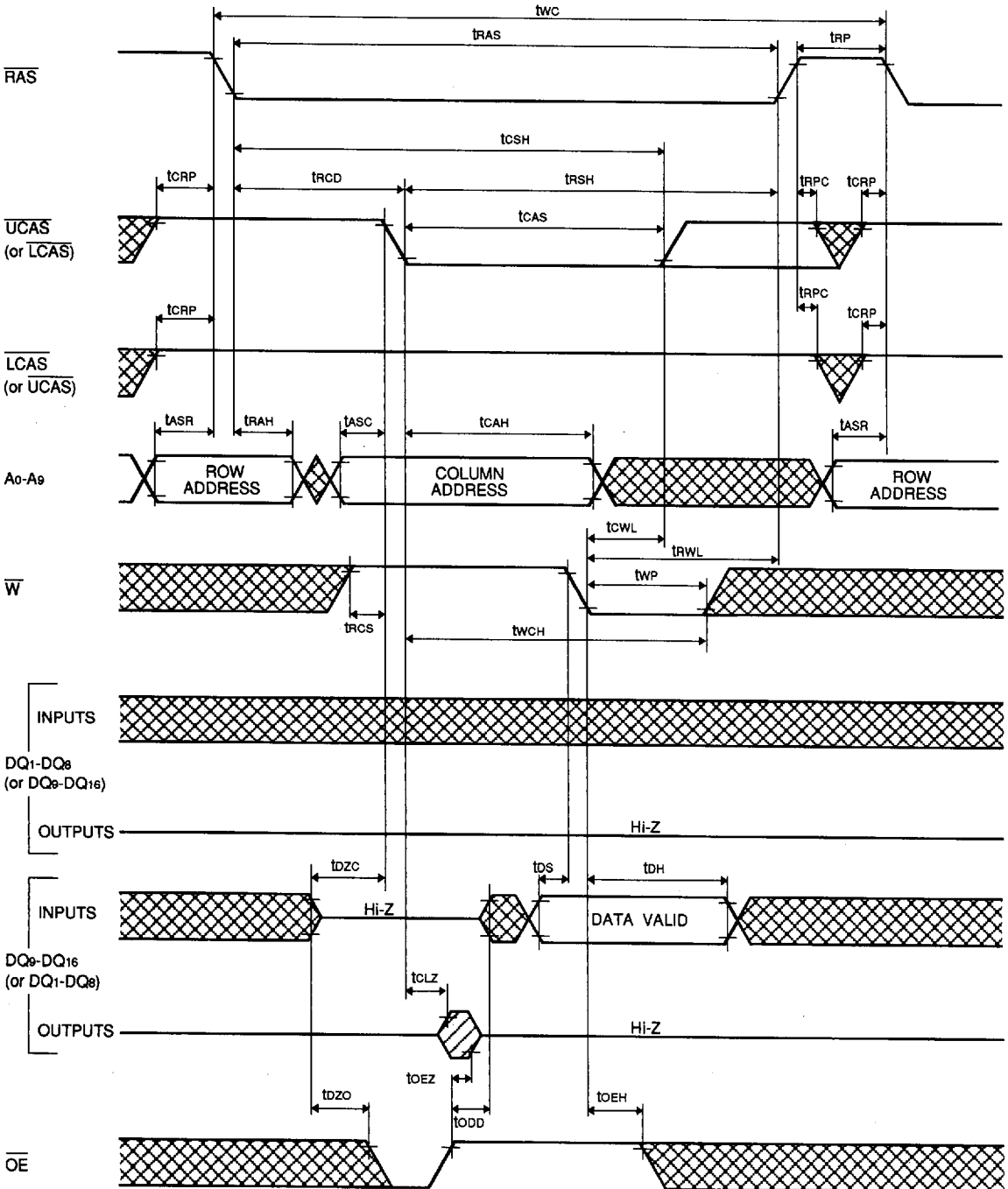


6249825 0028752 644

MITSUBISHI LSIs  
**M5M418160BJ, TP-6, -7, -6S, -7S**

FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

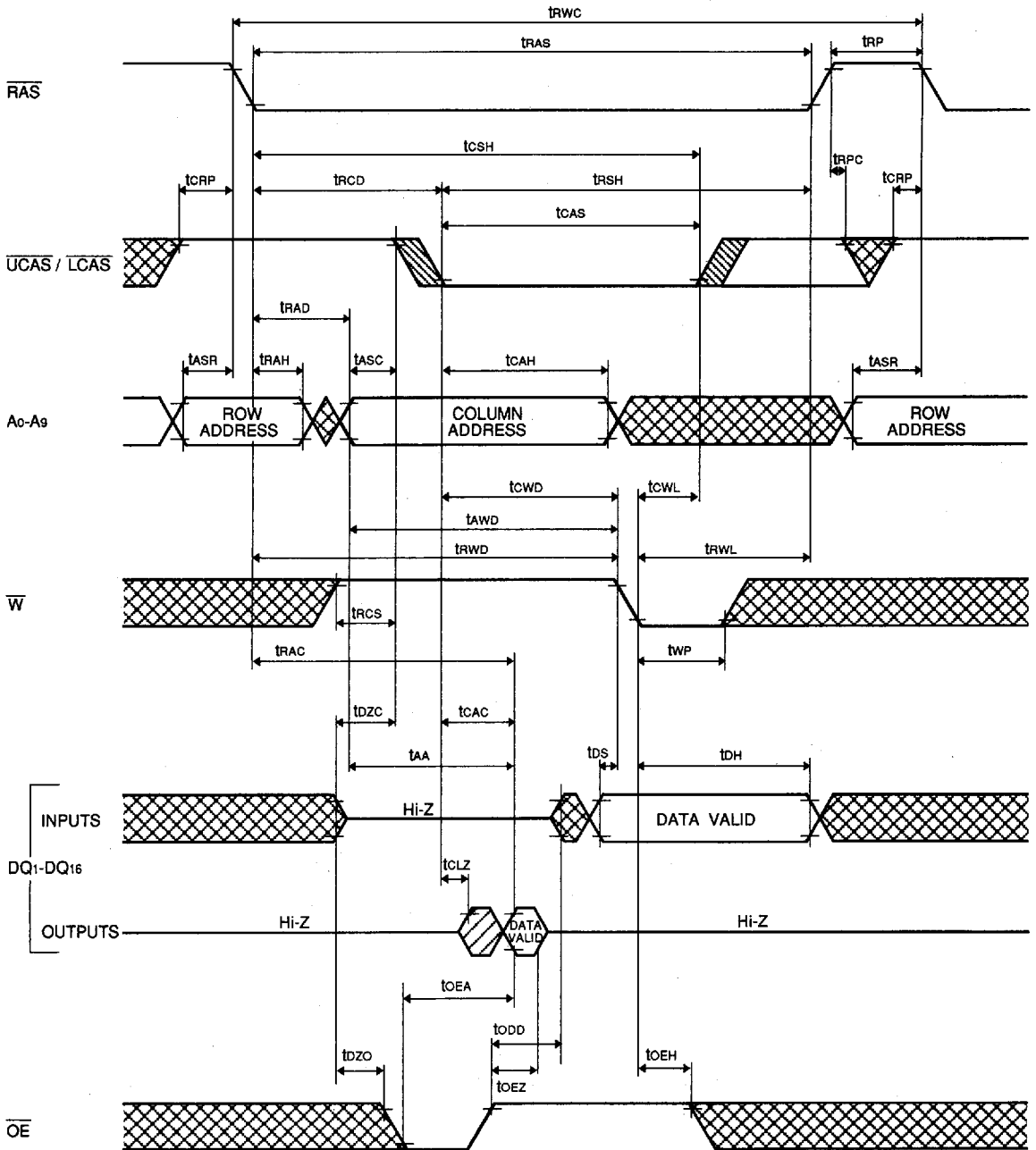
Upper/(Lower) Byte Write Cycle (Delayed write)



6249825 0028753 580



Read-Write, Read-Modify-Write Cycle

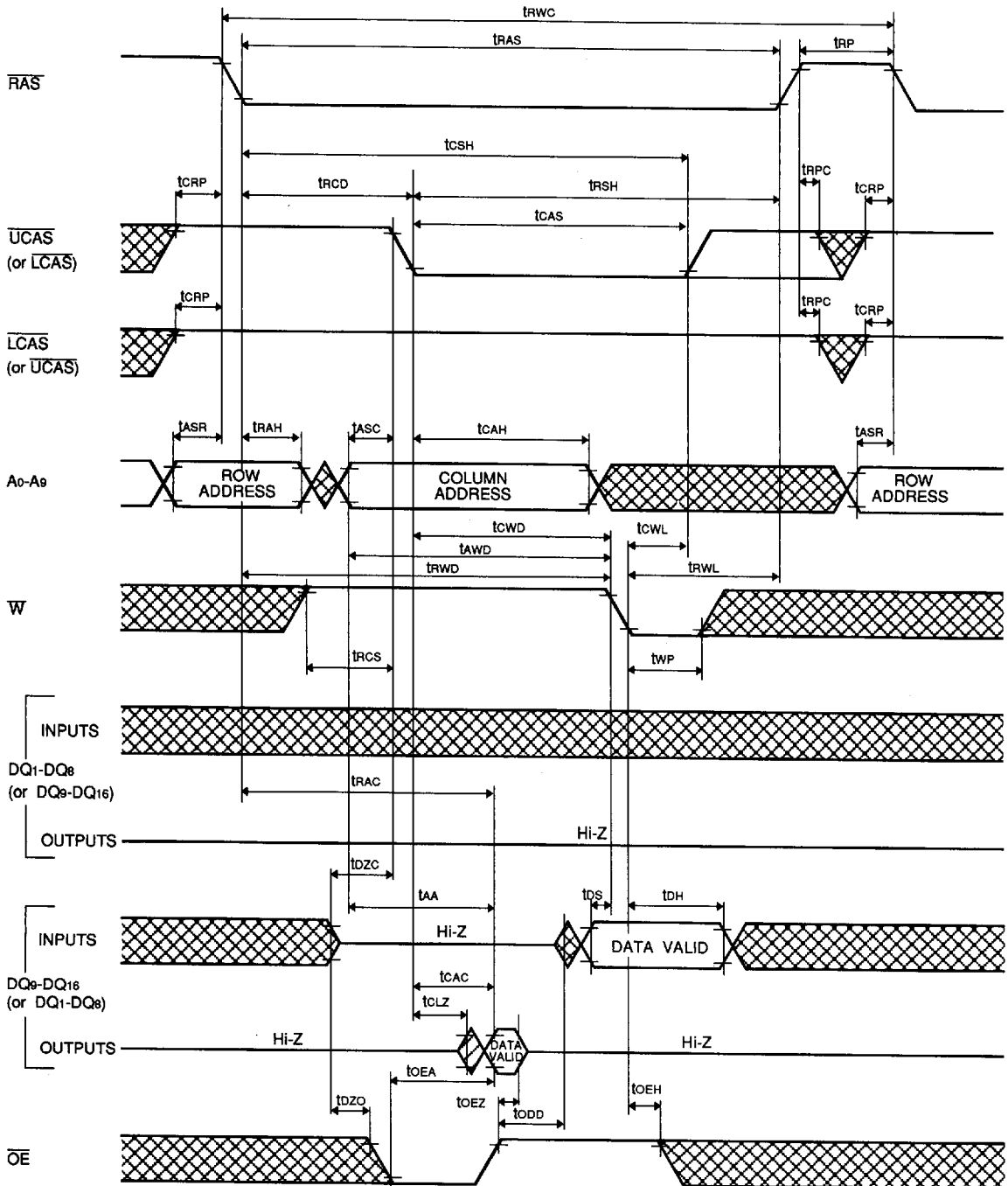


6249825 0028754 417

MITSUBISHI LSIs  
**M5M418160BJ,TP-6,-7,-6S,-7S**

FAST PAGE MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

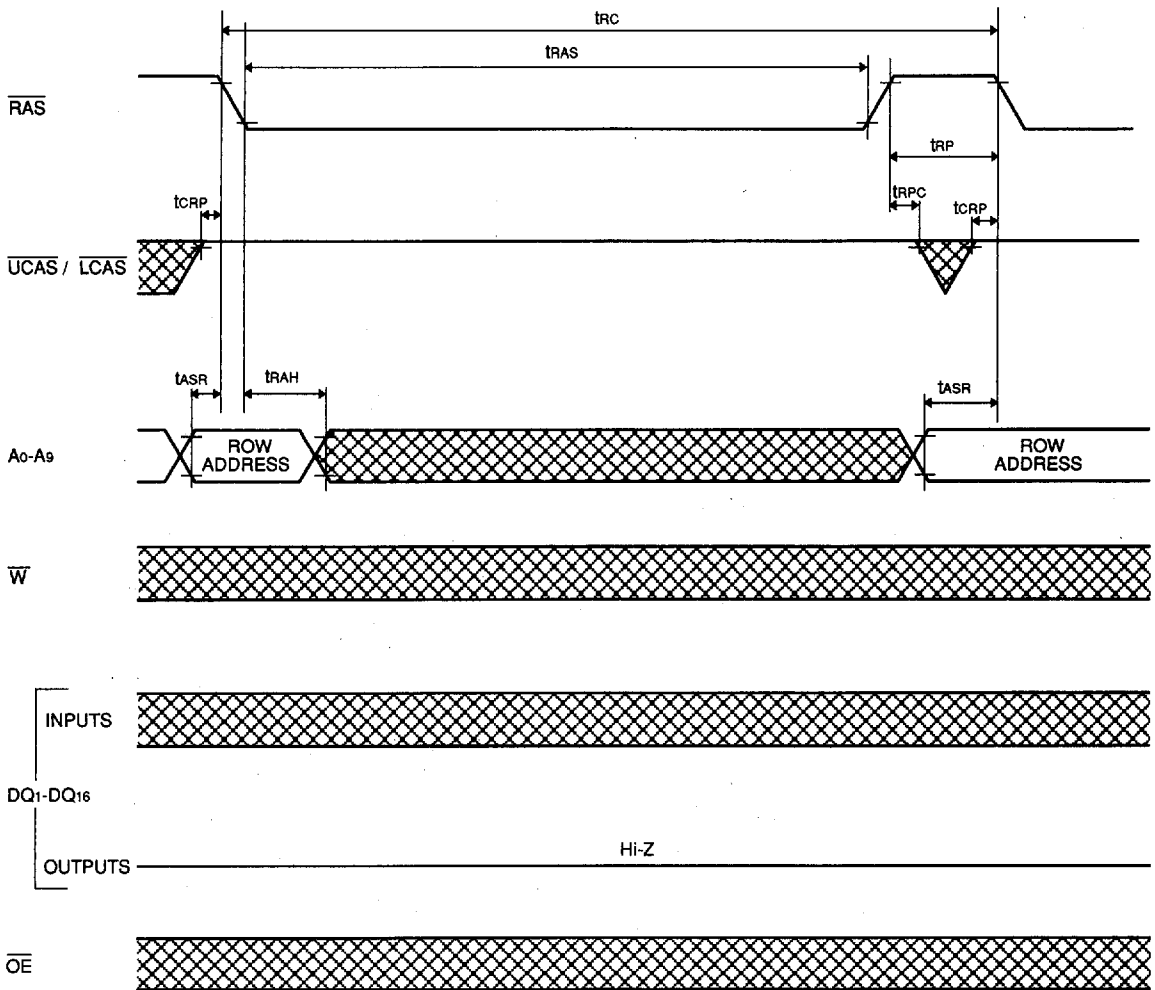
**Read-Upper/(Lower) Write, Read-Modify-Upper/(Lower) Write Cycle**



■ 6249825 0028755 353 ■



**RAS-only Refresh Cycle**

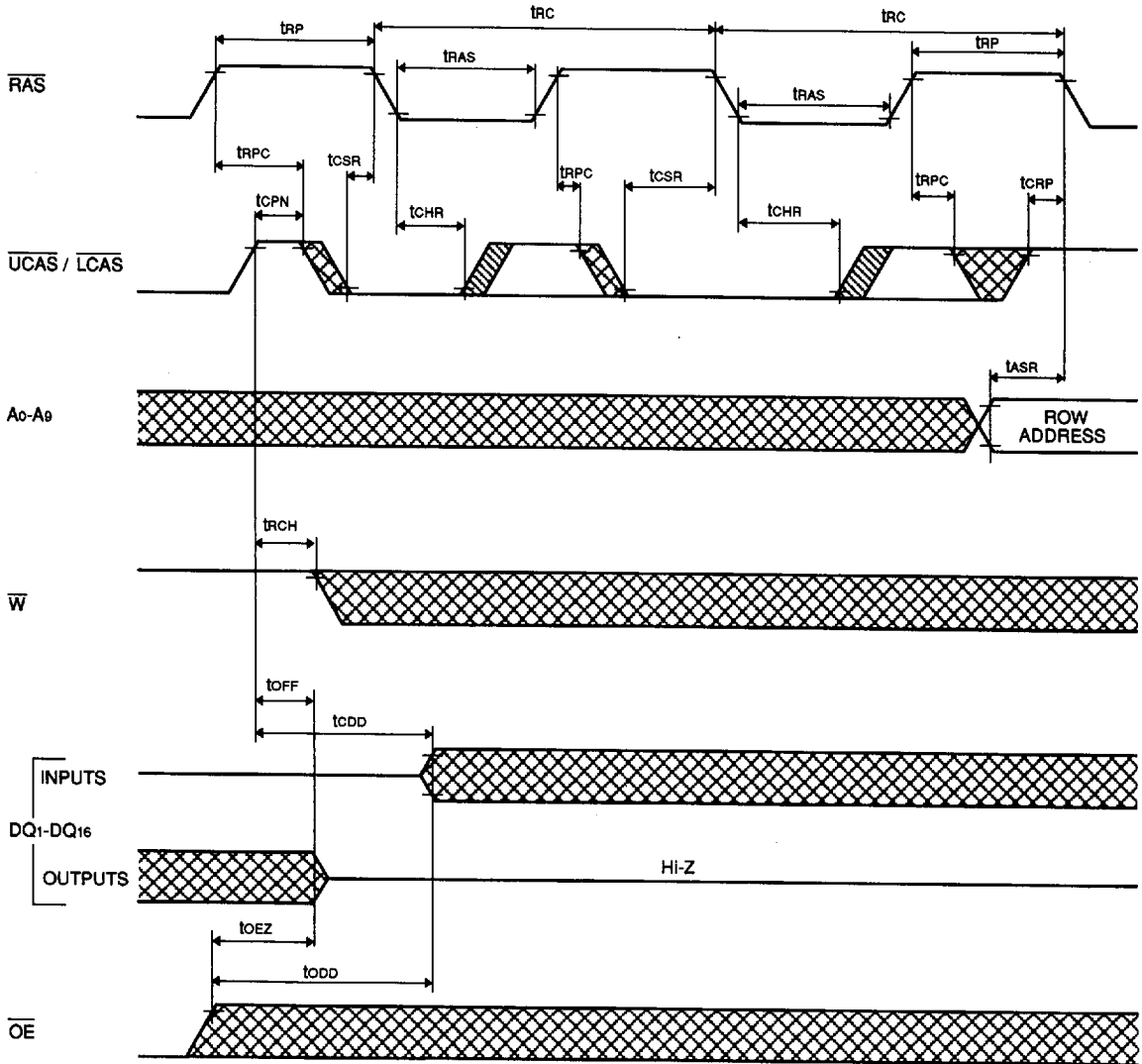


■ 6249825 0028756 29T ■

MITSUBISHI LSIs  
**M5M418160BJ,TP-6,-7,-6S,-7S**

FAST PAGE MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

**CAS before RAS Refresh Cycle**



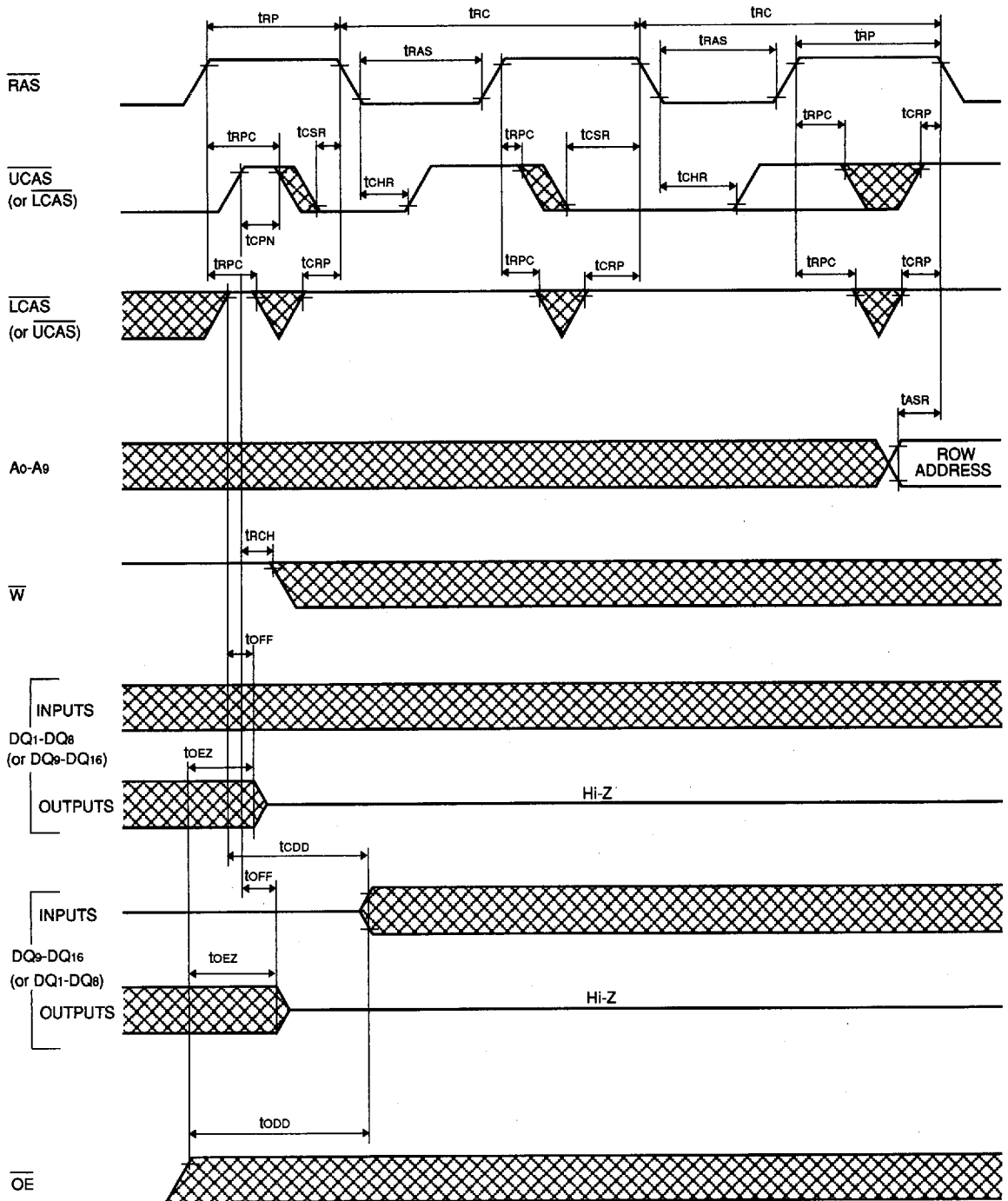
■ 6249825 0028757 126 ■



M5M418160BJ, TP-6, -7, -6S, -7S

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Upper/(Lower) CAS before RAS Refresh Cycle

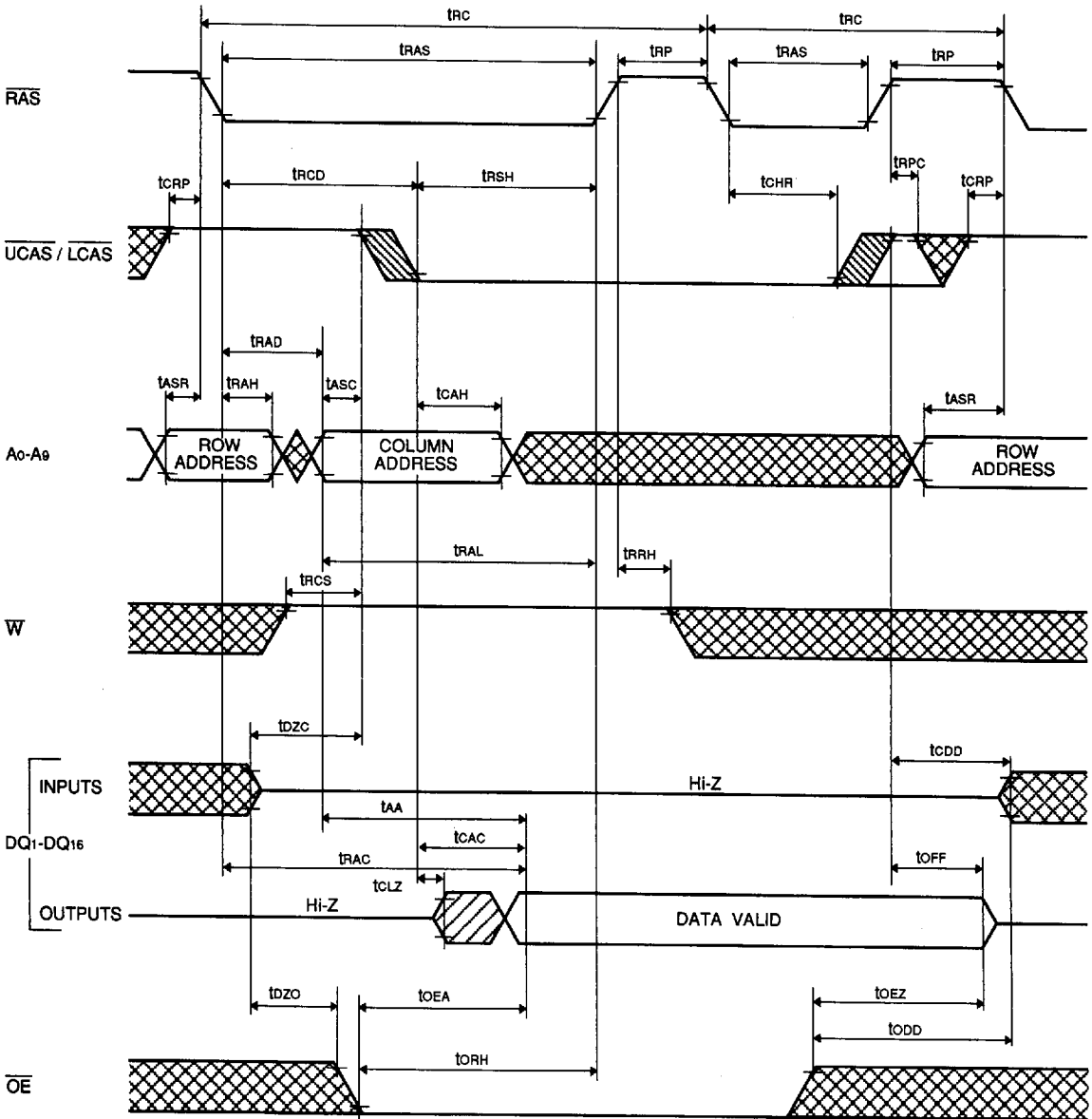


6249825 0028758 062

MITSUBISHI LSIs  
**M5M418160BJ,TP-6,-7,-6S,-7S**

FAST PAGE MODE 16777216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

**Hidden Refresh Cycle (Read)** (Note 29)

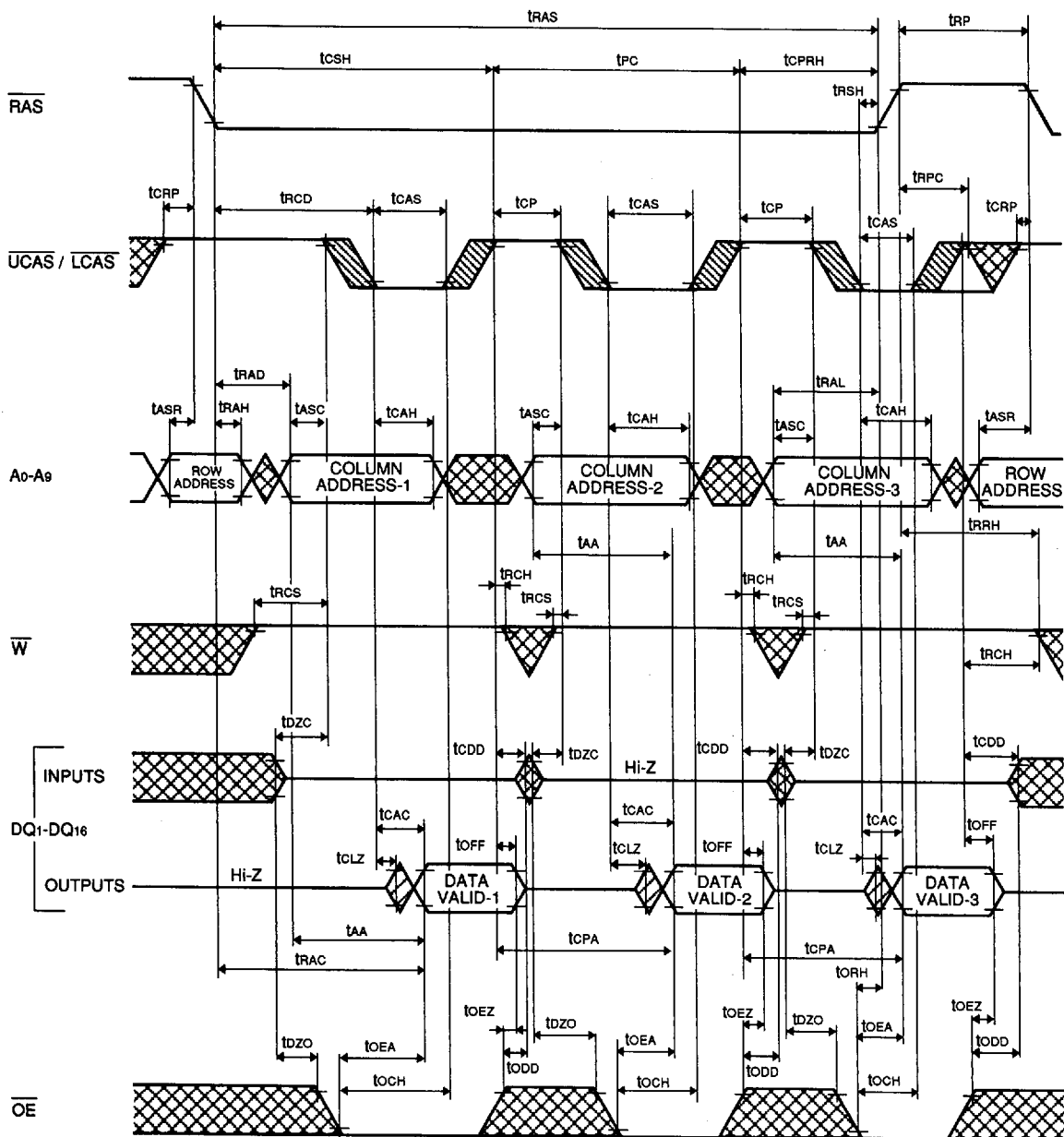


Note 29: Early write, delayed write, read write or read modify write cycle is applicable as well as read cycle. Timing requirements and output state are the same as that of each cycle shown above.

6249825 0028759 TT9

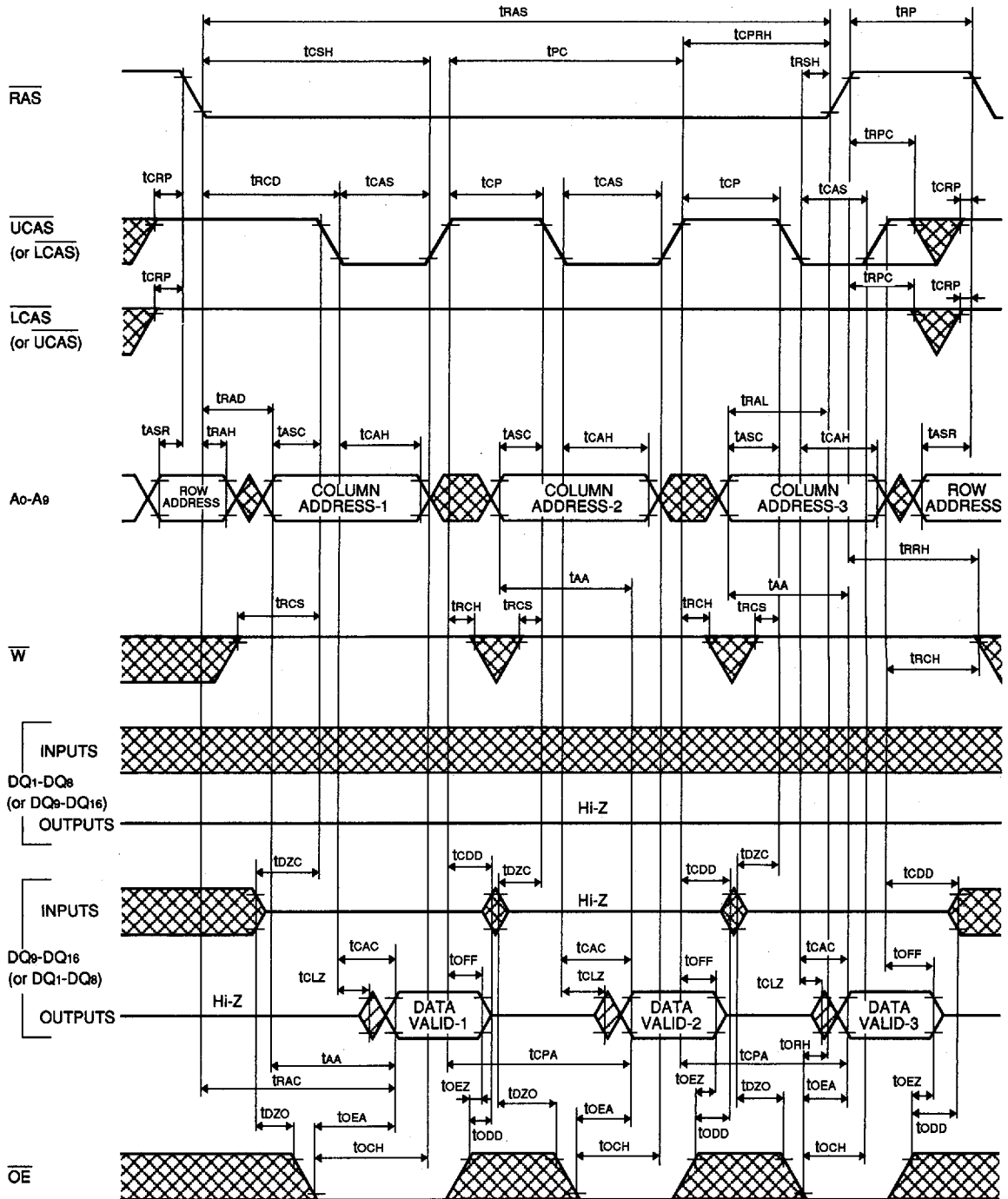


Fast Page Mode Read Cycle



6249825 0028761 657

**Upper/(Lower) Fast Page Mode Read Cycle**

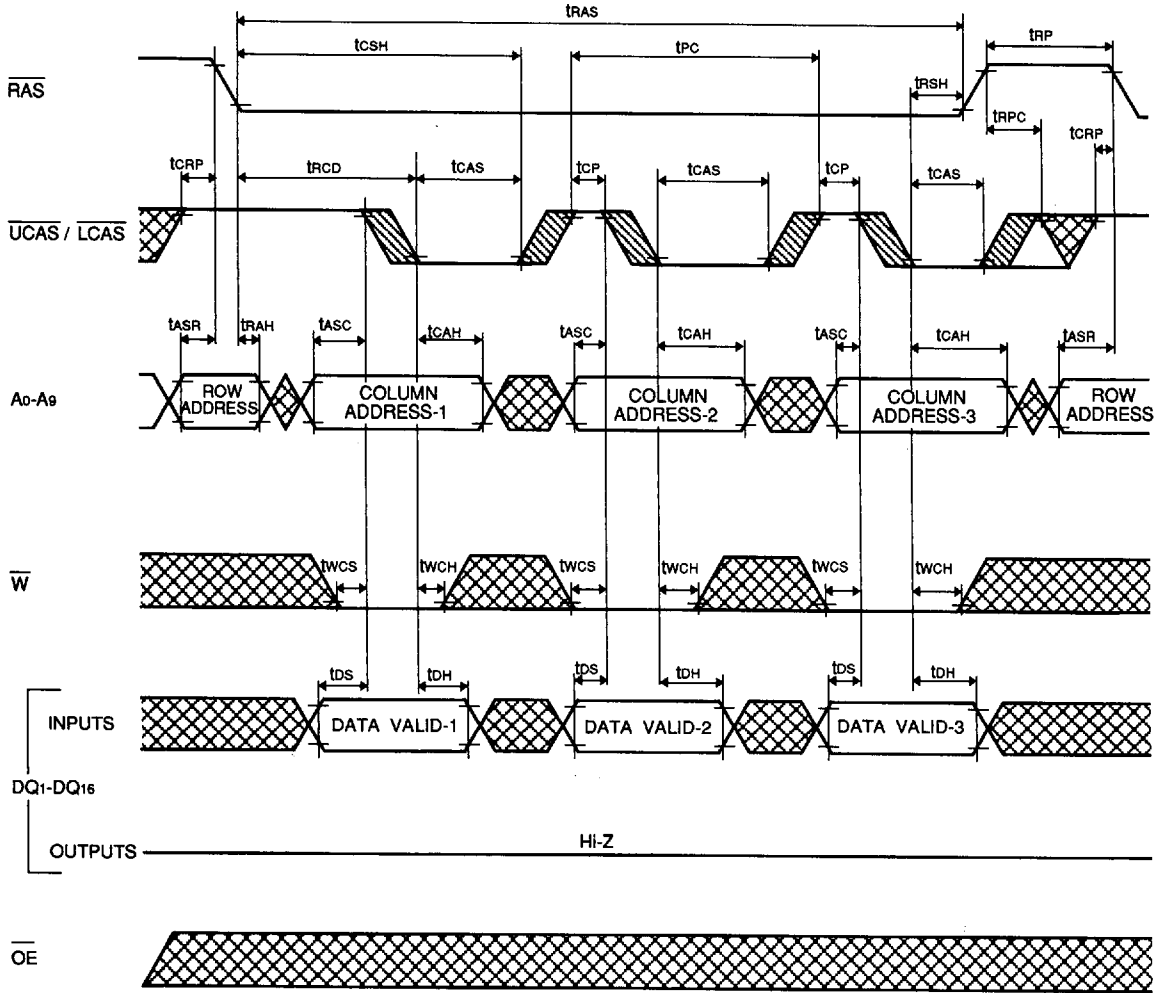


6249825 0028762 593

MITSUBISHI LSIs  
**M5M418160BJ,TP-6,-7,-6S,-7S**

FAST PAGE MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

**Fast Page Mode Write Cycle ( Early Write )**



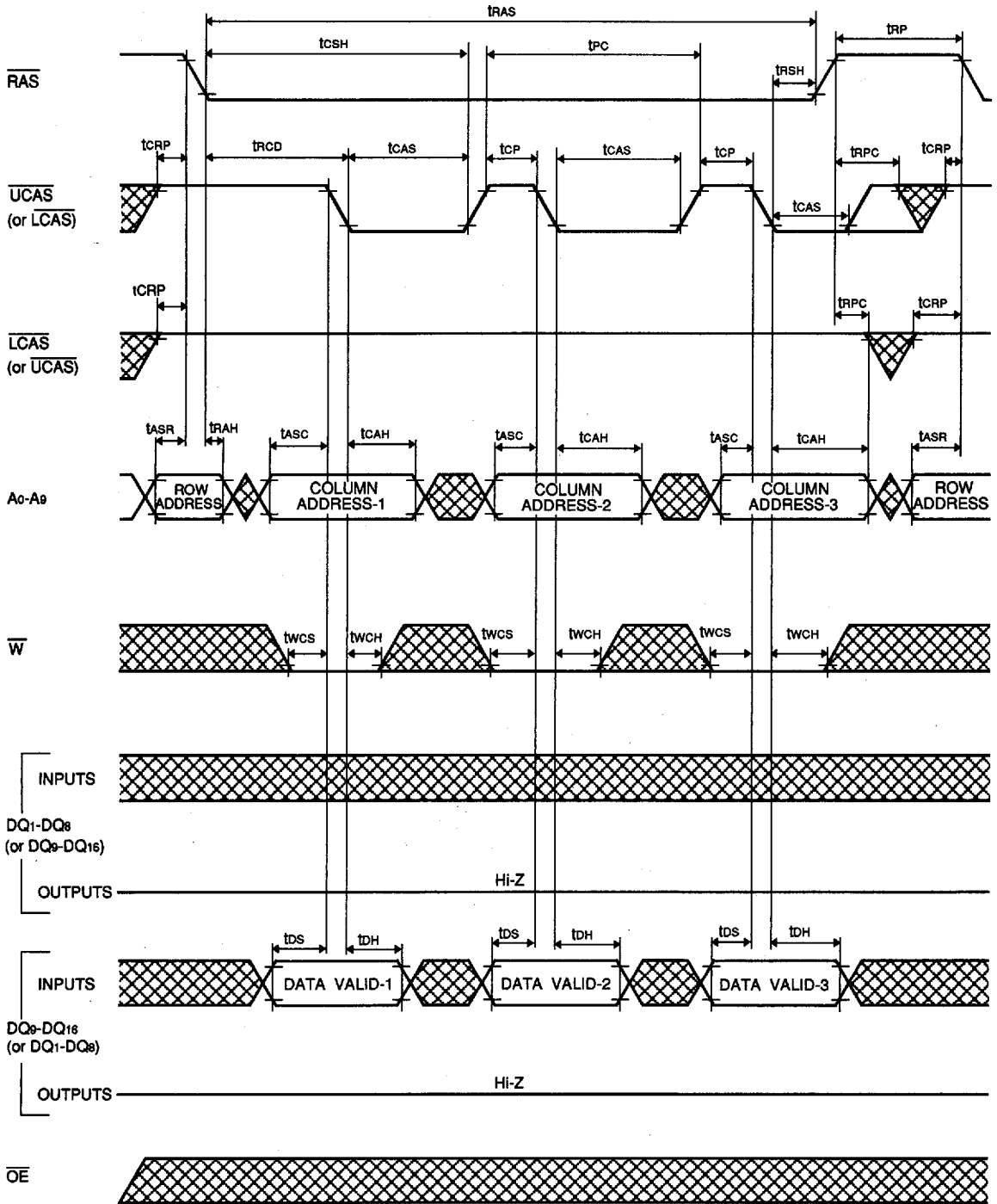
■ 6249825 0028763 42T ■



MITSUBISHI LSIs  
**M5M418160BJ, TP-6,-7,-6S,-7S**

FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

**Fast Page Mode Upper/(Lower) Byte Write Cycle ( Early Write )**

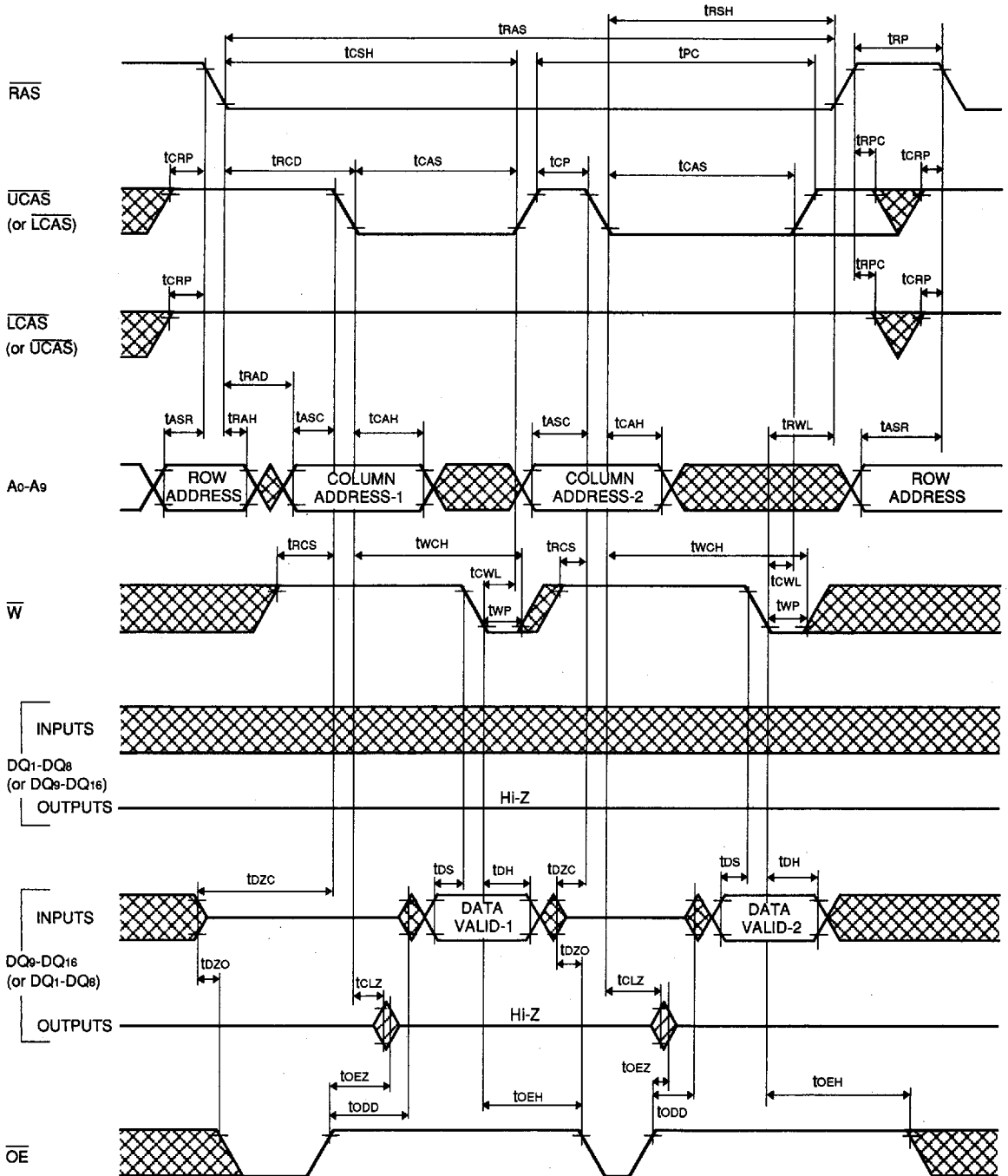


6249825 0028764 366





Fast Page Mode Upper / (Lower) Byte Write ( Delayed Write )



6249825 0028766 139







# M5M418160BJ, TP-6,-7,-6S,-7S

FAST PAGE MODE 16777216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

## SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -6S / -7S. The other characteristics and requirements than the below are same as normal devices.

## ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=5V ±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I <sub>cca</sub>	Supply current from V <sub>cc</sub> Extended refresh cycle	M5M418160B -6S,-7S  R <sub>AS</sub> cycling C <sub>AS</sub> ≤ 0.2V or C <sub>AS</sub> before R <sub>AS</sub> refresh cycling W ≤ 0.2V or ≥ V <sub>cc</sub> - 0.2V OE ≤ 0.2V or ≥ V <sub>cc</sub> - 0.2V A <sub>0</sub> ~A <sub>9</sub> ≤ 0.2V or ≥ V <sub>cc</sub> - 0.2V DQ = open I <sub>REF</sub> = 128ms I <sub>RAS</sub> = t <sub>RAS</sub> min ~ 1 μs			500	μA
I <sub>cc9</sub> (AV)	Average supply current from V <sub>cc</sub> Self-Refresh cycle	M5M418160B -6S,-7S  R <sub>AS</sub> = C <sub>AS</sub> ≤ 0.2V			400	μA

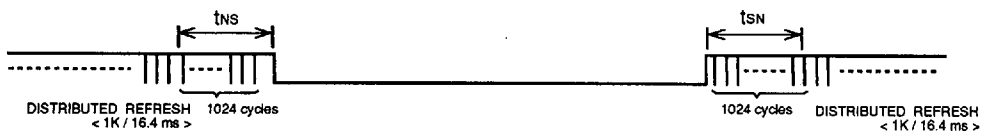
## TIMING REQUIREMENTS (Ta=0~70°C, Vcc=5V ±10%, Vss=0V, unless otherwise noted See notes 13,14)

Symbol	Parameter	Limits				Unit
		M5M418160B-6S		M5M418160B-7S		
		Min	Max	Min	Max	
t <sub>RASS</sub>	Self Refresh R <sub>AS</sub> low pulse width	100		100		μs
t <sub>RPS</sub>	Self Refresh R <sub>AS</sub> high precharge time	90		110		ns
t <sub>CHS</sub>	Self Refresh R <sub>AS</sub> hold time	-50		-50		ns

## SELF REFRESH ENTRY & EXIT CONDITIONS

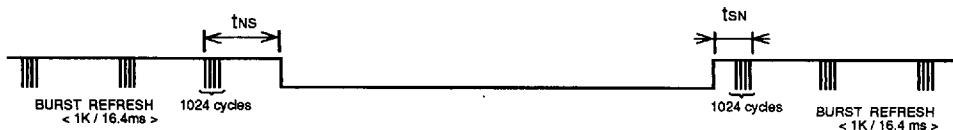
### (1) In case of distributed refresh

The last / first full refresh cycles (1K) must be made within t<sub>ns</sub> / t<sub>sn</sub> before / after self refresh, on the condition of t<sub>ns</sub> ≤ 16.4 ms and t<sub>sn</sub> ≤ 16.4 ms.



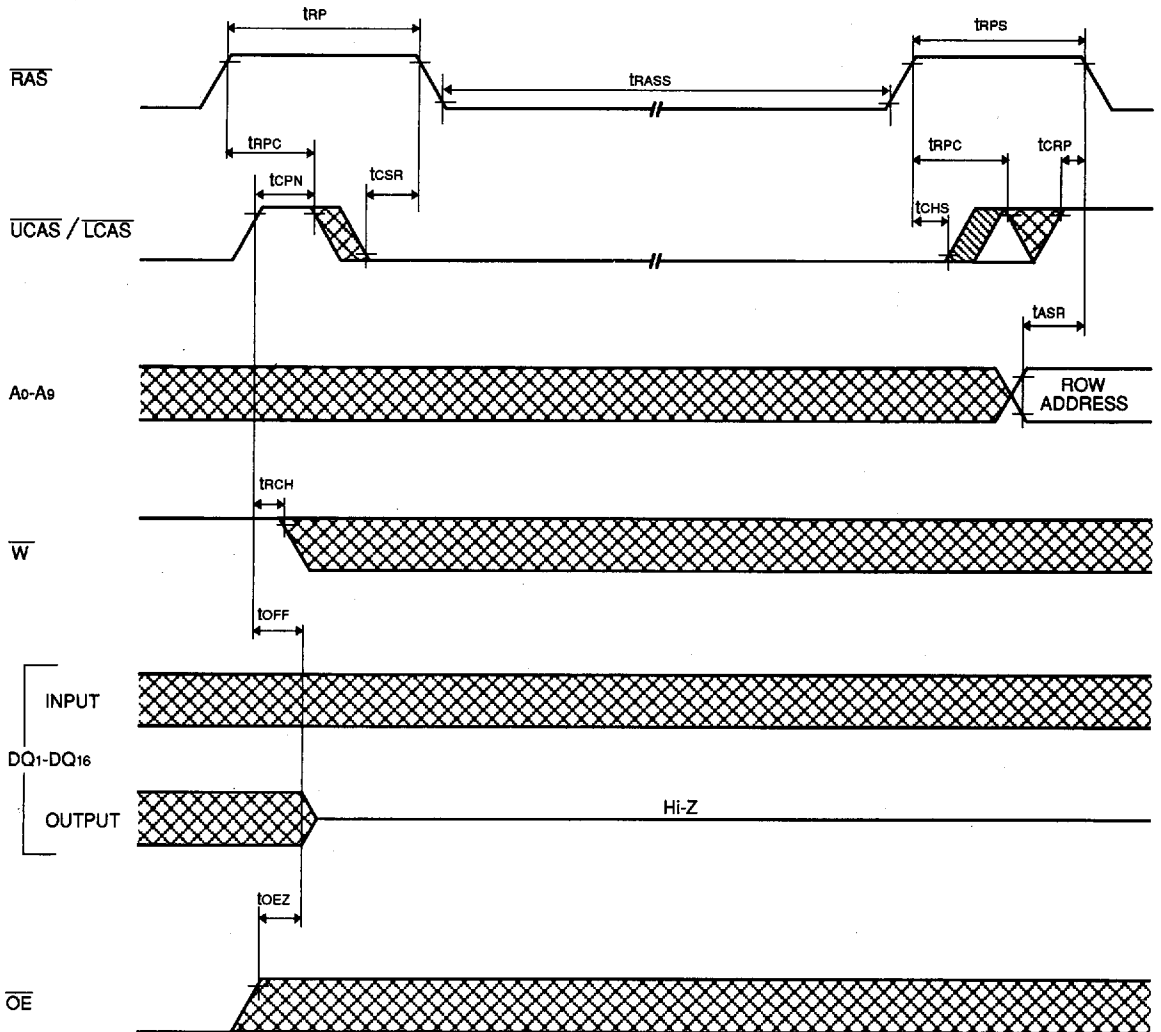
### (2) In case of burst refresh

The last / first full refresh cycles (1K) must be made within t<sub>ns</sub> / t<sub>sn</sub> before / after self refresh, on the condition of t<sub>ns</sub> + t<sub>sn</sub> ≤ 16.4 ms.



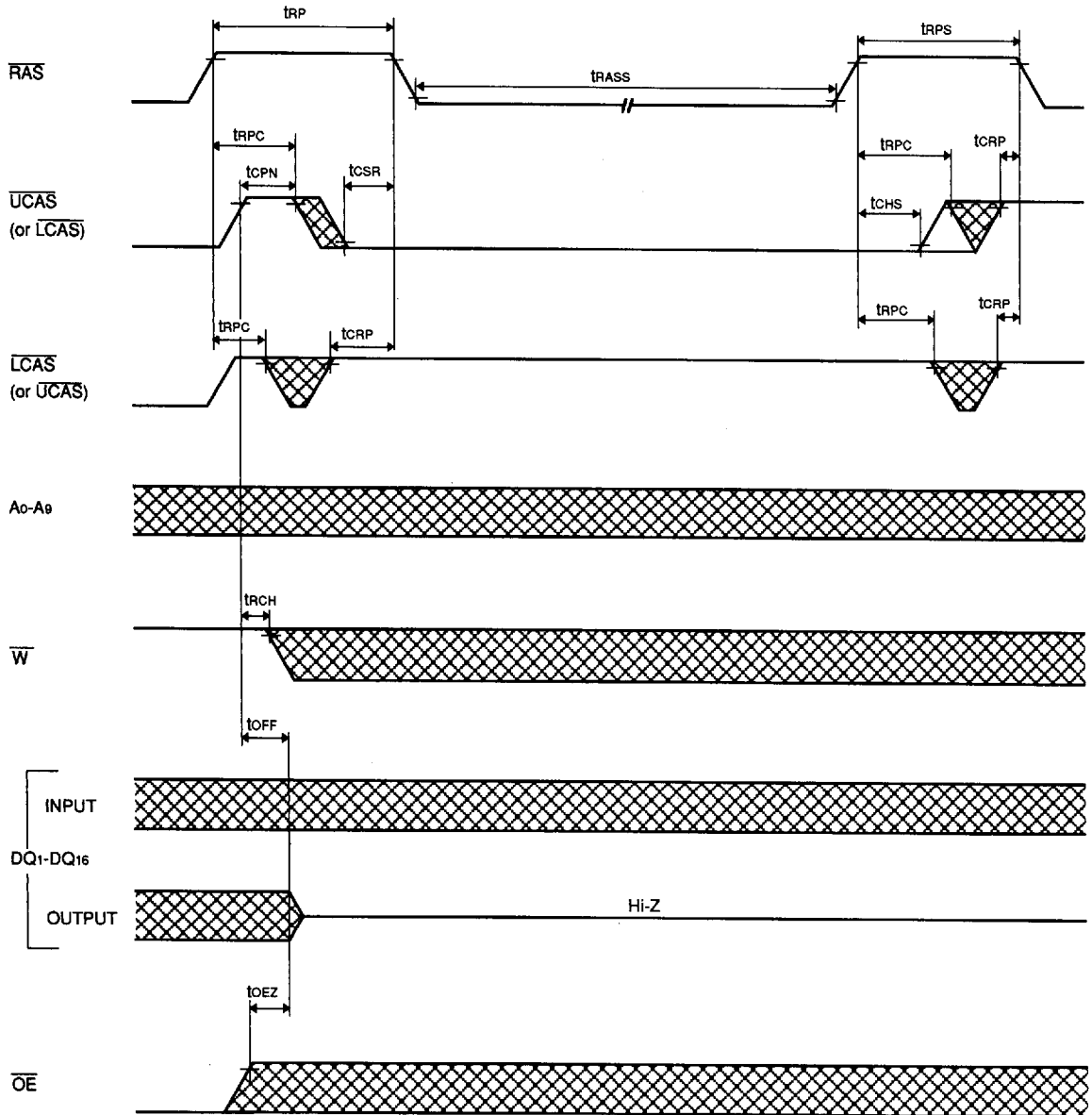
6249825 0028769 948

Self Refresh Cycle



■ 6249825 0028770 66T ■

**Upper/(Lower) Self Refresh Cycle\***



■ 6249825 0028771 5T6 ■