

# SRAM

# 128K x 8 SRAM

  
WITH SINGLE CHIP ENABLE

## AVAILABLE AS MILITARY SPECIFICATIONS

- SMD 5962-89598
- MIL-STD-883

## FEATURES

- Ultra high speed: 15ns
- High speed: 20, 25, 35 and 45ns
- Battery Backup: 2V data retention
- Low power standby
- High-performance, low-power CMOS process
- Single +5V ( $\pm 10\%$ ) power supply
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  options
- All inputs and outputs are TTL compatible

## OPTIONS

- Timing
  - 15ns access (contact factory)
  - 20ns access
  - 25ns access
  - 35ns access
  - 45ns access
  - 55ns access
  - 70ns access

- Packages
  - Ceramic DIP (400 mil)
  - Ceramic DIP (600 mil)
  - Ceramic LCC
  - Ceramic LCC
  - Ceramic Flat Pack
  - Ceramic SOJ

- 2V data retention, low power standby
- Radiation Tolerant (EPI)

## MARKING

-15 (New)
-20
-25
-35
-45
-55*
-70*

\*Electrical characteristics identical to those provided for the 45ns access devices.

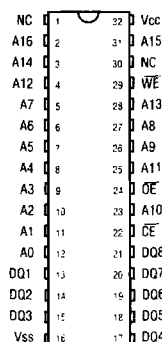
## GENERAL DESCRIPTION

The Austin Semiconductor SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Austin Semiconductor SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

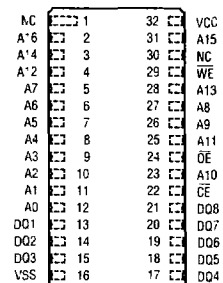
For flexibility in high-speed memory applications, Austin Semiconductor offers chip enable ( $\overline{CE}$ ) and output enable ( $\overline{OE}$ ) capability. These enhancements can place the outputs in High-Z for additional flexibility in system design.

## PIN ASSIGNMENT (Top View)

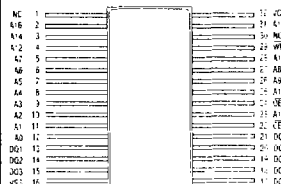
### 32-Pin DIP



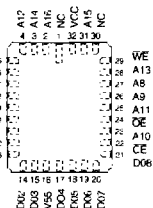
### 32-Pin LCC 32-Pin SOJ



### 32-Pin Flat Pack



### 32-Pin LCC



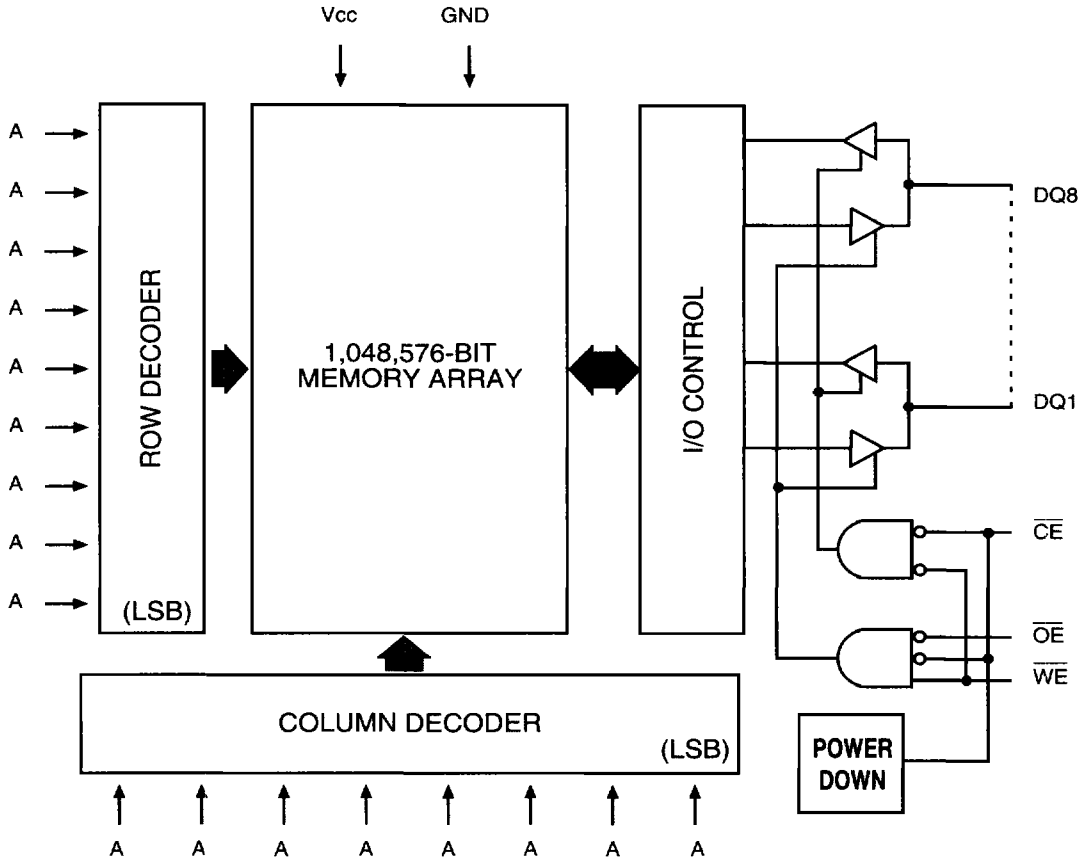
Writing to these devices is accomplished when write enable ( $\overline{WE}$ ) and  $\overline{CE}$  inputs are both LOW. Reading is accomplished when  $\overline{WE}$  remains HIGH while  $\overline{CE}$  and  $\overline{OE}$  go LOW. The devices offer a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

The "L" version provides an approximate 50 percent reduction in CMOS standby current ( $I_{SBCC}$ ) over the standard version.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.



FUNCTIONAL BLOCK DIAGRAM



**NOTE:** The two least significant row address bits (A8 and A6) are encoded using gray code.

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE



**ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Input or DQ Relative to Vss .. -5V to VCC+1V  
 Voltage on Vcc Supply Relative to Vss ..... -1V to +7V  
 Storage Temperature ..... -65°C to +150°C  
 Power Dissipation ..... 1W  
 Short Circuit Output Current ..... 20mA  
 Load Temperature (soldering temperature) ..... +260°C  
 Junction Temperature ..... +175°C

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

(-55°C ≤ T<sub>C</sub> ≤ 125°C; V<sub>CC</sub> = 5.0V ± 10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V <sub>IH</sub>	2.2	V <sub>CC</sub> +0.5	V	1
Input Low (Logic 0) Voltage		V <sub>IL</sub>	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	I <sub>LI</sub>	-5	5	μA	
Output Leakage Current	Output Disabled 0V ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub>	I <sub>LO</sub>	-5	5	μA	
Output High Voltage	I <sub>OH</sub> = -4.0mA	V <sub>OH</sub>	2.4		V	1
Output Low Voltage	I <sub>OL</sub> = 8.0mA	V <sub>OL</sub>		0.4	V	1

DESCRIPTION	CONDITIONS	SYMBOL	MAX					UNITS	NOTES
			-15	-20	-25	-35	-45		
Power Supply Current: Operating	$\overline{CE} \leq V_{IL}$ ; V <sub>CC</sub> = MAX f = MAX = 1/τ <sub>RC</sub> (MIN) Output Open	I <sub>CC</sub>	170	155	140	130	125	mA	3
Power Supply Current: Standby	$\overline{CE} \geq V_{IH}$ ; V <sub>CC</sub> = MAX f = MAX = 1/τ <sub>RC</sub> (MIN) Output Open	I <sub>SBT1</sub>	65	50	45	40	35	mA	
	$\overline{CE} \geq V_{IH}$ , All Other Inputs ≤ V <sub>IL</sub> or ≥ V <sub>IH</sub> , V <sub>CC</sub> = MAX f = 0 Hz	I <sub>SBT2</sub>	25	25	25	25	25	mA	
	$\overline{CE} \geq V_{CC} - 0.2V$ ; V <sub>CC</sub> = MAX V <sub>IL</sub> ≤ V <sub>SS</sub> + 0.2V V <sub>IH</sub> ≥ V <sub>CC</sub> - 0.2V; f = 0 Hz	I <sub>SBC2</sub>	10	10	10	10	10	mA	
	"L" Version Only	I <sub>SBC2</sub>	5	5	5	5	5	mA	

**CAPACITANCE**

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance ( $\overline{OE}$ , A2, A3, A10)	T <sub>A</sub> = 25°C, f = 1MHz V <sub>CC</sub> = 5V	C <sub>i</sub>		10	pF	4
Output Capacitance (DQ1-DQ8)		C <sub>o</sub>		8	pF	4
Input Capacitance (All Other Inputs)		C <sub>i</sub>		8	pF	4



**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Note 5) (-55°C ≤ T<sub>C</sub> ≤ 125°C; V<sub>CC</sub> = 5V ± 10%)

DESCRIPTION	SYM	-15		-20		-25		-35		-45		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
<b>READ Cycle</b>													
READ cycle time	<sup>t</sup> RC	15		20		25		35		45		ns	
Address access time	<sup>t</sup> AA		15		20		25		35		45	ns	
Chip Enable access time	<sup>t</sup> ACE		15		20		25		35		45	ns	
Output hold from address change	<sup>t</sup> OH	3		3		3		3		3		ns	
Chip Enable to output in Low-Z	<sup>t</sup> LZCE	3		3		3		3		3		ns	4, 6, 7
Chip disable to output in High-Z	<sup>t</sup> HZCE		6		8		10		15		15	ns	4, 6, 7
Chip Enable to power-up time	<sup>t</sup> PU	0		0		0		0		0		ns	4
Chip disable to power-down time	<sup>t</sup> PD		15		20		25		35		45	ns	4
Output Enable access time	<sup>t</sup> AOE		6		7		8		12		12	ns	
Output Enable to output in Low-Z	<sup>t</sup> LZOE	0		0		0		0		0		ns	
Output disable to output in High-Z	<sup>t</sup> HZOE		5		7		9		12		12	ns	4, 6, 7
<b>WRITE Cycle</b>													
WRITE cycle time	<sup>t</sup> WC	15		20		25		35		45		ns	
Chip Enable to end of write	<sup>t</sup> CW	12		15		17		20		25		ns	
Address valid to end of write	<sup>t</sup> AW	12		15		17		20		20		ns	
Address setup time	<sup>t</sup> AS	0		0		0		0		0		ns	
Address hold from end of write	<sup>t</sup> AH	1		1		1		1		1		ns	
WRITE pulse width	<sup>t</sup> WP	12		15		17		20		20		ns	
Data setup time	<sup>t</sup> DS	7		8		10		13		13		ns	
Data hold time	<sup>t</sup> DH	0		0		0		0		0		ns	
Write disable to output in Low-Z	<sup>t</sup> LZWE	3		3		3		3		3		ns	4, 6, 7
Write Enable to output in High-Z	<sup>t</sup> HZWE	0	7	0	9	0	10	0	13	0	13	ns	4, 6, 7



**AC TEST CONDITIONS**

Input pulse levels .....	Vss to 3V
Input rise and fall times .....	5ns
Input timing reference levels .....	1.5V
Output reference levels .....	1.5V
Output load .....	See Figures 1 and 2

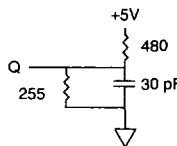


Fig. 1 OUTPUT LOAD EQUIVALENT

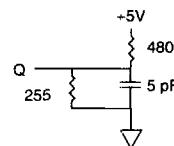


Fig. 2 OUTPUT LOAD EQUIVALENT

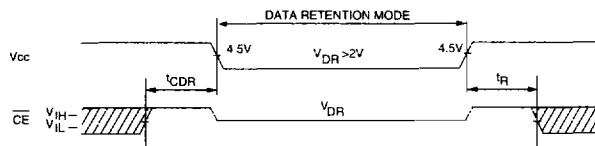
**NOTES**

- All voltages referenced to Vss (GND).
- 2V for pulse width < 20ns.
- Icc is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and  $f = \frac{1}{t_{RC} (MIN)}$  Hz.
- This parameter is guaranteed but not tested.
- Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- $t_{LZCE}$ ,  $t_{LZOE}$ ,  $t_{LZWE}$ ,  $t_{HZCE}$ ,  $t_{HZOE}$  and  $t_{HZWE}$  are specified with  $C_L = 5$  pF as in Fig. 2. Transition is measured  $\pm 200$ mV typical from steady state voltage, allowing for actual tester RC time constant.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$  and  $t_{HZWE}$  is less than  $t_{LZWE}$ , and  $t_{HZOE}$  is less than  $t_{LZOE}$ .
- $\overline{WE}$  is HIGH for READ cycle.
- Device is continuously selected. Chip enable and output enable are held in their active state.
- Address valid prior to or coincident with latest occurring chip enable.
- $t_{RC}$  = READ cycle time.
- Chip enable ( $\overline{CE}$ ) and write enable ( $\overline{WE}$ ) can initiate and terminate a WRITE cycle.

**DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)**

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Vcc for Retention Data		$V_{DR}$	2	—	V	
Data Retention Current	$\overline{CE} \geq (V_{CC} - 0.2V)$ $V_{IN} \geq (V_{CC} - 0.2V)$ or $\leq 0.2V$	$V_{CC} = 2V$ $I_{CCDR}$		1.0	mA	
		$V_{CC} = 3V$		1.5	mA	
Chip Deselect to Data Retention Time		$t_{CDR}$	0	—	ns	4
Operation Recovery Time		$t_R$	$t_{RC}$		ns	4, 11

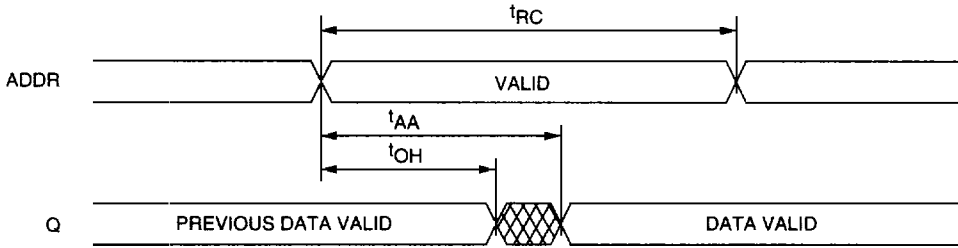
**LOW Vcc DATA RETENTION WAVEFORM**



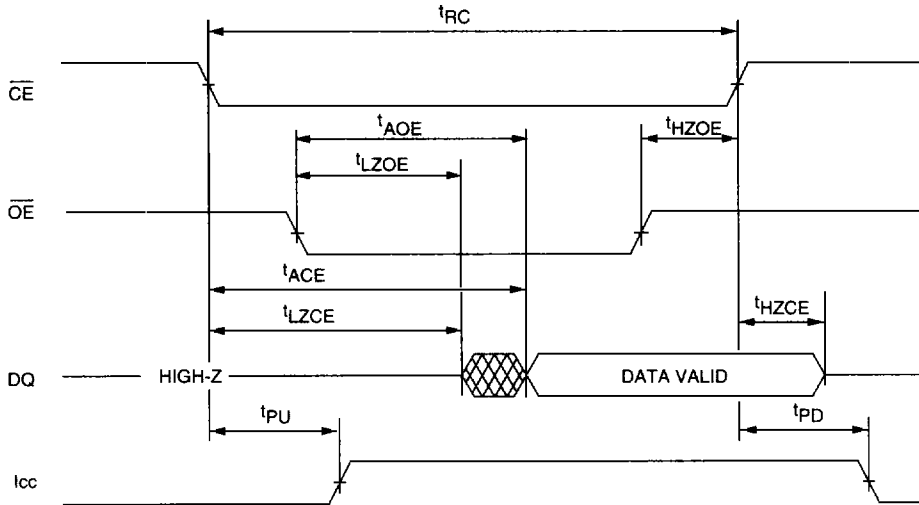
DON'T CARE  
 UNDEFINED



READ CYCLE NO. 1 8, 9



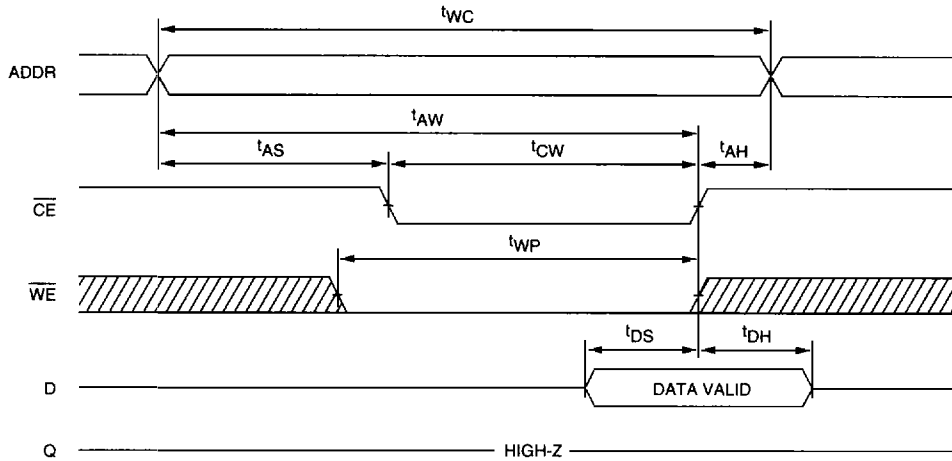
READ CYCLE NO. 2 7, 8, 10



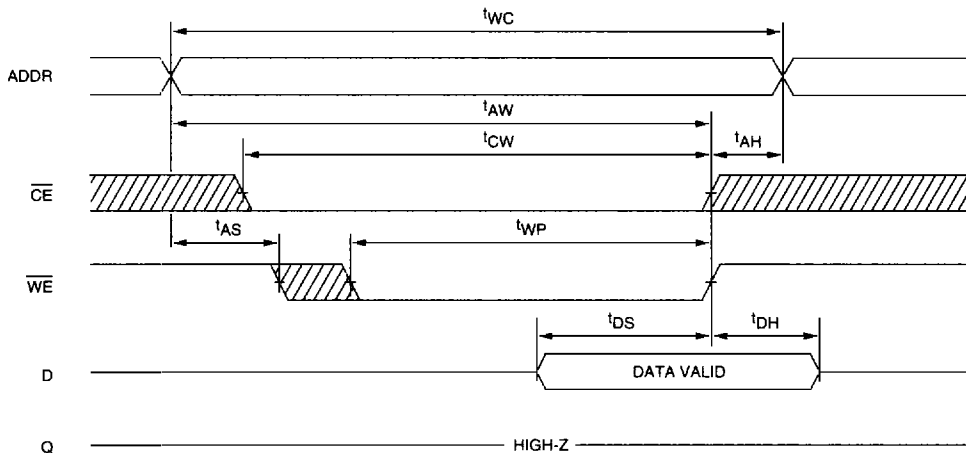
DON'T CARE  
 UNDEFINED



**WRITE CYCLE NO. 1** <sup>12</sup>  
(Chip Enable Controlled)



**WRITE CYCLE NO. 2** <sup>7, 12</sup>  
(Write Enable Controlled)



 DON'T CARE

 UNDEFINED

**NOTE:** Output enable ( $\overline{OE}$ ) is inactive (HIGH).



**ELECTRICAL TEST REQUIREMENTS**

<b>MIL-STD-883 TEST REQUIREMENTS</b>	<b>SUBGROUPS (per Method 5005, Table I)</b>
INTERIM ELECTRICAL (PRE-BURN-IN) TEST PARAMETERS (Method 5004)	2, 8A, 10
FINAL ELECTRICAL TEST PARAMETERS (Method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
GROUP A TEST REQUIREMENTS (Method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11
GROUP C AND D END-POINT ELECTRICAL PARAMETERS (Method 5005)	1, 2, 3, 7, 8, 9, 10, 11

\* PDA applies to subgroups 1 and 7.

\*\* Subgroup 4 shall be measured only for initial qualification and after process or design changes, which may affect input or output capacitance.