128Kx8 Monolithic SRAM, SMD 5962-89598

FEATURES

- Access Times of 15*, 17, 20, 25, 35, 45, 55ns
- Battery Back-up Operation
  - 2V Data Retention (EDI88130LPS)
- CS1#, CS2 & OE# Functions for Bus Control
- Inputs and Outputs Directly TTL Compatible
- Organized as 128Kx8
- Commercial, Industrial and Military Temperature Ranges
- Thru-hole and Surface Mount Packages JEDEC Pinout
  - 32 pin Sidebrazed Ceramic DIP, 400 mil (Package 102)
  - 32 pin Sidebrazed Ceramic DIP, 600 mil (Package 9)
  - 32 lead Ceramic SOJ (Package 140)
  - 32 pad Ceramic Quad LCC (Package 12)
  - 32 pad Ceramic LCC (Package 141)
  - 32 lead Ceramic Flatpack (Package 142)
- Single +5V (±10%) Supply OperationThe EDI88130CS is a high speed, high performance, 128Kx8 bits monolithic Static RAM.

An additional chip enable line provides system memory security during power down in non-battery backed up systems and memory banking in high speed battery backed systems where large multiple pages of memory are required.

The EDI88130CS has eight bi-directional input-output lines to provide simultaneous access to all bits in a word.

A low power version, EDI88130LPS, offers a 2V data retention function for battery back-up applications.

Military product is available compliant to MIL-PRF-38535.

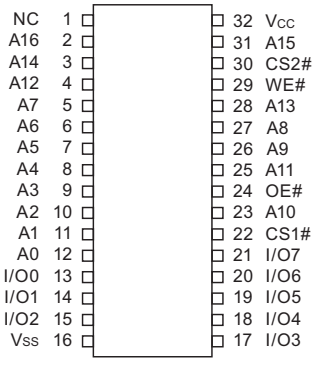
* 15ns access time is advanced information, contact factory for availability.

This product is subject to change without notice.

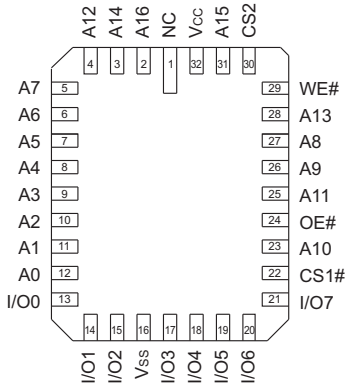
FIGURE 1 – PIN CONFIGURATION

32 DIP
32 SOJ
32 CLCC
32 FLATPACK

TOP VIEW



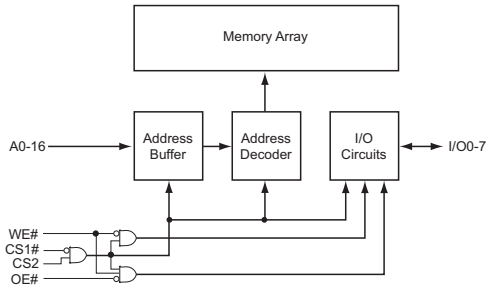
32 QUAD LCC
TOP VIEW



PIN DESCRIPTION

I/O0-7	Data Input/Output
A0-16	Address Inputs
WE#	Write Enable
CS1#, CS2	Chip Select
OE#	Output Enable
VCC	Power Supply
VSS	Ground
NC	Not Connected

Block Diagram



ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Voltage on any pin relative to V_{SS}	-0.2 to 7.0	V
Operating Temperature T_A (Ambient)		
Industrial	-40 to +85	°C
Military	-55 to +125	°C
Storage Temperature, Ceramic	-65 to +150	°C
Power Dissipation	1.7	W
Output Current	40	mA
Junction Temperature, T_J	175	°C

NOTE:
Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

OE#	CS1#	CS2	WE#	Mode	Output	Power
X	H	X	X	Standby	High Z	Icc2, Icc3
X	X	L	X	Standby	High Z	Icc2, Icc3
H	L	H	H	Output Deselect	High Z	Icc1
L	L	H	H	Read	Data Out	Icc1
X	L	H	L	Write	Data In	Icc1

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} +0.5	V
Input Low Voltage	V_{IL}	-0.5	—	+0.8	V

CAPACITANCE

T_A = +25°C

Parameter	Symbol	Condition	Max		Unit
			LCC	CSOJ,DIP, Flatpack	
Address Lines	C_I	V_{IN} = Vcc or Vss, f = 1.0MHz	6	12	pF
Data Lines	C_O	V_{OUT} = Vcc or Vss, f = 1.0MHz	8	14	pF

These parameters are sampled, not 100% tested.

DC CHARACTERISTICS

V_{CC} = 5.0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Input Leakage Current	I_{LI}	V_{IN} = 0V to V_{CC}		—	—	±5	µA
Output Leakage Current	I_{LO}	$V_{I/O}$ = 0V to V_{CC}		—	—	±10	µA
Operating Power Supply Current	Icc1	WE# = V_{IH}, CS1# = V_{IL}, $I_{I/O}$ = 0mA, CS2 = V_{IH}	(15-17ns)	—		300	mA
			(20ns)	—		225	mA
			(25-55ns)	—		200	mA
Standby (TTL) Power Supply Current	Icc2	CS1# ≥ V_{IH} and/or CS2 ≤ V_{IL},	(17-55ns)	—		25	mA
		V_{IN} ≥ V_{IH} or ≤ V_{IL}, f = 0	(15ns)	—		60	mA
Full Standby Power Supply Current	Icc3	CS1# ≥ V_{CC} -0.2V and/or CS2 ≤ 0.2V	CS (17-55ns)	—	3	10	mA
			CS (15ns)	—	—	15	mA
		V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V, f = 0	LPS	—	—	5	mA
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA		—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA		2.4	—	—	V

AC Test Conditions

Figure 1

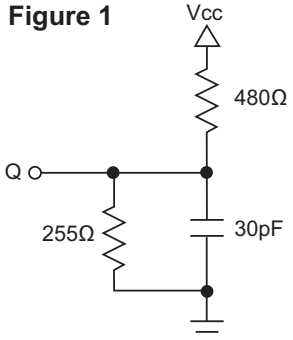
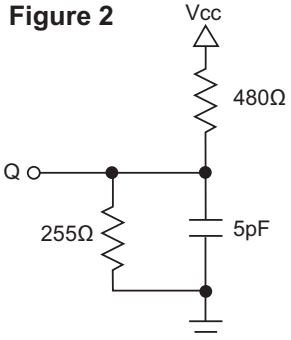


Figure 2



Input Pulse Levels	V_{SS} to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

NOTE: For t_{EHQZ}, t_{GHQZ} and t_{WLQZ}, CL = 5pF Figure 2

AC CHARACTERISTICS – READ CYCLE (15 to 20ns)

V_{CC} = 5.0V, Vss = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		15ns*		17ns		20ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	15		17		20		ns
Address Access Time	t_{AVQV}	t_{AA}		15		17		20	ns
Chip Enable Access Time	t_{E1LQV} t_{E2HQV}	t_{ACS} t_{ACS}		15 15		17 17		20 20	ns ns
Chip Enable to Output in Low Z (1)	t_{E1LQX} t_{E2HQX}	t_{CLZ} t_{CLZ}	5 5		5 5		5 5		ns ns
Chip Disable to Output in Low Z (1)	t_{E1HQZ} t_{E2LQZ}	t_{CHZ} t_{CHZ}		6 6		7 7		8 8	ns ns
Output Hold from Address Change	t_{AVQX}	t_{OH}	3		3		3		ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		6		6		7	ns
Output Enable to Output in Low Z (1)	t_{GLQX}	t_{OLZ}	0		0		0		ns
Output Disable to Output in High Z(1)	t_{GHQZ}	t_{OHZ}		5		6		8	ns
Chip Enable to Power Up (1)	$t_{E1LICCH}$ $t_{E2HICCH}$	t_{PU} t_{PU}	0 0		0 0		0 0		ns ns
Chip Enable to Power Down (1)	$t_{E1HICCL}$ $t_{E2LICCL}$	t_{PD} t_{PD}		15 15		17 17		20 20	ns ns

1. This parameter is guaranteed by design but not tested.
* 15ns access time is advanced information, contact factory for availability.

AC CHARACTERISTICS – READ CYCLE (25 to 55ns)

V_{CC} = 5.0V, Vss = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		25ns		35ns		45ns		55ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	25		35		45		55		ns
Address Access Time	t_{AVQV}	t_{AA}		25		35		45		55	ns
Chip Enable Access Time	t_{E1LQV}	t_{ACS}		25		35		45		55	ns
Chip Enable Access Time	t_{E2HQV}	t_{ACS}		25		35		45		55	ns
Chip Enable to Output in Low Z (1)	t_{E1LQX} t_{E2HQX}	t_{CLZ} t_{CLZ}	5 5		5 5		5 5		5 5		ns ns
Chip Disable to Output in Low Z (1)	t_{E1HQZ} t_{E2LQZ}	t_{CHZ} t_{CHZ}		10 10		15 15		20 20		20 20	ns ns
Output Hold from Address Change	t_{AVQX}	t_{OH}	0		0		0		0		ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		10		15		20		25	ns
Output Enable to Output in Low Z (1)	t_{GLQX}	t_{OLZ}	0		0		0		0		ns
Output Disable to Output in High Z(1)	t_{GHQZ}	t_{OHZ}		10		15		20		20	ns
Chip Enable to Power Up (1)	$t_{E1LICCH}$ $t_{E2HICCH}$	t_{PU} t_{PU}	0 0		0 0		0 0		0 0		ns ns
Chip Enable to Power Down (1)	$t_{E1HICCL}$ $t_{E2LICCL}$	t_{PD} t_{PD}		25 25		35 35		45 45		55 55	ns ns

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS – WRITE CYCLE (15 to 20ns)

V_{CC} = 5.0V, Vss = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol JEDEC	Symbol Alt.	15ns* Min	15ns* Max	17ns Min	17ns Max	20ns Min	20ns Max	Units
Write Cycle Time	t_{AVAV}	t_{WC}	15		17		20		ns
Chip Enable to End of Write	t_{E1LWH}	t_{CW}	12		13		15		ns
	t_{E1LE1H}	t_{CW}	12		13		15		ns
	t_{E2HWH}	t_{CW}	12		13		15		ns
	t_{E2HE2L}	t_{CW}	12		13		15		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		ns
	t_{AVE1L}	t_{AS}	0		0		0		ns
	t_{AVE2H}	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AVWH}	t_{AW}	12		13		15		ns
Write Pulse Width	t_{WLWH}	t_{WP}	12		13		15		ns
	t_{WLE1H}	t_{WP}	12		13		15		ns
	t_{WLE2L}	t_{WP}	12		13		15		ns
Write Recovery Time	t_{WHAX}	t_{WR}	0		0		0		ns
	t_{E1HAX}	t_{WR}	0		0		0		ns
	t_{E2LAX}	t_{WR}	0		0		0		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		ns
	t_{E1HDX}	t_{DH}	0		0		0		ns
	t_{E2LDX}	t_{DH}	0		0		0		ns
Write to Output in High Z (1)	t_{WLQZ}	t_{WHZ}	0	7	0	8	0	8	ns
Data to Write Time	t_{DVWH}	t_{DW}	7		8		10		ns
	t_{DVE1H}	t_{DW}	7		8		10		ns
	t_{DVE2L}	t_{DW}	7		8		10		ns
Output Active from End of Write (1)	t_{WHQX}	t_{WLZ}	3		3		3		ns

1. This parameter is guaranteed by design but not tested.

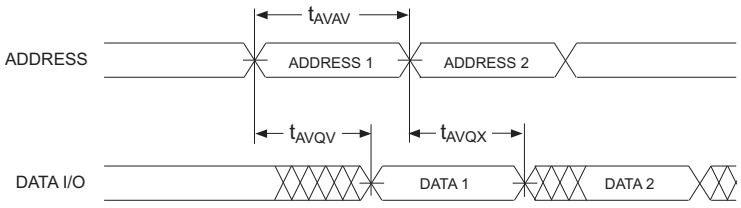
AC CHARACTERISTICS – WRITE CYCLE (25 to 55ns)

V_{CC} = 5.0V, Vss = 0V, -55°C ≤ T_A ≤ +125°C

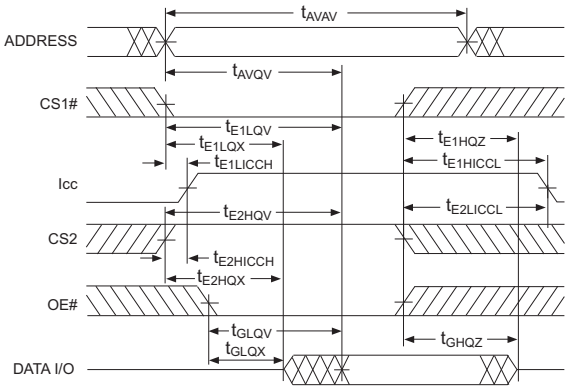
Parameter	Symbol JEDEC	Symbol Alt.	25ns Min	25ns Max	35ns Min	35ns Max	45ns Min	45ns Max	55ns Min	55ns Max	Units
Write Cycle Time	t_{AVAV}	t_{WC}	25		35		45		55		ns
Chip Enable to End of Write	t_{E1LWH}	t_{CW}	20		25		35		45		ns
	t_{E1LE1H}	t_{CW}		16		20		25		40	ns
	t_{E2HWH}	t_{CW}	16		20		25		40		ns
	t_{E2HE2L}	t_{CW}		16		20		25		40	ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		0		ns
	t_{AVE1L}	t_{AS}	0		0		0		0		ns
	t_{AVE2H}	t_{AS}	0		0		0		0		ns
Address Valid to End of Write	t_{AVWH}	t_{AW}	20		25		35		45		ns
	t_{AVEH}	t_{AW}	20		25		35		45		ns
Write Pulse Width	t_{WLWH}	t_{WP}	20		30		30		35		ns
	t_{WLE1H}	t_{WP}	20		30		30		35		ns
	t_{WLE2L}	t_{WP}	20		30		30		35		ns
Write Recovery Time	t_{WHAX}	t_{WR}	0		0		5		5		ns
	t_{E1HAX}	t_{WR}	0		0		5		5		ns
	t_{E2LAX}	t_{WR}	0		0		5		5		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		0		ns
	t_{E1HDX}	t_{DH}	0		0		0		0		ns
	t_{E2LDX}	t_{DH}	0		0		0		0		ns
Write to Output in High Z (1)	t_{WLQZ}	t_{WHZ}	0	10	0	13	0	15	0	20	ns
Data to Write Time	t_{DVWH}	t_{DW}	15		20		20		25		ns
	t_{DVE1H}	t_{DW}	15		20		20		25		ns
	t_{DVE2L}	t_{DW}	15		20		20		25		ns
Output Active from End of Write (1)	t_{WHQX}	t_{WLZ}	3		3		3		3		ns

1. This parameter is guaranteed by design but not tested.

FIGURE 2 – TIMING WAVEFORM – READ CYCLES

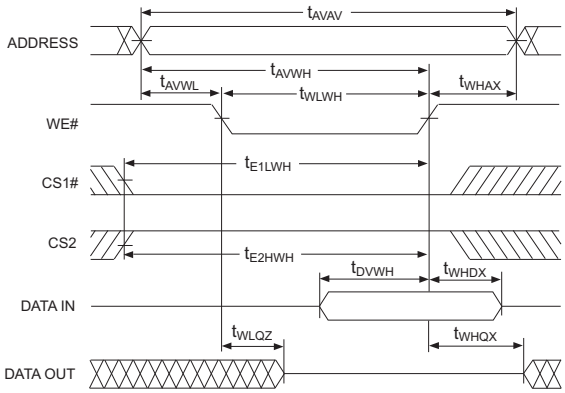


READ CYCLE 1 (WE# HIGH; OE#, CS# LOW)



READ CYCLE 2 (CS1# AND/OR CS2 CONTROLLED, WE# HIGH)

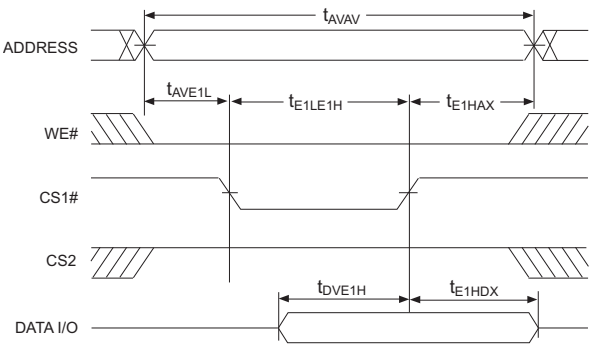
FIGURE 3 – WRITE CYCLE 1



WRITE CYCLE 1 - LATE WRITE, WE# CONTROLLED

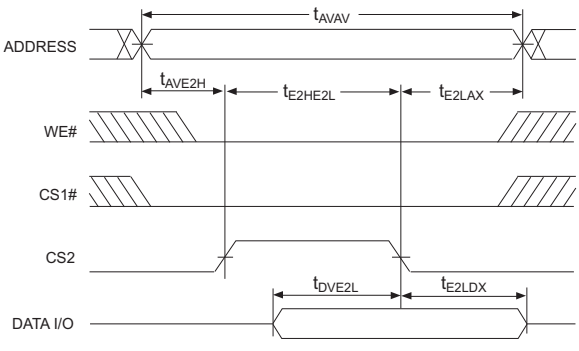
FIGURE 4 –

WRITE CYCLES 2



WRITE CYCLE 2 – EARLY WRITE, CS1# CONTROLLED

WRITE CYCLES 3



WRITE CYCLE 3 – EARLY WRITE, CS2 CONTROLLED

DATA RETENTION CHARACTERISTICS (EDI88130LPS Only)

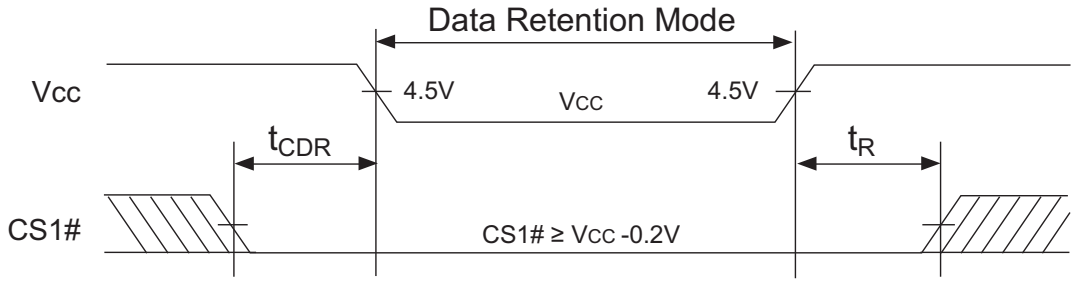
-55°C ≤ T_A ≤ +125°C

Characteristic Low Power Version only	Sym	Conditions	Min	Typ	Max	Units
Data Retention Voltage	V_{CC}	V_{CC} = 2.0V	2	–	–	V
Data Retention Quiescent Current	I_{CCDR}	CS1# ≥ V_{CC} -0.2V and/or CS2 ≥ V_{SS} +0.2V	–	0.5	2	mA
Chip Disable to Data Retention Time (1)	T_{CDR}	V_{IN} ≥ V_{CC} -0.2V	0	–	–	ns
Operation Recovery Time (1)	T_R	or V_{IN} ≤ 0.2V	Tavav*	–	–	ns

NOTE:
1. Parameter guaranteed by design, but not tested.

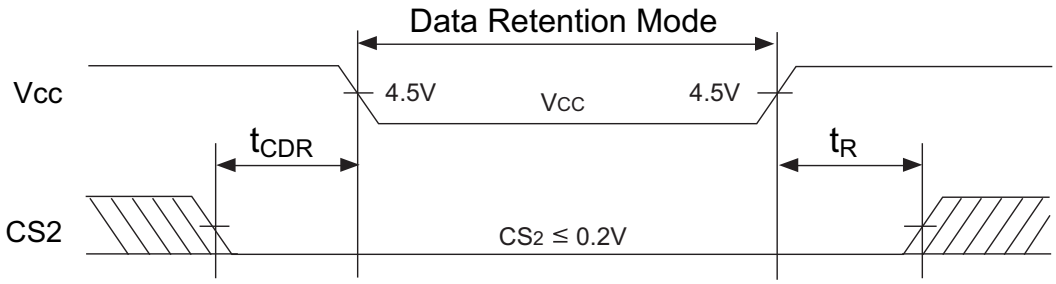
* Read Cycle Time

FIGURE 5 – DATA RETENTION – CS1# CONTROLLED



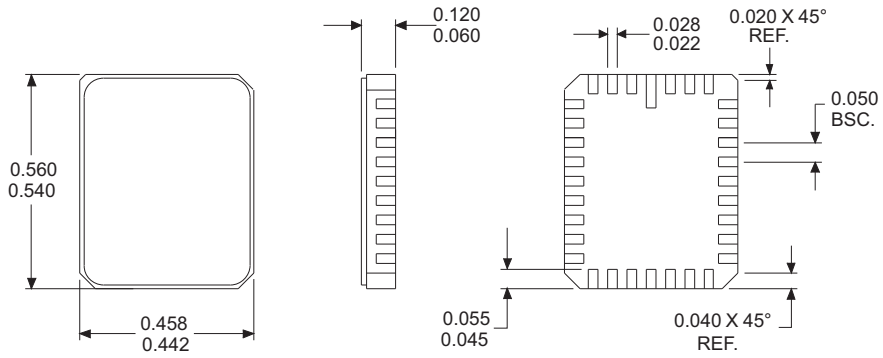
DATA RETENTION, CS1# CONTROLLED

FIGURE 6 – DATA RETENTION – CS2 CONTROLLED



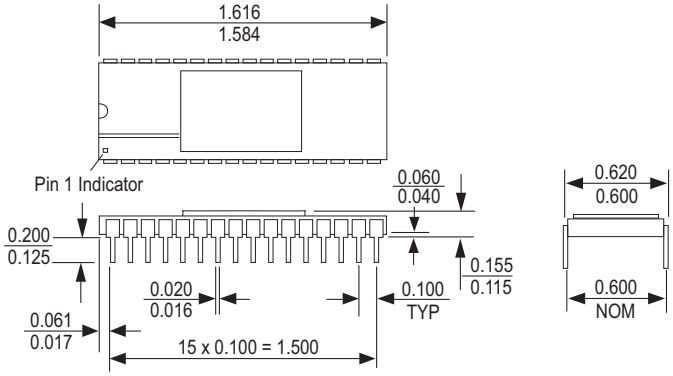
DATA RETENTION, CS2 CONTROLLED

PACKAGE 12 – 32 PIN CERAMIC QUAD LCC



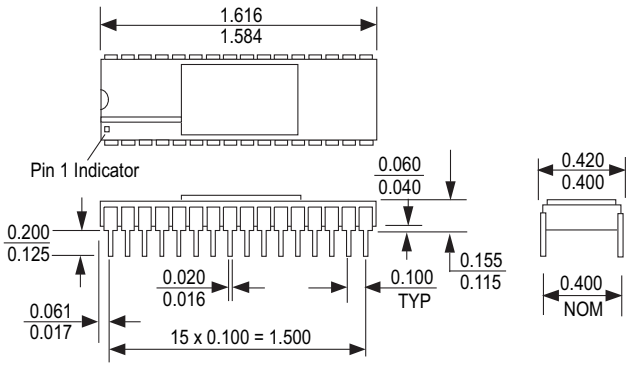
ALL DIMENSIONS ARE IN INCHES

PACKAGE 9 – 32 PIN SIDEBRAZED CERAMIC DIP (600 MILS WIDE)



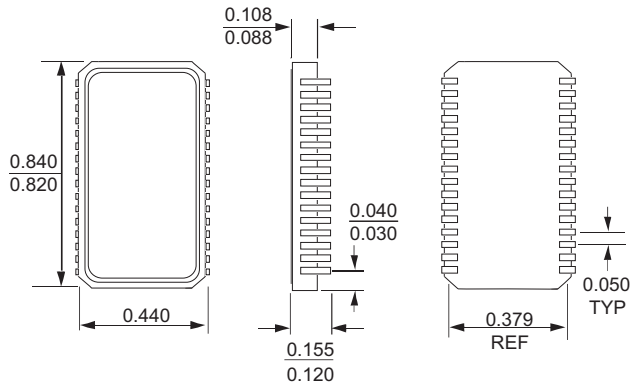
ALL DIMENSIONS ARE IN INCHES

PACKAGE 102 – 32 PIN SIDEBRAZED CERAMIC DIP (400 MILS WIDE)



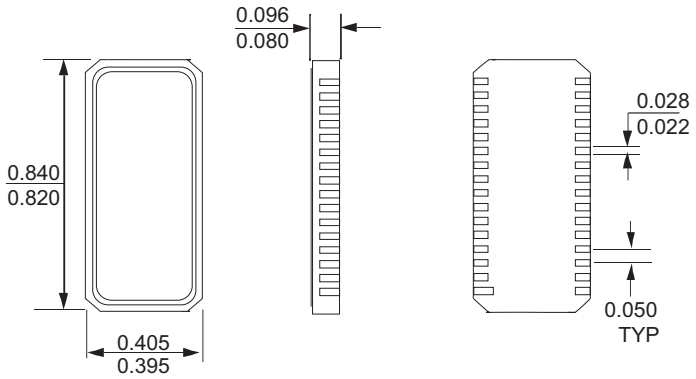
ALL DIMENSIONS ARE IN INCHES

PACKAGE 140 – 32 LEAD CERAMIC SOJ



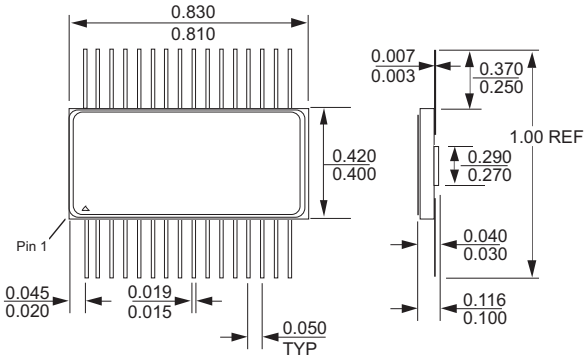
ALL DIMENSIONS ARE IN INCHES

PACKAGE 141 – 32 PAD CERAMIC LCC



ALL DIMENSIONS ARE IN INCHES

PACKAGE 142 – 32 PIN CERAMIC FLATPACK



ALL DIMENSIONS ARE IN INCHES

ORDERING INFORMATION

EDI 8 8130 CS X X X

MICROSEMI CORPORATION

SRAM

ORGANIZATION, 128Kx8
(130 = Dual CS)

TECHNOLOGY:
CS = CMOS Standard Power (5V)
LPS = Low Power

ACCESS TIME (ns)

PACKAGE TYPE:
C = 32 lead Sidebrazed DIP, 600 mil (Package 9)
F = 32 lead Ceramic Flatpack (Package 142)
L = 32 pad Ceramic LCC (Package 141)
L32 = 32 pad Ceramic Quad LCC (Package 12)
N = 32 lead Ceramic SOJ (Package 140)
T = 32 lead Sidebrazed DIP, 400 mil (Package 102)

DEVICE GRADE:
B = MIL-STD-883 Compliant
M = Military Screened -55°C to +125°C
I = Industrial -40°C to +85°C
C = Commercial 0°C to +70°C

Document Title

128Kx8 Monolithic SRAM, SMD 5962-89598

Revision History

Rev #	History	Release Date	Status
Rev 12	Changes (Pg. 1-10) 12.1 Change document layout from White Electronic Designs to Microsemi 12.2 Add document Revision History page	March 2011	Final
Rev 13	Changes (Pg. 2) 13.1 Change WE# to WE# = V_{IH} for Icc1 in the DC Characteristics chart 13.2 Add 'f = 0' to Icc2 in the DC Characteristics chart 13.3 Add 'f = 0' to Icc3 in the DC Characteristics chart	October 2011	Final