

Rochester Electronics Manufactured Components

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Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)

• Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

SN54ALS29825, SN74ALS29825, SN74ALS29826 8 BIT BUS INTERFACE FLIP DFLOPS WITH 3 DSTATE OUTPUTS

SDAS147B — JANUARY 1986 — REVISED MARCH 1990

- Functionally Equivalent to AMD AM29825 and AM29826
- Improved I_{OH} Specifications
- Multiple Output Enables Allow Multiuser Control of the Interface
- Outputs Have Undershoot Protection Circuitry
- Power-Up High-Impedance State
- Package Options Include Plastic "Small-Outline" Packages and Standard Plastic and Ceramic 300-mil DIPs
- Buffered Control Inputs to Reduce DC Loading Effect

description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing multiuser registers, I/O ports, bidirectional bus drivers, and working registers.

With the clock enable ($\overline{\text{CLKEN}}$) low, the eight D-type edge-triggered flip-flops enter data on the low-to- high transitions of the clock. Taking $\overline{\text{CLKEN}}$ high will disable the clock buffer, thus latching the outputs. The 'ALS29825 has noninverting D inputs and the 'ALS29826 has inverting $\overline{\text{D}}$ inputs. Taking the $\overline{\text{CLR}}$ input low causes the eight Q outputs to go low independently of the clock.

SN54ALS29825 JT PACKAGE
SN74ALS29825 DW OR NT PACKAGE

(TOP VIEW)									
	1 2 3 4 5 6 7 8 9 10 11 12	24 23 22 21 20 19 18 17 16 15 14 13	V _C C OC3 1Q 2Q 3Q 4Q 5Q 6Q 7Q 8Q CLKEN CLK						
, I									

SN74ALS29826 ... DW OR NT PACKAGE (TOP VIEW)

	(101	vi L vv)	
		24	Vcc
<u>OC</u> 2 [2	23	OC3
1D [3	22	1Q
2D 🛛	4	21	2Q
3D [5	20	3Q
4D 🛛	6	19	4Q
5D [7	18	5Q
6D [8	17	6Q
7D 🛛	9	16	7Q
8D [10	15	8Q
CLR	11	14	CLKEN
GND [12	13	CLK

Multiuser buffered output-control inputs ($\overline{OC1}$, $\overline{OC2}$, and $\overline{OC3}$) can be used to place the eight outputs in either a normal logic state (high or low level) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pullup components. The output controls do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS29825 is characterized over the full military range of – 55°C to 125°C. The SN74ALS29825 and SN74ALS29826 are characterized for operation from 0°C to 70°C.



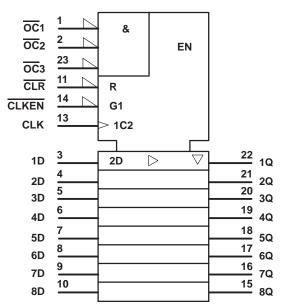
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FUNCTION TABLE							
		INPUTS			OUTPUT		
* OO	CLR	CLKEN	CLK	D	Q		
L	L	Х	Х	Х	L		
L	Н	L	↑	Н	Н		
L	Н	L	↑	L	L		
L	Н	Н	Х	Х	Q ₀		
Н	Х	Х	Х	Х	Z		

 $\overline{OC}^* = H$ if any of \overline{OC} 1, \overline{OC} 2, or \overline{OC} 3 is high. $OC^* = L$ if any of OC1, OC2, or OC3 is low.

logic symbol †



[†] This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

MISSING ILLUSTRATION



SN74ALS29826 8 BIT BUS INTERFACE FLIP - FLOPS WITH 3 STATE OUTPUTS

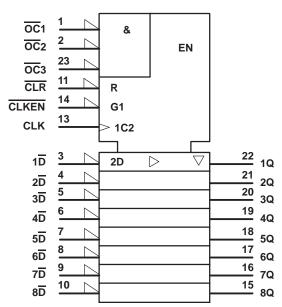
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FUNCTION TABLE

		INPUTS			OUTPUT
* OO	CLR	CLKEN	CLK	D	Q
L	L	Х	Х	Х	L
L	Н	L	\uparrow	Н	Н
L	Н	L	\uparrow	L	L
L	Н	Н	Х	Х	Q ₀
Н	Х	Х	Х	Х	Z

 $\overline{OC}^* = H$ if any of $\overline{OC}1$, $\overline{OC}2$, or $\overline{OC}3$ is high. $OC^* = L$ if any of OC1, OC2, or OC3 is low.

logic symbol †



[†] This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

MISSING ILLUSTRATION



SN54ALS29825 8 BIT BUS INTERFACE FLIP FLOPS WITH 3 STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise no	ted) †
Supply voltage, V _{CC} (see Note 1)	7V
Input voltage	7V
Voltage applied to a disabled high-impedance output	5.5 V
Operating free-air temperature range – 55°C to	125°C
Storage temperature range	150°C

[†] Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage			5		4.75	5	5.5	V
VIH	High-level input voltage					2			V
V_{IL}	Low-level input voltage							0.8	V
ЮН	High-level output current							- 18	mA
IOL	Low-level output current							32	mA
		CLR low	7			7			
tw	Pulse duration	CLK high	8			8			ns
		CLK low	8			8			
		CLR inactive	7			7			
t _{su}	Setup time before CLK \uparrow	Data	4			4			ns
		CLKEN high or low	8			8			
	t_h Hold time, data after CLK [↑]	Data	4			4			
۲h		CLKEN	2			2			ns
TA	Operating free-air temperature			25		- 55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [‡]	MIN	ΤΥΡ§	MAX	UNIT
VIK	V _{CC} = MIN,	^I I = – 18 mA			-1.2	V
Vou	$V_{CC} = MIN,$	^I OH = – 12 mA	2.4			V
VOH	V _{CC} = MIN,	^I OH = – 18 mA	2			v
VOL	$V_{CC} = MIN,$	IOL = 32 mA		0.35	0.5	V
IOZH	V _{CC} = MAX,	V _O = 2.4 V			50	μΑ
IOZL	V _{CC} = MAX,	$V_{O} = 0.4 V$			- 50	μΑ
lj	$V_{CC} = MAX,$	V _I = 5.5 V			0.1	mA
Iн	V _{CC} = MAX,	V _I = 2.7 V			20	μΑ
۱ _{IL}	V _{CC} = MAX,	V _I = 0.4 V			- 0.5	mA
los¶	V _{CC} = MAX,	$V_{O} = 0 V$	-75		-250	mA
ICC	V _{CC} = MAX,	Outputs open		70	115	mA

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ All typical values are at V_{CC} = 5 V, $T_A = 25^{\circ}C$.

I Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.



SN74ALS29825, SN74ALS29826 8 BIT BUS INTERFACE FLIP DFLOPS WITH 3 DSTATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwi	se noted) †
Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage	7 V
Voltage applied to a disabled high-impedance output	
Operating free-air temperature range	0°C to 70°C
Storage temperature range – 6	5°C to 150°C

[†] Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage			5		4.75	5	5.5	V
VIH	High-level input voltage					2			V
VIL	Low-level input voltage							0.8	V
ЮН	High-level output current							-24	mA
IOL	Low-level output current							48	mA
		CLR low	5			7			
tw	Pulse duration	CLK high	5			7			ns
		CLK low	5			7			
		CLR inactive	5			7			
t _{su}	Setup time before $CLK\!\uparrow$	Data	2			4			ns
		CLKEN high or low	6			6			
		Data	2			2			
th	Hold time, data after $CLK\uparrow$	CLKEN	0			2			ns
Тд	Operating free-air temperature			25		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [‡]	MIN	TYP‡	MAX	UNIT
VIK	$V_{CC} = MIN,$	lj = – 18 mA			-1.2	V
Vou	$V_{CC} = MIN,$	I _{OH} = –15 mA	2.4	3.3		V
VOH	$V_{CC} = MIN,$	$I_{OH} = -24 \text{ mA}$	2	3.1		v
VOL	$V_{CC} = MIN,$	I _{OL} = 48 mA		0.35	0.5	V
IOZH	V _{CC} = MAX,	$V_{O} = 2.4 V$			20	μA
IOZL	V _{CC} = MAX,	$V_{O} = 0.4 V$			- 20	μA
lj	V _{CC} = MAX,	VI = 5.5 V			0.1	mA
IIН	V _{CC} = MAX,	V _I = 2.7 V			20	μA
۱ _{IL}	V _{CC} = MAX,	$V_{I} = 0.4 V$			- 0.2	mA
los¶	V _{CC} = MAX,	$V_{O} = 0 V$	-75		-250	mA
ICC	V _{CC} = MAX,	Outputs open		70	100	mA

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ All typical values are at V_{CC} = 5 V, $T_A = 25^{\circ}C$.

¶Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.



SN54ALS29825 8 BIT BUS INTERFACE FLIP FLOPS WITH 3 STATE OUTPUTS

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switching characteristics over recommended ranges of supply voltage and free-air temperature

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		/CC = 5 \ [A = 25°(V, C	$V_{CC} = MIR$ $T_A = MIR$	N to MAX,† I to MAX†	UNIT	
	(INFOT)	(001F01)	(see Figure 1)	MIN	TYP	MAX	MIN	MAX		
^t PLH			C _I = 50 pF	2		8.5	2	14		
^t PHL		A O	0 <u> </u>	2		8.5	2	17.5	ns	
^t PLH	CLK	Any Q	C _I = 300 pF	2		14	2	16	110	
^t PHL				0L = 300 pi	2		17.5	2	21	
^t PHL	CLR	Any Q	C _L = 50 pF	1	6	14.5	1	17.5	ns	
^t PZH				1	11.5	14.5	1	17.5		
^t PZL	<u>oc</u>	Any O	C _L = 50 pF	1	11	13	1	18	20	
^t PZH	00	Any Q	C _L = 300 pF	1		18	1	22	ns	
^t PZL			0L = 300 pi	1		25	1	29.5		
^t PHZ			$C_{1} = 50 \text{ pF}$	1		15	1	19		
^t PLZ	OC	Any Q	C _L = 50 pF	1		10	1	12	ns	
^t PHZ	00	, any Q	CL = 5 pF	1	5.2	10	1	14	113	
^t PLZ			υ υ μι	1	5.2	9	1	11		

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



SN74ALS29825, SN74ALS29826 8 BIT BUS INTERFACE FLIP DFLOPS WITH 3 DSTATE OUTPUTS

SDAS147B — JANUARY 1986 — REVISED MARCH 1990

switching characteristics over recommended ranges of supply voltage and free-air temperature

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS (see Figure 1)	V _{CC} = 5 V, T _A = 25°C			$V_{CC} = MIN \text{ to } MAX,^{\dagger}$ T _A = MIN to MAX [†]		UNIT
				MIN	TYP	MAX	MIN	MAX	UNIT
^t PLH	CLK	Any Q	C _L = 50 pF	2		8.5	2	10	ns
^t PHL				2		8.5	2	10	
^t PLH			C _L = 300 pF			14		16	
^t PHL						14		16	
^t PHL	CLR	Any Q	CL = 50 pF		6	10		12	ns
^t PZH	ŌĊ	Any Q	C _L = 50 pF		11.5	12		14	ns -
^t PZL					11	12		14	
^t PZH			C _L = 300 pF			17		20	
^t PZL						21		23	
^t PHZ	OC	Any Q	C _L = 50 pF			11		14	ns
^t PLZ						9		12	
^t PHZ			CL = 5 pF		5.2	8		9	
^t PLZ					5.2	8		9	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



SN54ALS29825, SN74ALS29825, SN74ALS29826 8 I BIT BUS INTERFACE FLIP I FLOPS WITH 3 I STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION

MISSING ILLUSTRATION

NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z₀ = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.

Figure 1. Load Circuit and Voltage Waveforms



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