# Signetics

# 54LS197
## Counter

**Presettable 4-Bit Binary Ripple Counter**

***Product Specification***

**Military Logic Products**

## FEATURES

- **High speed 4-bit binary counting**
- **Asynchronous parallel load for presetting counter**
- **Overriding Master Reset**
- **Buffered $Q_0$ output drives $\overline{CP}_1$ input plus standard fan-out**

## DESCRIPTION

The 54LS197 is an asynchronously presettable binary ripple counter partitioned into divide-by-2 and divide-by-8 sections with each section having a separate Clock input. Stage changes are initiated in the counting modes by the High-to-Low transition of the Clock inputs, however, state changes of the Q outputs do not occur simultaneously because of the internal ripple delays. Designers should keep in mind when using external logic to decode the Q outputs, that the unequal delays can lead to decoding spikes, and thus a decoded signal should not be used as a strobe or clock.

The $Q_0$ flip-flop is triggered by the $\overline{CP}_0$ input while the $\overline{CP}_1$ input triggers the divide-by-8 section.

The device has an asynchronous active-Low Master Reset ($\overline{MR}$) input which overrides all other inputs and forces all outputs Low. The counter is also asynchronously presettable. A Low on the Parallel Load ($\overline{PL}$) input overrides the Clock inputs and loads the data from parallel Data ($D_0$ - $D_3$) inputs into the flip-flops. The counter acts as a transparent latch while the $\overline{PL}$ is Low and any change in the $D_n$ inputs will be reflected in the outputs.

## ORDERING INFORMATION

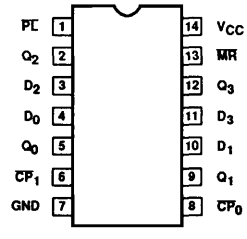
| DESCRIPTION | ORDER CODE |
|---|---|
| 14-Pin Ceramic DIP | 54LS197/BCA |
| 14-Pin Ceramic FlatPack | 54LS197/BDA |
| 20-Pin Ceramic LLCC | 54LS197/B2A |

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 54LS |
|---|---|---|
| $\overline{CP}_0$ | Clock input | 6LSUL |
| $\overline{CP}_1$ | Clock input | 3.5LSUL |
| All | Other inputs | 1LSUL |
| $Q_0$ - $Q_3$ | Outputs | 10LSUL |

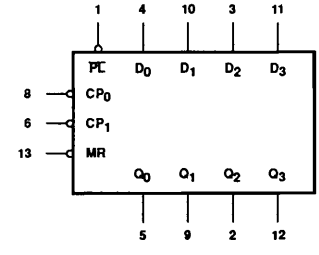
**NOTE:** Where a 54LS Unit Load (LSUL) is 20μA $I_{IH}$ and -0.4mA $I_{IL}$.

## PIN CONFIGURATION




For LLCC pin assignments, see JEDEC Standard No. 2

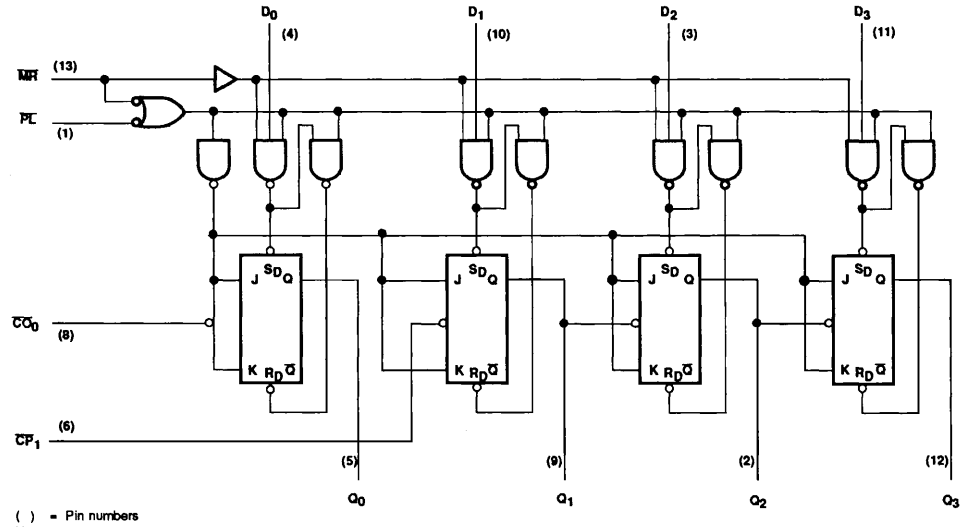
## LOGIC SYMBOL




VCC = Pin 14
GND = Pin 7

For LLCC pin assignments, see JEDEC Standard No. 2

## LOGIC DIAGRAM




For LLCC Pin Assignments, see JEDEC Standard No. 2

## COUNT SEQUENCE

| COUNT | 4-BIT BINARY[1] | | | |
|---|---|---|---|---|
| | $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |
| 10 | H | L | H | L |
| 11 | H | L | H | H |
| 12 | H | H | L | L |
| 13 | H | H | L | H |
| 14 | H | H | H | L |
| 15 | H | H | H | H |

**NOTE:** $Q_0$ connected to input $\overline{CP}_1$; input applied to $\overline{CP}_0$

## MODE SELECT — FUNCTION TABLE

| OPERATING MODE | INPUTS | | | | OUTPUT |
|---|---|---|---|---|---|
| | $\overline{MR}$ | $\overline{PL}$ | $\overline{CP}$ | $D_n$ | $Q_n$ |
| Reset (clear) | L | X | X | X | L |
| Parallel load | H | L | X | L | L |
| | H | L | X | H | H |
| Count | H | H | ↓ | X | count |

H = High voltage level
L = Low voltage level
X = Don't care
↓ = High-to-Low clock transition

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | V |
| $V_I$ | Input voltage range | -0.5 to +5.5 | V |
| $I_I$ | Input current range | -30 to +1 | mA |
| $V_O$ | Voltage applied to output in High output state range | -0.5 to $V_{CC}$ | V |
| $T_{STG}$ | Storage temperature range | -65 to +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2.0 | | | V |
| $V_{IL}$ | Low-level input voltage | | | +0.7 | V |
| $I_{IK}$ | Input clamp current | | | -18 | mA |
| $I_{OH}$ | High-level output current | | | -400 | µA |
| $I_{OL}$ | Low-level output current | | | 4 | mA |
| $T_A$ | Operating free-air temperature range | -55 | | +125 | °C |

## DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL | PARAMETER | TEST CONDITIONS[1] | | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[2] | Max | |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = Min, $V_{IH}$ = Min, $V_{IL}$ = Max, $I_{OH}$ = Max | | 2.4 | 3.4 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = Min, $V_{IH}$ = Min, $V_{IL}$ = Max, $I_{OL}$ = Max | | | 0.25 | 0.4 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = Min, $I_I$ = $I_{IK}$ | | | | -1.5 | V |
| $I_{IH2}$ | Input current at maximum input voltage | $V_{CC}$ = Max, $V_I$ = 5.5V | $D_0$ - $D_3$, $\overline{PL}$ | | | 0.1 | mA |
| | | | $\overline{MR}$, $\overline{CP_0}$, $\overline{CP_1}$ | | | 0.2 | mA |
| $I_{IH1}$ | High-level input current | $V_{CC}$ = Max, $V_I$ = 2.7V | $D_0$ - $D_3$, $\overline{PL}$ | | | 20 | µA |
| | | | $\overline{MR}$, $\overline{CP_0}$, $\overline{CP_1}$ | | | 40 | µA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = Max, $V_I$ = 0.4V | $D_0$ - $D_3$, $\overline{PL}$ | | | -0.4 | mA |
| | | | $\overline{MR}$ input | | | -0.8 | mA |
| | | | $\overline{CP_0}$ input | | | -2.4 | mA |
| | | | $\overline{CP_1}$ input | | | -1.3 | mA |
| $I_{OS}$ | Short-circuit output current[3] | $V_{CC}$ = Max | | -20 | | -100 | mA |
| $I_{CC}$ | Supply current[4] (total) | $V_{CC}$ = Max | | | 16 | 27 | mA |

## AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

| SYMBOL | PARAMETER | TEST CONDITIONS | | LIMITS $C_L = 15pF$ Min | LIMITS $C_L = 15pF$ Max | UNIT |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum count frequency | Waveform 1 | $\overline{CP}_0$ | 30 | | MHz |
| | | | $\overline{CP}_1$ | 15 | | MHz |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{CP}_0$ to $Q_0$ | Waveform 1 | | | 15<br>21 | ns<br>ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{CP}_1$ to $Q_1$ | Waveform 1 | | | 19<br>35 | ns<br>ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{CP}_1$ to $Q_2$ | Waveform 1 | | | 51<br>63 | ns<br>ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{CP}_1$ to $Q_3$ | Waveform 1 | | | 78<br>95 | ns<br>ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>Data to output | Waveform 2 | | | 27<br>44 | ns<br>ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{PL}$ to output | Waveform 3 | | | 39<br>45 | ns<br>ns |
| $t_{PHL}$ | Propagation delay<br>$\overline{MR}$ to output | Waveform 4 | | | 51 | ns |

## AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

| SYMBOL | PARAMETER | TEST CONDITIONS | | LIMIT Min | LIMIT Max | UNIT |
|---|---|---|---|---|---|---|
| $t_W$ | Clock pulse width | Waveform 1 | $\overline{CP}_0$ | 20 | | ns |
| | | | $\overline{CP}_1$ | 30 | | ns |
| $t_W$ | $\overline{MR}$ pulse width | Waveform 4 | | 15 | | ns |
| $t_W$ | $\overline{PL}$ pulse width | Waveform 3 | | 20 | | ns |
| $t_s(H)$ | Setup time High data to $\overline{PL}$ | Waveform 5 | | 10 | | ns |
| $t_h(H)$ | Hold time High data to $\overline{PL}$ | Waveform 5 | | 20 | | ns |
| $t_s(L)$ | Setup time Low data to $\overline{PL}$ | Waveform 5 | | 15 | | ns |
| $t_h(L)$ | Hold time Low data to $\overline{PL}$ | Waveform 5 | | 20 | | ns |
| $t_{rec}$ | Recovery time, $\overline{MR}$ to $\overline{CP}$ | Waveform 4 | | 30 | | ns |
| $t_{rec}$ | Recovery time, $\overline{PL}$ to $\overline{CP}$ | Waveform 3 | | 30 | | ns |

## AC ELECTRICAL CHARACTERISTICS $T_A$ = 25°C, $V_{CC}$ = 5.0V[5]

| SYMBOL | PARAMETER | TEST CONDITIONS | | LIMITS $C_L$ = 50pF Min | LIMITS $C_L$ = 50pF Max | UNIT |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum count frequency | Waveform 1 | $\overline{CP}_0$ | 30 | | MHz |
| | | | $\overline{CP}_1$ | 15 | | MHz |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{CP}_0$ to $Q_0$ | Waveform 1 | | | 20<br>26 | ns<br>ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{CP}_1$ to $Q_1$ | Waveform 1 | | | 24<br>40 | ns<br>ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{CP}_1$ to $Q_2$ | Waveform 1 | | | 56<br>68 | ns<br>ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{CP}_1$ to $Q_3$ | Waveform 1 | | | 83<br>100 | ns<br>ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>Data to output | Waveform 2 | | | 32<br>49 | ns<br>ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{PL}$ to output | Waveform 3 | | | 44<br>50 | ns<br>ns |
| $t_{PHL}$ | Propagation delay<br>$\overline{MR}$ to output | Waveform 4 | | | 56 | ns |

## AC ELECTRICAL CHARACTERISTICS $T_A$ = -55°C and +125°C, $V_{CC}$ = 5.0V[5]

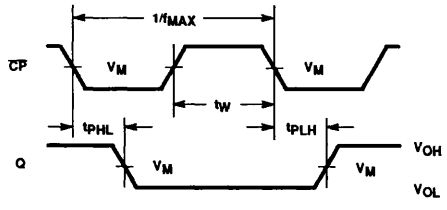
| SYMBOL | PARAMETER | TEST CONDITIONS | | LIMITS $C_L$ = 50pF Min | LIMITS $C_L$ = 50pF Max | UNIT |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum count frequency | Waveform 1 | $\overline{CP}_0$ | 30 | | MHz |
| | | | $\overline{CP}_1$ | 15 | | MHz |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{CP}_0$ to $Q_0$ | Waveform 1 | | | 26<br>34 | ns<br>ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{CP}_1$ to $Q_1$ | Waveform 1 | | | 31<br>52 | ns<br>ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{CP}_1$ to $Q_2$ | Waveform 1 | | | 73<br>88 | ns<br>ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{CP}_1$ to $Q_3$ | Waveform 1 | | | 108<br>130 | ns<br>ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>Data to output | Waveform 2 | | | 42<br>64 | ns<br>ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{PL}$ to output | Waveform 3 | | | 57<br>65 | ns<br>ns |
| $t_{PHL}$ | Propagation delay<br>$\overline{MR}$ to output | Waveform 4 | | | 73 | ns |

## AC SETUP REQUIREMENTS $T_A$ = -55°C and +125°C, $V_{CC}$ = 5.0V[5]

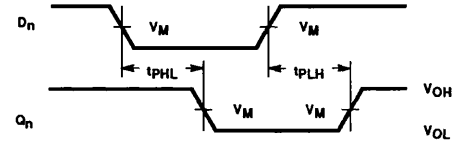
| SYMBOL | PARAMETER | TEST CONDITIONS | | LIMIT | | UNIT |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| $t_W$ | Clock pulse width | Waveform 1 | $\overline{CP}_0$ | 20 | | ns |
| | | | $\overline{CP}_1$ | 30 | | ns |
| $t_W$ | $\overline{MR}$ pulse width | Waveform 4 | | 20 | | ns |
| $t_W$ | $\overline{PL}$ pulse width | Waveform 3 | | 20 | | ns |
| $t_s$(H) | Setup time High data to $\overline{PL}$ | Waveform 5 | | 10 | | ns |
| $t_h$(H) | Hold time High data to $\overline{PL}$ | Waveform 5 | | 20 | | ns |
| $t_s$(L) | Setup time Low data to $\overline{PL}$ | Waveform 5 | | 15 | | ns |
| $t_h$(L)) | Hold time Low data to $\overline{PL}$ | Waveform 5 | | 20 | | ns |
| $t_{rec}$ | Recovery time, $\overline{MR}$ to $\overline{CP}$ | Waveform 4 | | 30 | | ns |
| $t_{rec}$ | Recovery time, $\overline{PL}$ to $\overline{CP}$ | Waveform 3 | | 30 | | ns |

**NOTES:**
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure $I_{CC}$ with all inputs grounded and all outputs open.
5. These parameters are guaranteed, but not tested.

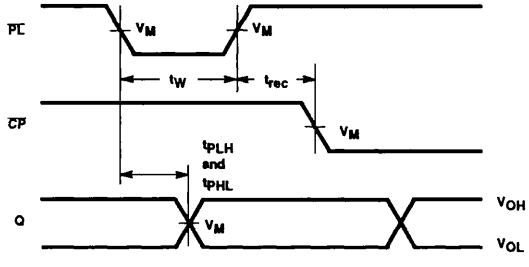
## AC WAVEFORMS



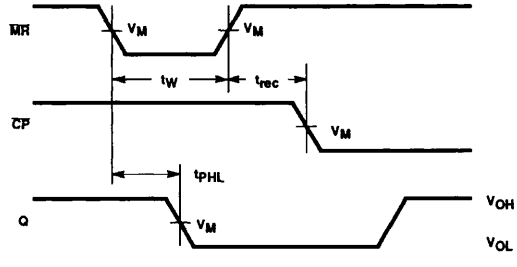

**Waveform 1. Clock to Output Delays and Clock Pulse Width**




**Waveform 2. Parallel Data to Output Delays**

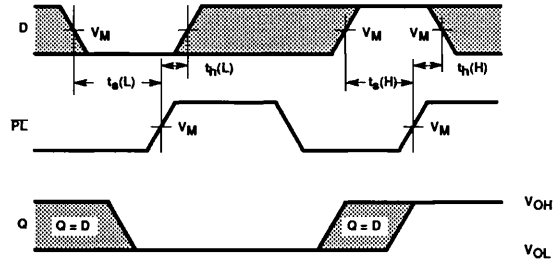



**Waveform 3. Parallel Load Pulse Width, Parallel Load to Output Delay and Parallel Load to Clock Recovery Time**




**Waveform 4. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time**

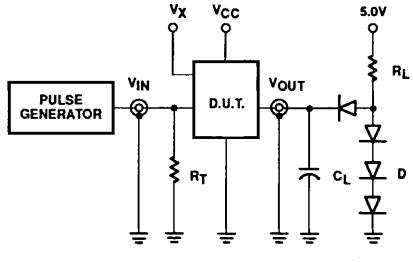
## AC WAVEFORMS (Continued)



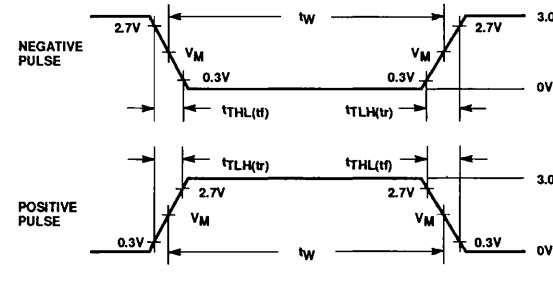

**Waveform 5. Data Setup and Hold Times**

**NOTE:** For all waveforms, $V_M$ = 1.3V for 54LS
The shaded areas indicate when the input is permitted to change for predictable output performance.

## TEST CIRCUIT AND WAVEFORM




**Test Circuit for 54 Totem-Pole Outputs**




**Input Pulse Definition**

| FAMILY | INPUT PULSE CHARACTERISTICS | | | | | |
|---|---|---|---|---|---|---|
| | $R_L$ | $V_M$ | Rep. Rate | $T_W$ | $T_{TLH}$ | $T_{THL}$ |
| 54LSXXX | 2.0kΩ | 1.3V | 1MHz | 500ns | ≤15ns | ≤6ns |

**DEFINITIONS:**
$C_L$ = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
$R_T$ = Termination resistance should be equal to $Z_{OUT}$ of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
$V_X$ = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.