# FT6175

## High Speed 8K x 8 Cache Tag Static Ram

## FEATURES

- **High Speed Address-To-Match - 8 ns Maximum Access Time**
- **High-Speed Read-Access Time**
  - **– 8/10/12/15/20/25 ns (Commercial)**
  - **– 15/20/25 ns (Military)**
- **Open Drain MATCH Output**
- **Reset Function**
- **8-Bit Tag Comparison Logic**
- **Automatic Powerdown During Long Cycles**
- **Data Retention at 2V for Battery Backup Operation**
- **Advanced CMOS Technology**
- **Low Power Operation**
- **Package Styles Available**
  - **— 28 Pin 300 mil DIP**
  - **— 28 Pin 300 mil Plastic SOJ**
- **Single Power Supply**
  - **— 5V±10%**

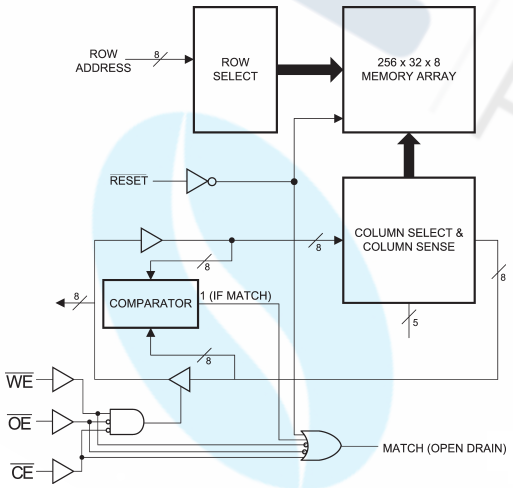
## DESCRIPTION

The FT6175 is a 65,536 bit high speed cache tag static RAM organised as 8K x 8. The CMOS memory has equal access and cycle times. Inputs are fully TTL-compatible. The cache tag RAMs operate from a single 5V±10% power supply. An 8-bit data comparator with a MATCH output is included for use as an address tag comparator in high speed cache applications. The reset function provides the capability to reset all memory locations to a LOW level.

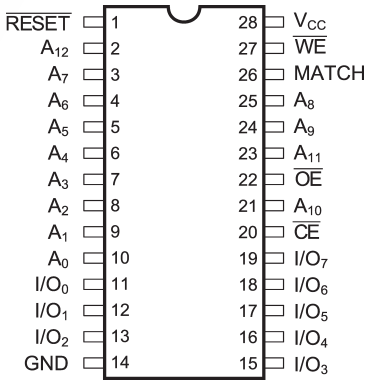
The MATCH output of the FT6175 reflects the comparison result between the 8-bit data on the I/O pins and the addressed memory location. 8K Cache lines can be mapped into 1M-Byte address spaces by comparing 20 address bits organised as 13-line address bits and 7-page address bits.

Low power operation of the FT6175 is enhanced by automatic powerdown when the memory is deselected or during long cycle times. Also, data retention is maintained down to $V_{cc}$ = 2.0. Typical battery backup applications consume only 30 µW at $V_{cc}$ = 3.0V.

## FUNCTIONAL BLOCK DIAGRAM




## PIN CONFIGURATION




DIP (C5, P5), SOJ (J5)

## MAXIMUM RATINGS[1]

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Power Supply Pin with Respect to GND | –0.5 to +7 | V |
| $V_{TERM}$ | Terminal Voltage with Respect to GND (up to 7.0V) | –0.5 to $V_{CC}$ +0.5 | V |
| $T_A$ | Operating Temperature | –55 to +125 | °C |

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $T_{BIAS}$ | Temperature Under Bias | –55 to +125 | °C |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |
| $P_T$ | Power Dissipation | 1.0 | W |
| $I_{OUT}$ | DC Output Current | 50 | mA |

## RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

| Grade(2) | Ambient Temperature | GND | $V_{cc}$ |
|---|---|---|---|
| Commercial | 0°C to +70°C | 0V | 5.0V ± 10% |
| Commercial | 0°C to +70°C | 0V | 5.0V ± 10% |

## CAPACITANCES[4]

$V_{CC}$ = 5.0V, $T_A$ = 25°C, f = 1.0MHz

| Symbol | Parameter | Conditions | Typ. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 7 | pF |

## DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage[2]

| Symbol | Parameter | Test Conditions | | FT6175 Min | FT6175 Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | | 2.2 | $V_{CC}$ +0.5 | V |
| $V_{IL}$ | Input Low Voltage | | | –0.5[3] | 0.8 | V |
| $V_{HC}$ | CMOS Input High Voltage | | | $V_{CC}$ –0.2 | $V_{CC}$ +0.5 | V |
| $V_{LC}$ | CMOS Input Low Voltage | | | –0.5[3] | 0.2 | V |
| $V_{CD}$ | Input Clamp Diode Voltage | $V_{CC}$ = Min., $I_{IN}$ = 18 mA | | | –1.2 | V |
| $V_{OL}$ | Output Low Voltage (TTL Load) | $I_{OL}$ = +8 mA, $V_{CC}$ = Min. | | | 0.4 | V |
| $V_{OH}$ | Output High Voltage (TTL Load) | $I_{OH}$ = –4 mA, $V_{CC}$ = Min. | | 2.4 | | V |
| $I_{LI}$ | Input Leakage Current | $V_{CC}$ = Max.<br>$V_{IN}$ = GND to $V_{CC}$ | Com'l.<br>Mil. | –5<br>-10 | +5<br>+10 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{CC}$ = Max., $\overline{CE}$ = $V_{IH}$,<br>$V_{OUT}$ = GND to $V_{CC}$ | Com'l.<br>Mil. | –5<br>-10 | +5<br>+10 | µA |
| $I_{SB}$ | Standby Power Supply Current (TTL Input Levels) | $\overline{CE} \geq V_{IH}$<br>$V_{CC}$ = Max .,<br>f = Max., Outputs Open | Com'l.<br>Mil. | ——<br>—— | 25<br>40 | mA |
| $I_{SB1}$ | Standby Power Supply Current (CMOS Input Levels) | $\overline{CE} \geq V_{HC}$<br>$V_{CC}$ = Max.,<br>f = 0, Outputs Open<br>$V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$ | Com'l.<br>Mil. | ——<br>—— | 5<br>25 | mA |

n/a = Not Applicable

**Notes:**

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. Transient inputs with $V_{IL}$ and $I_{IL}$ not more negative than –3.0V and –100mA, respectively, are permissible for pulse widths up to 20 ns.
4. This parameter is sampled and not 100% tested.

## DATA RETENTION CHARACTERISTICS (FT6175 Military Temperature Only)

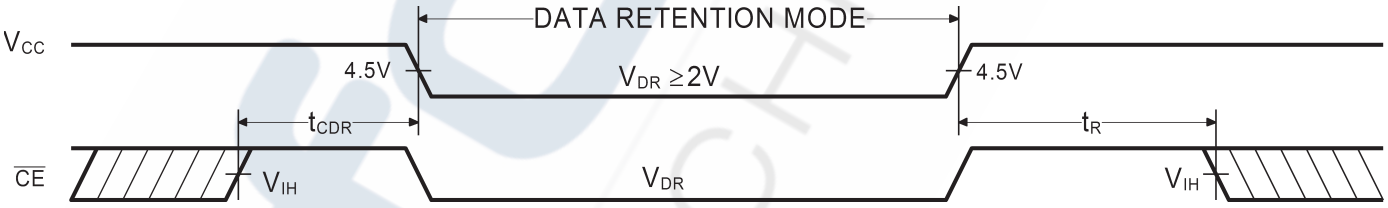
| Symbol | Parameter | Test Conditons | Min | Typ.* $V_{cc}$ = 2.0V | Typ.* $V_{cc}$ = 3.0V | Max $V_{cc}$ = 2.0V | Max $V_{cc}$ = 3.0V | Unit |
|---|---|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for Data Retention | | 2.0 | | | | | V |
| $I_{CCDR}$ | Data Retention Current | $\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ | | 10 | 15 | 600 | 900 | µA |
| $t_{CDR}$ | Chip Deselect to Data Retention Time | | 0 | | | | | ns |
| $t_R$† | Operation Recovery Time | | $t_{RC}$§ | | | | | ns |

*$T_A$ = +25ºC

§$t_{RC}$ = Read Cycle Time

† This parameter is guaranteed but not tested.

## DATA RETENTION WAVEFORM




## POWER DISSIPATION CHARACTERISTICS VS. SPEED

| Symbol | Parameter | Temperature Range | –8 | –10 | –12 | –15 | –20 | –25 | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Dynamic Operating Current* | Commercial | 200 | 180 | 170 | | 155 | 150 | mA |
| | | Military | | | | 170 | 160 | 155 | mA |

*$V_{CC}$ = 5.5V. Tested with outputs open. f = Max. Switching inputs are 0V and 3V. $\overline{CE}$ = $V_{IL}$, $\overline{OE}$ = $V_{IH}$.

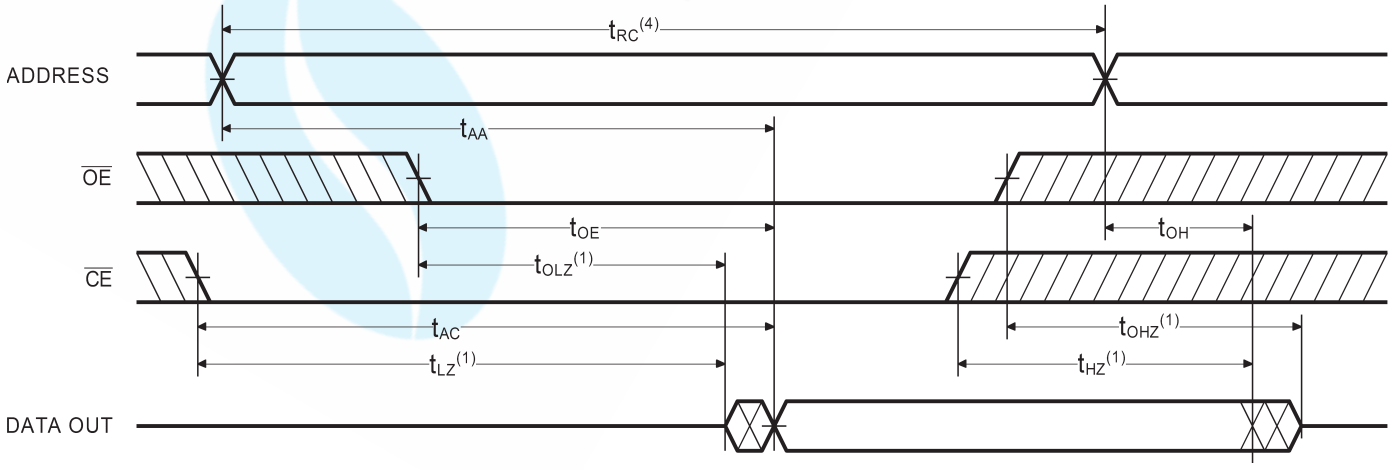
## AC CHARACTERISTICS—READ CYCLE

($V_{CC}$ = 5V ± 10%, All Temperature Ranges)[2]

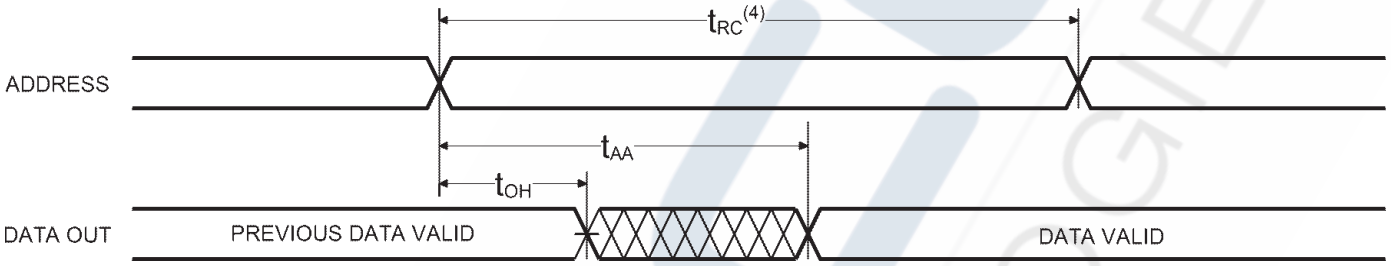
| Symbol | Parameter | –8 | | –10 | | –12 | | –15 | | –20 | | –25 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{RC}$ | Read Cycle Time | 8 | | 10 | | 12 | | 15 | | 20 | | 25 | | ns |
| $t_{AA}$ | Address Access Time | | 8 | | 10 | | 12 | | 15 | | 20 | | 25 | ns |
| $t_{OH}$ | Address Change to Output Change | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | ns |
| $t_{AC}$ | Chip Enable LOW to Output Valid | | 8 | | 10 | | 12 | | 15 | | 20 | | 25 | ns |
| $t_{LZ}$ | Chip Enable LOW to Output LOW-Z [1] | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | ns |
| $t_{HZ}$ | Chip Enable HIGH to Output HIGH -Z [1] | | 5 | | 5 | | 5 | | 8 | | 8 | | 10 | ns |
| $t_{OE}$ | Output Enable LOW to Output Valid | | 5 | | 6 | | 6 | | 8 | | 10 | | 12 | ns |
| $t_{OLZ}$ | Output Enable LOW to Output LOW-Z [1] | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{OHZ}$ | Output Enable HIGH to Output HIGH -Z [1] | | 5 | | 5 | | 5 | | 5 | | 8 | | 10 | ns |
| $t_{PU}$ | Chip Enable LOW or Address Change to Powerup | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{pUPD}$ | Powerup to Powerdown | | 20 | | 20 | | 20 | | 20 | | 20 | | 25 | ns |

Note:
1. Transition is measured ± 200 mV from steady state voltage with Output Load B.

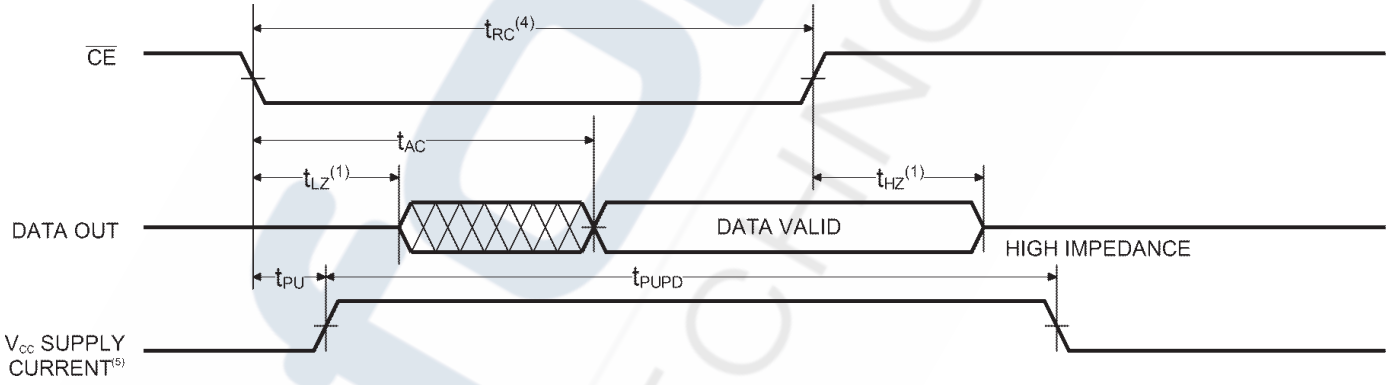
## READ CYCLE NO. 1 ($\overline{OE}$ CONTROLLED)[2, 3]



## READ CYCLE NO. 2 (ADDRESS CONTROLLED)[2]




## READ CYCLE NO. 3 ($\overline{CE}$ CONTROLLED)[2, 3]




Notes:

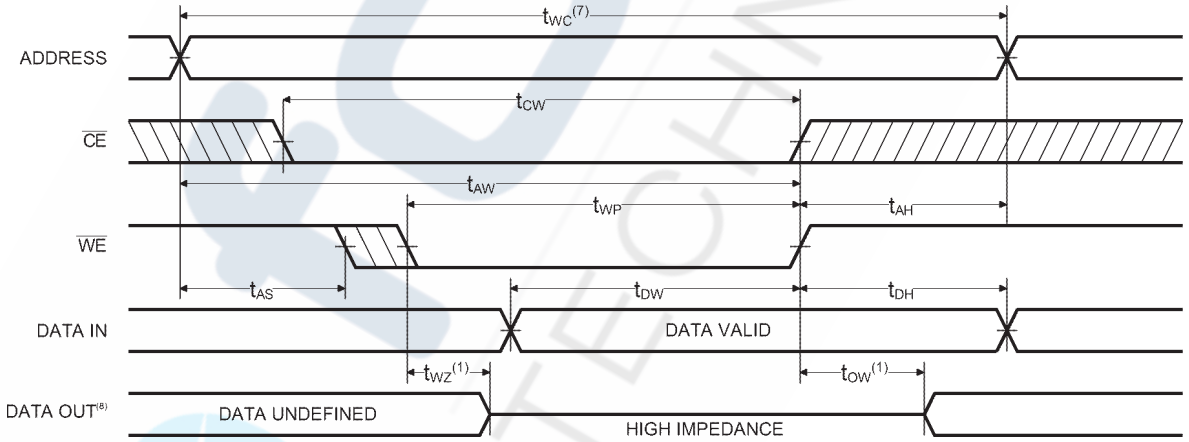
1. Transition is measured ±200 mV from steady state voltage with Output Load B. This parameter is sampled, not 100% tested.
2. $\overline{CE}$ is LOW, $\overline{OE}$ is LOW, $\overline{WE}$ is HIGH for READ cycle. $\overline{CE}$ or $\overline{WE}$ must be HIGH during address transitions.
3. All address lines are valid no later than the transition of $\overline{CE}$ to LOW.
4. READ cycle time is measured from the last valid address to the first transitioning address.
5. Powerup occurs as a result of any of the following conditions:
   a) Falling edge of $\overline{CE}$.
   b) Falling edge of $\overline{WE}$ ($\overline{CE}$ active).
   c) Any address line transition ($\overline{CE}$ active).
   d) Any Data line transition ($\overline{CE}$ and $\overline{WE}$ active).
   This device automatically powers down after $T_{PUPD}$ has elapsed from any of the prior conditions. Power dissipation is therefore a function of cycle rate, not $\overline{CE}$ pulse width.
6. $\overline{CE}$ is LOW, $\overline{WE}$ is LOW for WRITE cycle. $\overline{CE}$ or $\overline{WE}$ must be HIGH during address transitions.
7. WRITE cycle time is measured from the last valid address to the first transitioning address.
8. $\overline{OE}$ is LOW for this WRITE cycle to show $T_{WZ}$ and $T_{OW}$.

## AC CHARACTERISTICS - WRITE CYCLE

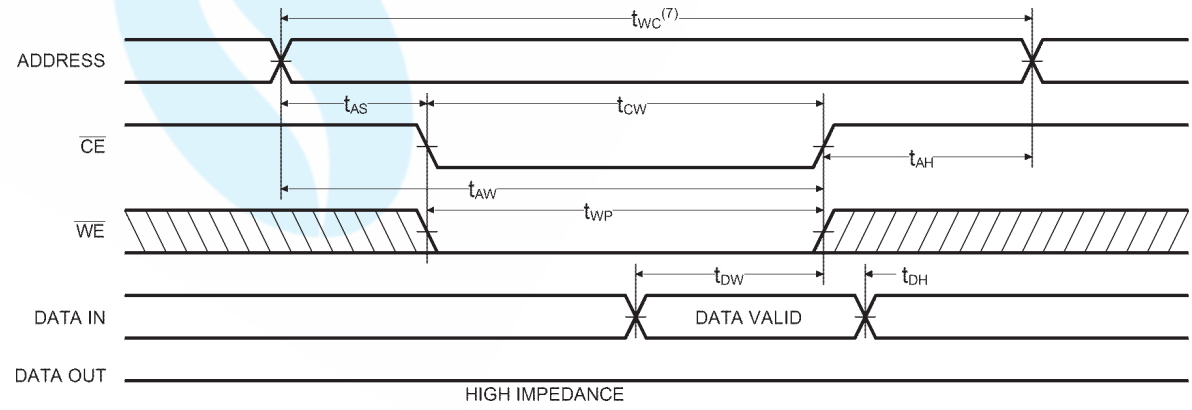
($V_{CC}$ = 5V ± 10%, 0°C to +70°C)

| Symbol | Parameter | –8 | | –10 | | –12 | | –15 | | –20 | | –25 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{WC}$ | Write Cycle Time | 8 | | 10 | | 12 | | 15 | | 20 | | 20 | | ns |
| $t_{CW}$ | Chip Enable LOW to End of Write | 7 | | 9 | | 10 | | 12 | | 15 | | 15 | | ns |
| $t_{AS}$ | Address Valid to Beginning of Write | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{AW}$ | Address Valid to End of Write | 7 | | 9 | | 10 | | 12 | | 15 | | 15 | | ns |
| $t_{AH}$ | End of Write to Address Change | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{WP}$ | Write Pulse Width | 7 | | 9 | | 10 | | 12 | | 15 | | 15 | | ns |
| $t_{DW}$ | Data Valid to End of Write | 6 | | 6 | | 6 | | 7 | | 10 | | 10 | | ns |
| $t_{DH}$ | End of Write to Data Change | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{OW}$ | Write Enable HIGH to Output LOW-Z (1) | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{WZ}$ | Write Enable LOW to Output HIGH-Z (1) | | 4 | | 4 | | 4 | | 5 | | 7 | | 7 | ns |

## WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(6)




## WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED)(6)

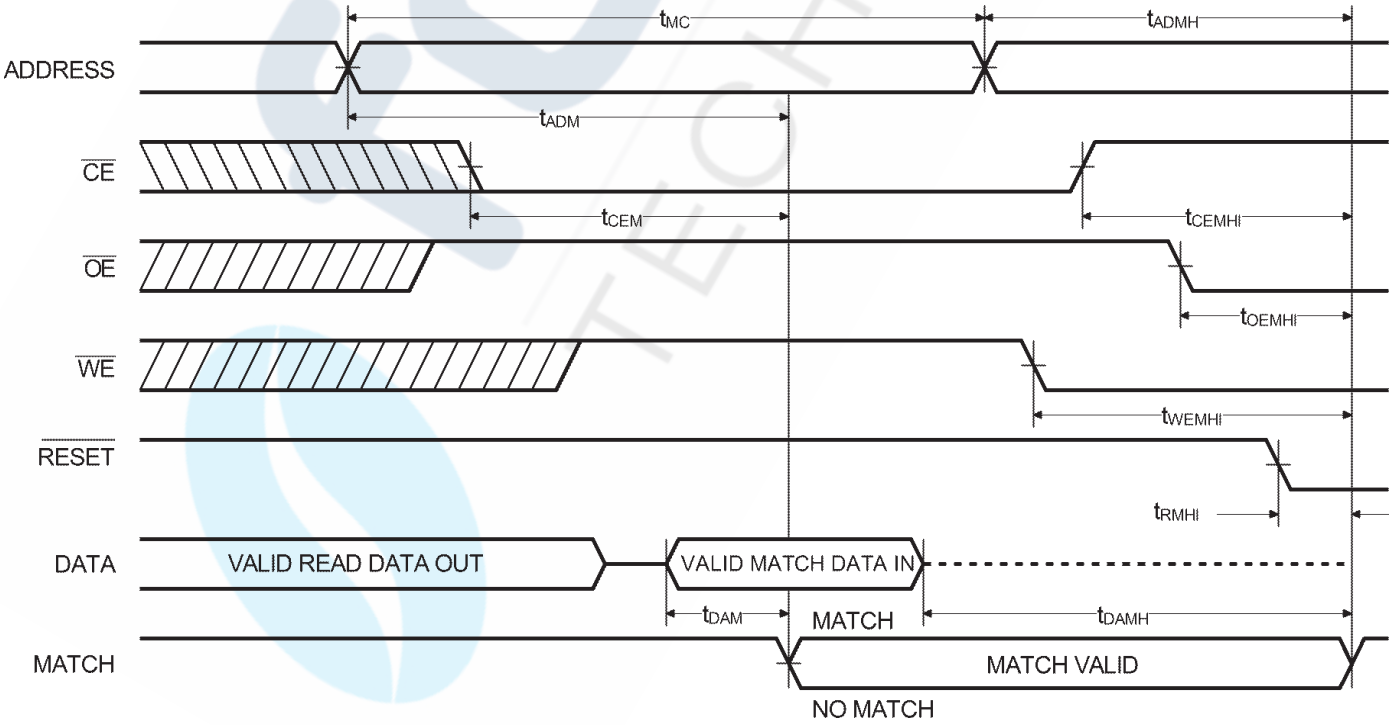


## AC CHARACTERISTICS - MATCH CYCLE

($V_{CC}$ = 5.0V ± 10%, 0°C to +70°C)

| Symbol | Parameter | –8 | | –10 | | –12 | | –15 | | –20 | | –25 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{MC}$ | Match Cycle Time | 8 | | 10 | | 12 | | 15 | | 20 | | 25 | | ns |
| $t_{ADM}$ | Address Valid to MATCH Valid | | 8 | | 10 | | 12 | | 15 | | 20 | | 25 | ns |
| $t_{ADMH}$ | Address Change to MATCH Change | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | ns |
| $t_{CEM}$ | Chip Enable LOW to MATCH Valid | | 7 | | 8 | | 8 | | 10 | | 10 | | 15 | ns |
| $t_{CEMHI}$ | Chip Enable HIGH to MATCH HIGH | | 7 | | 8 | | 8 | | 10 | | 10 | | 15 | ns |
| $t_{OEMHI}$ | Output Enable LOW to MATCH HIGH | | 7 | | 9 | | 10 | | 12 | | 15 | | 20 | ns |
| $t_{WEMHI}$ | Write Enable LOW to MATCH HIGH | | 7 | | 9 | | 10 | | 12 | | 15 | | 20 | ns |
| $t_{DAM}$ | Data Valid to MATCH Valid | | 7 | | 9 | | 10 | | 13 | | 15 | | 15 | ns |
| $t_{DAMH}$ | Data Change to MATCH Change | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |

## MATCH TIMING

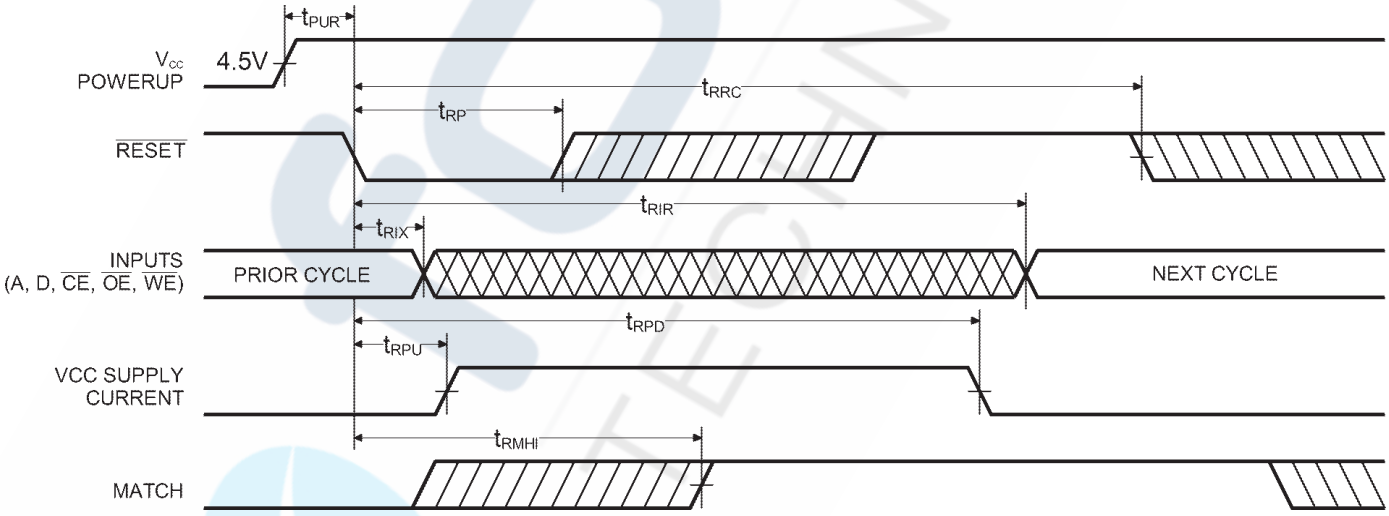


## AC CHARACTERISTICS - RESET CYCLE

($V_{CC}$ = 5.0V ± 10%, 0°C to +70°C)

| Symbol | Parameter | –8 | | –10 | | –12 | | –15 | | –20 | | –25 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{RRC}$ | Reset Cycle Time | 35 | | 40 | | 45 | | 50 | | 50 | | 60 | | ns |
| $t_{RP}$ | Reset Pulse Width | 8 | | 10 | | 12 | | 12 | | 15 | | 15 | | ns |
| $t_{RPU}$ | Reset LOW to Powerup | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{RPD}$ | Reset LOW to Powerdown | | 35 | | 40 | | 45 | | 50 | | 50 | | 60 | ns |
| $t_{RMHI}$ | Reset LOW to MATCH HIGH | 0 | 8 | 0 | 10 | 0 | 10 | 0 | 12 | 0 | 15 | 0 | 20 | ns |
| $t_{RIX}$ | Reset LOW to Inputs Ignored | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{RIR}$ | Reset LOW to inputs Recognized | | 35 | | 40 | | 45 | | 50 | | 50 | | 60 | ns |
| $t_{PUR}$ | Powerup to RESET LOW | 8 | | 10 | | 12 | | 15 | | 20 | | 25 | | ns |

## RESET TIMING

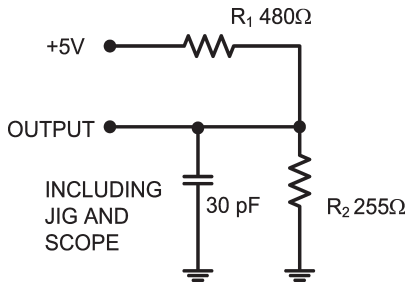



## AC TEST CONDITIONS

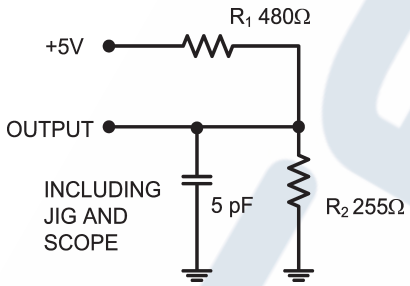
| | |
|---|---|
| Input Pulse Levels | GND to 3.0V |
| Input Rise and Fall Times | < 3ns |
| Input Timing Reference Level | 1.5V |
| Output Timing Reference Level | 1.5V |
| Output Load | Outputs Loads A, B & C |

## TRUTH TABLE

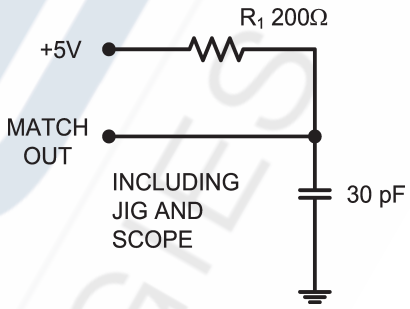
| Mode | $\overline{CE}$ | $\overline{WE}$ | Output | Power |
|---|---|---|---|---|
| Standby | H | X | High Z | Standby |
| Read | L | H | $D_{OUT}$ | Active |
| Write | L | L | High Z | Active |




**OUTPUT LOAD A**

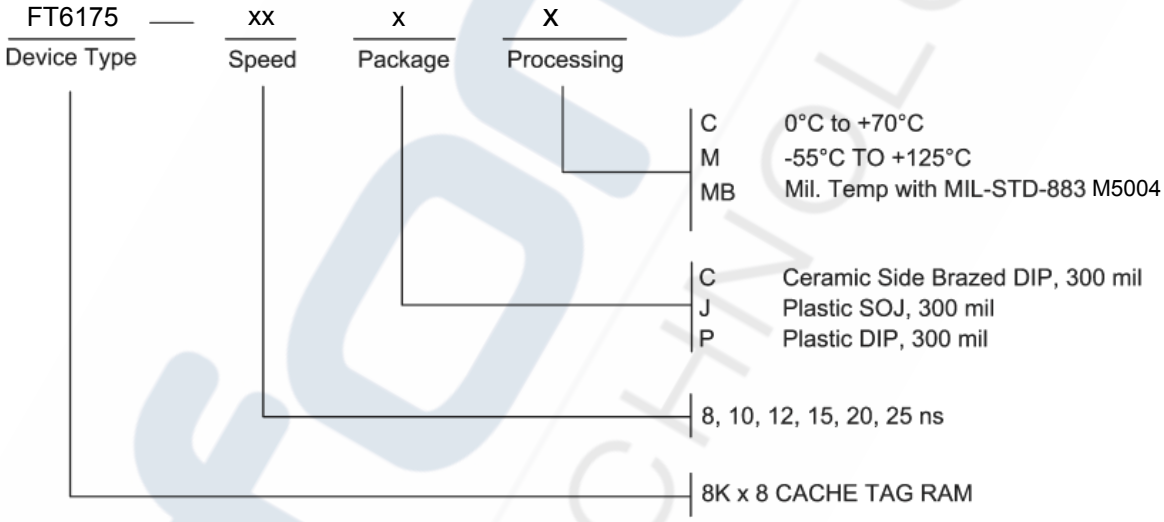



**OUTPUT LOAD B**




**OUTPUT LOAD C**

## ORDERING INFORMATION




## SELECTION GUIDE

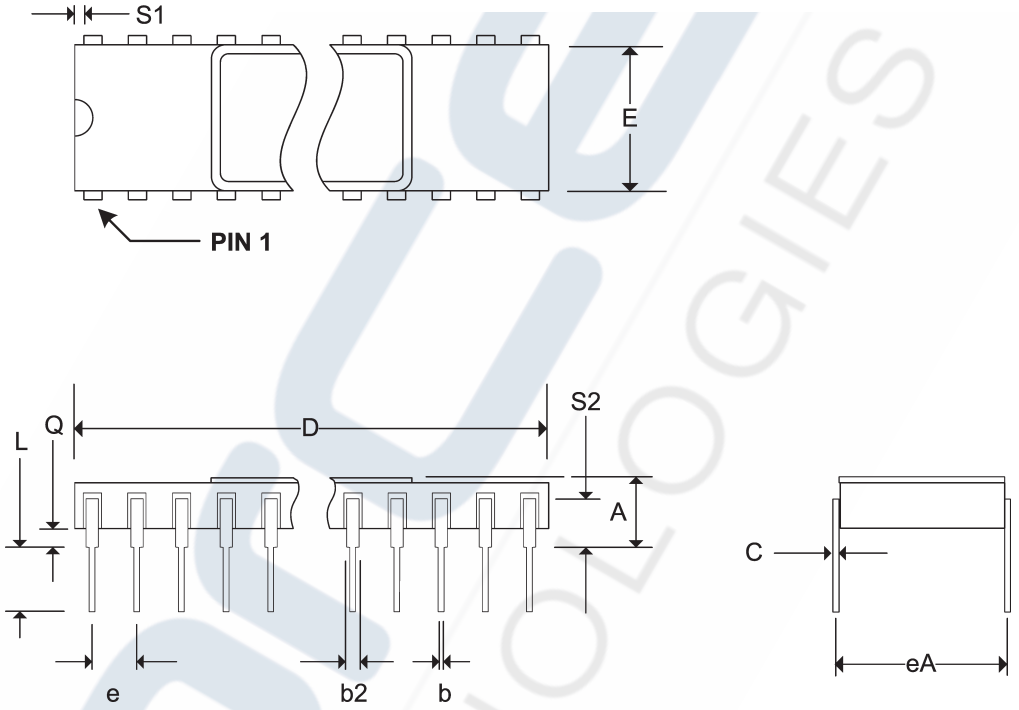
The FT6175 is available in the following temperature, speed and package options.

| Temperature Range | Package | Speed | | | | | |
|---|---|---|---|---|---|---|---|
| | | 8 | 10 | 12 | 15 | 20 | 25 |
| Commercial | Plastic DIP | -8PC | -10PC | -15PC | -15PC | -20PC | -25PC |
| | Plastic SOJ | -8JC | -10JC | -15JC | -15JC | -20JC | -25JC |
| Miliitary Temperature | Side Brazed DIP | N/A | N/A | N/A | -15CM | -20CM | -25CM |
| Military Processed* | Side Brazed DIP | N/A | N/A | N/A | -15CMB | -20CMB | -25CMB |

* Military temperature range with MIL-STD-883 M5004
N/A = Not Available

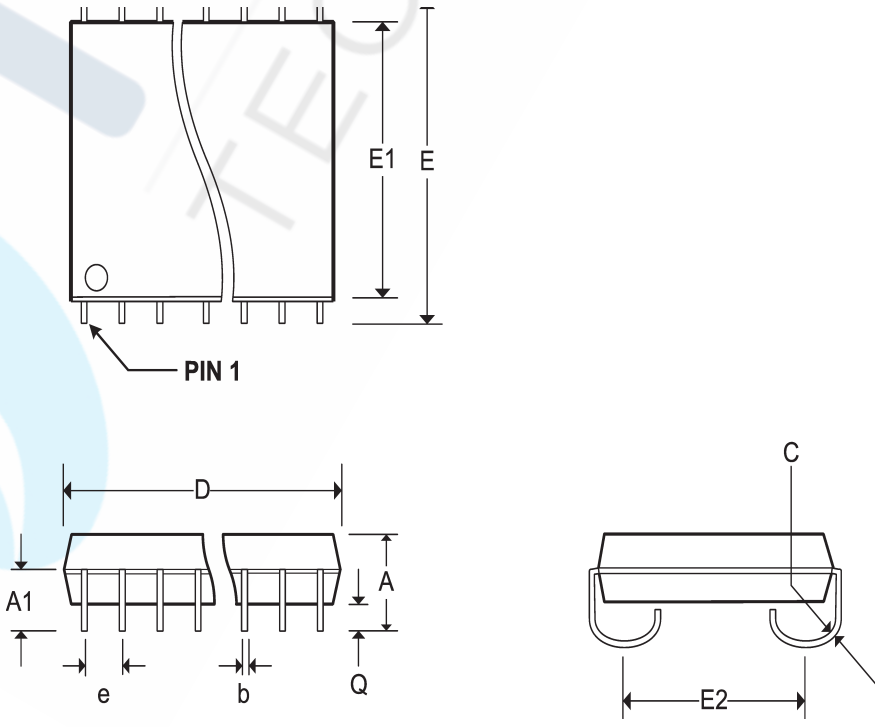
| Pkg # | C5 | |
|---|---|---|
| # Pins | 28 (300 mil) | |
| Symbol | **Min** | **Max** |
| A | - | 0.225 |
| b | 0.014 | 0.026 |
| b2 | 0.045 | 0.065 |
| C | 0.008 | 0.018 |
| D | - | 1.485 |
| E | 0.240 | 0.310 |
| eA | 0.300 BSC | |
| e | 0.100 BSC | |
| L | 0.125 | 0.200 |
| Q | 0.015 | 0.070 |
| S1 | 0.005 | - |
| S2 | 0.005 | - |

## SIDE BRAZED DUAL IN-LINE PACKAGE



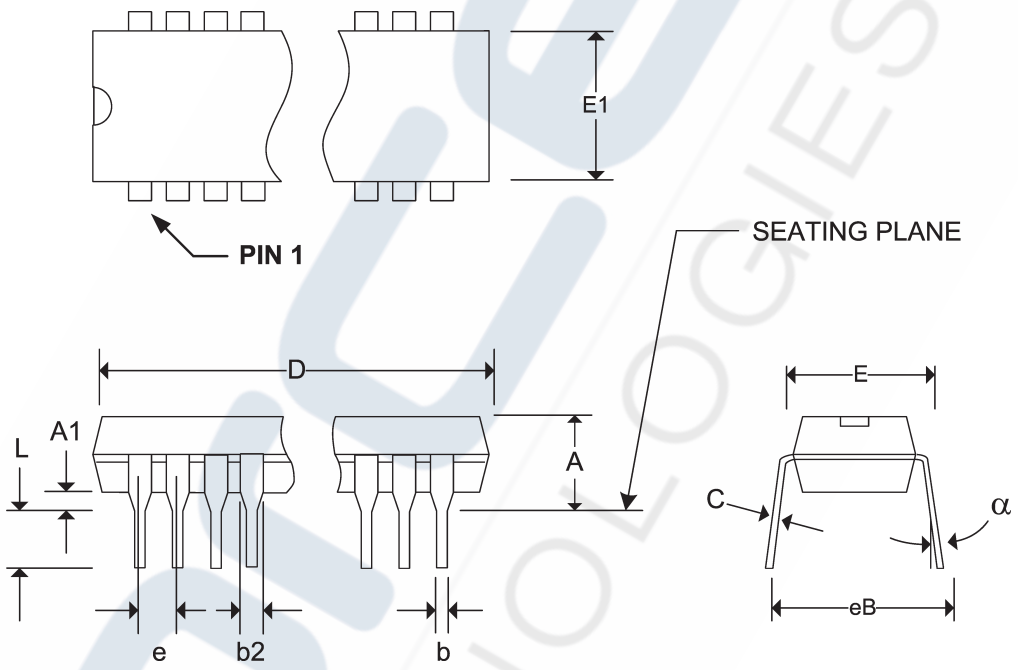

| Pkg # | J5 | |
|---|---|---|
| # Pins | 28 (300 mil) | |
| Symbol | **Min** | **Max** |
| A | 0.120 | 0.148 |
| A1 | 0.078 | - |
| b | 0.014 | 0.020 |
| C | 0.007 | 0.011 |
| D | 0.700 | 0.730 |
| e | 0.050 BSC | |
| E | 0.335 BSC | |
| E1 | 0.292 | 0.300 |
| E2 | 0.267 BSC | |
| Q | 0.025 | - |

## SOJ SMALL OUTLINE IC PACKAGE



| Pkg # | P5 | |
|---|---|---|
| # Pins | 28 (300 mil) | |
| Symbol | **Min** | **Max** |
| A | - | 0.210 |
| A1 | | - |
| b | 0.014 | 0.023 |
| b2 | 0.045 | 0.070 |
| C | 0.008 | 0.014 |
| D | 1.345 | 1.400 |
| E1 | 0.270 | 0.300 |
| E | 0.300 | 0.380 |
| e | 0.100 BSC | |
| eB | - | 0.430 |
| L | 0.115 | 0.150 |
| α | 0° | 15° |

**PLASTIC DUAL IN-LINE PACKAGE**



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## REVISIONS

**DOCUMENT NUMBER**: SRAM118
**DOCUMENT TITLE**: FT6175 HIGH SPEED 8Kx8 CACHE TAG STATIC RAM

| REV. | ISSUE DATE | ORIG. OF CHANGE | DESCRIPTION OF CHANGE |
|---|---|---|---|
| ORIG | 1997 | M.S | New Data Sheet |
| 1 | Oct-05 | M.S | Change logo to Pyramid |
| 1.1 | Nov-05 | M.S | Corrected error in Selection Guide |
| 1.2 | Aug-06 | M.S | Updated SOJ package information |
| | | | |
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