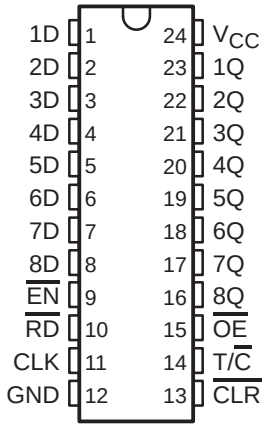
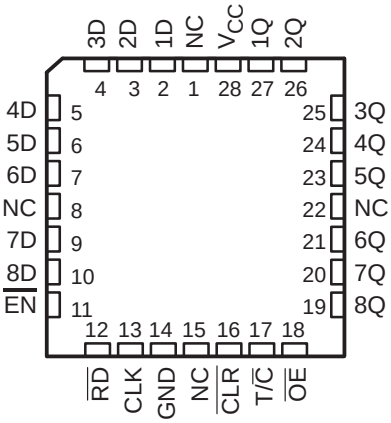
- **3-State I/O-Type Read-Back Inputs**
- **Bus-Structured Pinout**
- **T/$\overline{C}$ Determines True or Complementary Data at Q Outputs**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs**

SN54ALS996 . . . JT PACKAGE
SN74ALS996 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS996 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These 8-bit latches are designed specifically for storing the contents of the input data bus and providing the capability of reading back the stored data onto the input data bus. The Q outputs are designed with bus-driving capability.

The edge-triggered flip-flops enter the data on the low-to-high transition of the clock (CLK) input when the enable ($\overline{EN}$) input is low. Data can be read back onto the data inputs by taking the read ($\overline{RD}$) input low, in addition to having $\overline{EN}$ low. When $\overline{EN}$ is high, both the read-back and write modes are disabled. Transitions on $\overline{EN}$ should only be made with CLK high to prevent false clocking.

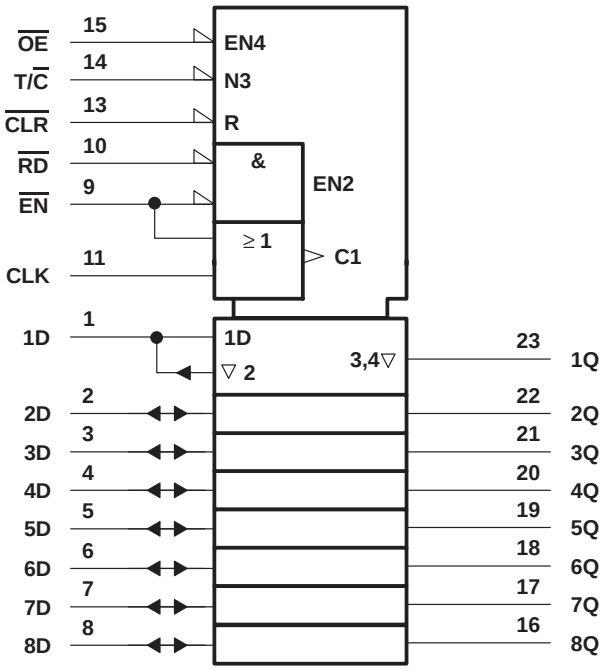
The polarity of the Q outputs can be controlled by the polarity (T/$\overline{C}$) input. When T/$\overline{C}$ is high, Q is the same as is stored in the flip-flops. When T/$\overline{C}$ is low, the output data is inverted. The Q outputs can be placed in the high-impedance state by taking the output-enable ($\overline{OE}$) input high. $\overline{OE}$ does not affect the internal operation of the register. Old data can be retained or new data can be entered while the outputs are off.

A low level at the clear ($\overline{CLR}$) input resets the internal registers low. The clear function is asynchronous and overrides all other register functions.

The -1 version of the SN74ALS996 is identical to the standard version, except that the recommended maximum I_{OL} for the -1 version is increased to 48 mA. There is no -1 version of the SN54ALS996.

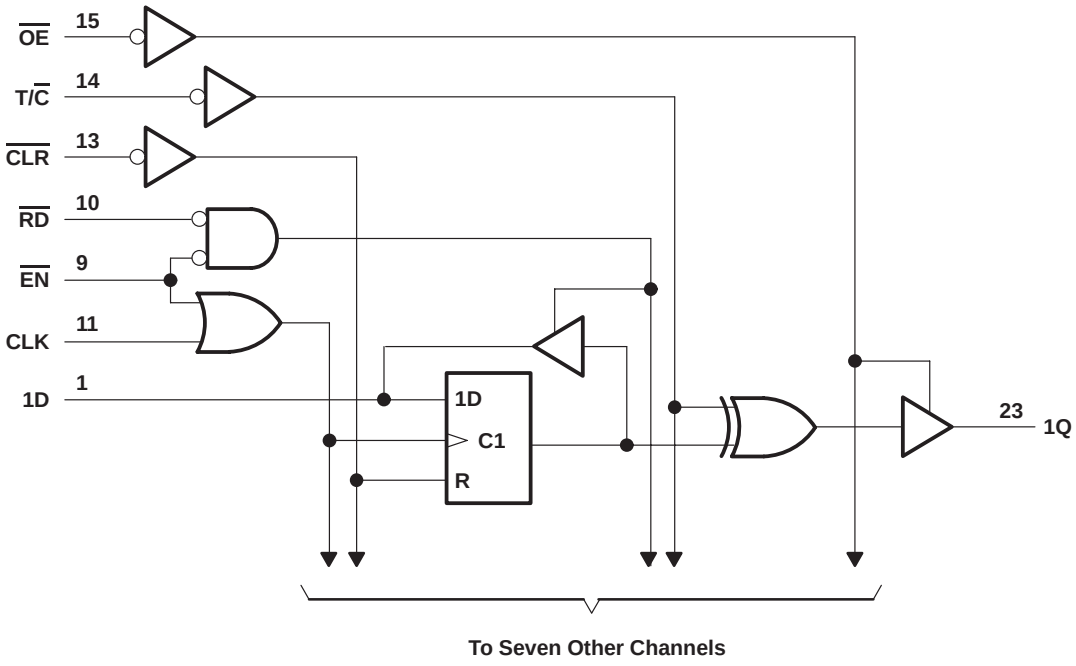
The SN54ALS996 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALS996 is characterized for operation from 0°C to 70°C.

logic symbol†



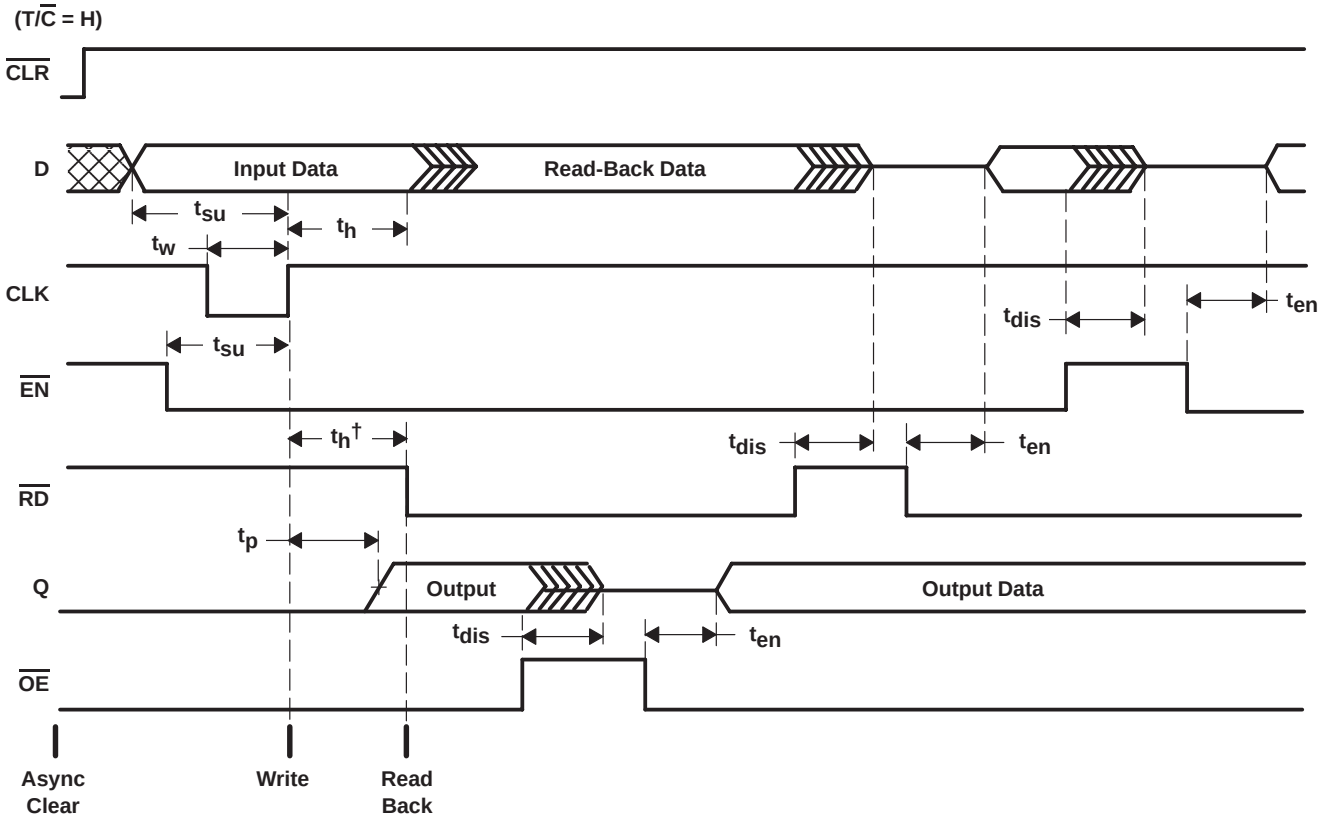
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

timing diagram



† This hold time ensures that the read-back circuit will not create a conflict on the input data bus.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I ($\overline{OE}$, $\overline{RD}$, $\overline{EN}$, CLK, $\overline{CLR}$, and T/$\overline{C}$) . . . . . 7 V
Voltage applied to D inputs and to disabled 3-state outputs . . . . . 5.5 V
Operating free-air temperature range, T_A: SN54ALS996 . . . . . –55°C to 125°C
SN74ALS996 . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54ALS996			SN74ALS996			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	All inputs				2			V
		All inputs except $\overline{OE}$, $\overline{RD}$	2						
		$\overline{OE}$, $\overline{RD}$	2.2						
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	Q			−1			−2.6	mA
		D			−0.4			−0.4	
I_{OL}	Low-level output current	Q			12			24	mA
								48†	
		D			8			8	
f_{clock}	Clock frequency		0		35	0		35	MHZ
t_w	Pulse duration	$\overline{CLR}$ low	10			10			ns
		CLK low	14.5			14.5			
		CLK high	14.5			14.5			
t_{su}	Setup time	Data before CLK↑	15			15			ns
		$\overline{EN}$ low before CLK↑	10			10			
		CLK high before $\overline{EN}$↑‡	15			15			
		$\overline{CLR}$ high (inactive) before CLK↑	10			10			
t_h	Hold time	Data after CLK↑	1			0			ns
		$\overline{EN}$ low after CLK↑	5			5			
		$\overline{RD}$ high after CLK↑§	5			5			
T_A	Operating free-air temperature		−55		125	0		70	°C

† Applies only to the -1 version and only if V_{CC} is maintained between 4.75 V and 5.25 V
‡ This setup time ensures that $\overline{EN}$ will not false clock the data register.
§ This hold time ensures that there will be no conflict on the input data bus.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS996			SN74ALS996			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = – 0.4 mA	V_{CC} –2			V_{CC} –2			V
	Q	V_{CC} = 4.5 V	I_{OH} = – 1 mA	2.4	3.2					
			I_{OH} = – 2.6 mA				2.4	3.2		
V_{OL}	D	V_{CC} = 4.5 V	I_{OL} = 4 mA		0.25	0.4				V
			I_{OL} = 8 mA					0.35	0.5	
	Q	V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
			I_{OL} = 24 mA					0.35	0.5	
			I_{OL} = 48 mA‡					0.35	0.5	
I_{OZH}	Q	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	µA
I_{OZL}	Q	V_{CC} = 5.5 V,	V_O = 0.4 V			–20			–20	µA
I_I	D inputs	V_{CC} = 5.5 V	V_I = 5.5 V			0.1			0.1	mA
	All others		V_I = 7 V			0.1			0.1	
I_{IH}	D inputs§	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
	All others					20			20	
I_{IL}	D inputs§	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.1			–0.1	mA
	All others					–0.1			–0.1	
I_O¶		V_{CC} = 5.5 V, $\overline{CLR}$ = 2.5 V	V_O = 2.25 V	–20		–112	–30		–112	mA
I_{CC}		V_{CC} = 5.5 V, $\overline{EN}$, $\overline{RD}$ low	Outputs high		35	55		35	55	mA
			Outputs low		55	85		55	85	
			Outputs disabled		42	65		42	65	

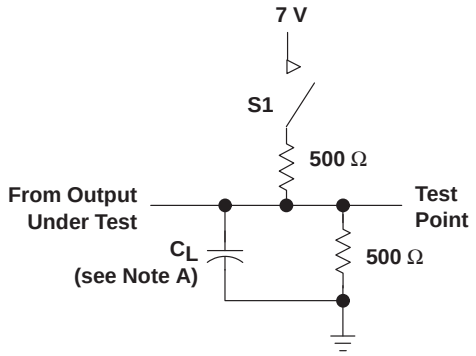
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Applies only to the -1 version and only if V_{CC} is maintained between 4.75 V and 5.25 V
§ For I/O ports (Q_A thru Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.
¶ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

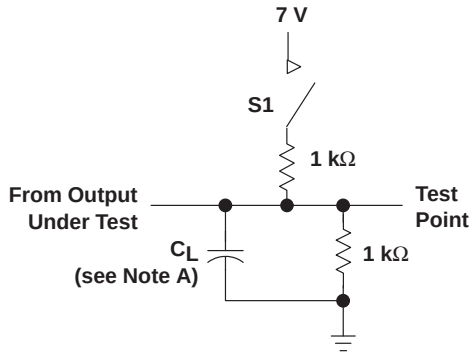
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = MIN to MAX†				UNIT
			SN54ALS996		SN74ALS996		
			MIN	MAX	MIN	MAX	
f_{max}			35		35		MHz
t_{PLH}	CLK (T/$\overline{C}$ = H or L)	Q	5	30	5	28	ns
t_{PHL}			5	24	5	28	
t_{PLH}	$\overline{CLR}$ (T/$\overline{C}$ = L)	Q	5	27	7	27	ns
t_{PHL}	$\overline{CLR}$ (T/$\overline{C}$ = H)		5	23	7	23	
t_{PLH}	T/$\overline{C}$	Q	4	23	5	23	ns
t_{PHL}			5	23	5	23	
t_{PHL}	$\overline{CLR}$	D	5	30	8	30	ns
t_{en}‡	$\overline{RD}$	D	2	18	3	16	ns
t_{dis}§			1	19	3	19	
t_{en}‡	$\overline{EN}$	D	2	17	3	16	ns
t_{dis}§			1	19	3	19	
t_{en}‡	$\overline{OE}$	Q	2	15	4	15	ns
t_{dis}§			1	11	1	10	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ $t_{en} = t_{PZH}$ or t_{PZL}
§ $t_{dis} = t_{PHZ}$ or t_{PLZ}

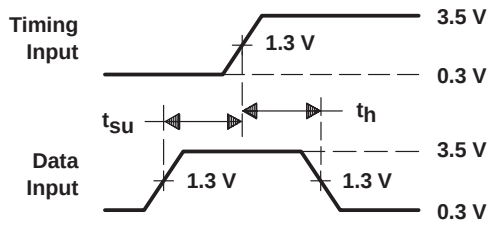
PARAMETER MEASUREMENT INFORMATION



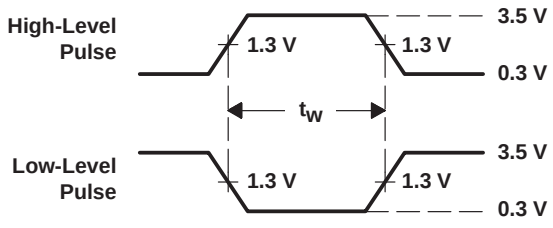
LOAD CIRCUIT FOR Q OUTPUTS



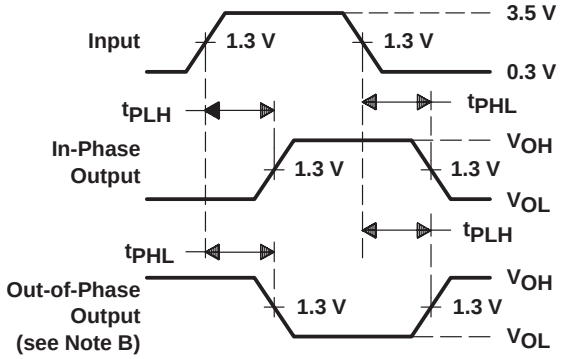
LOAD CIRCUIT FOR D OUTPUTS



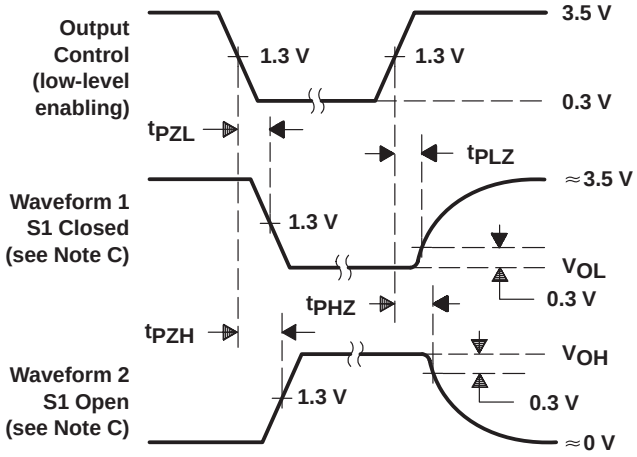
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. When measuring propagation delay times of 3-state outputs, switch S1 is open.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.

Figure 1. Load Circuits and Voltage Waveforms

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SN54ALS996, 8-Bit D-type Edge-Triggered Read-Back Latches

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54ALS996	SN74ALS996
Voltage Nodes (V)	5	5
Vcc range (V)	4.5 to 5.5	4.5 to 5.5
Input Level	TTL	TTL
Output Level	TTL	TTL
Output Drive (mA)		-2.6/24
Output	3S	
No. of Bits	8	
th (ns)		0
tpd max (ns)		28
tsu (ns)		15

FEATURES

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- 3-State I/O-Type Read-Back Inputs
- Bus-Structured Pinout
- T/C\ Determines True or Complementary Data at Q Outputs
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

DESCRIPTION

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These 8-bit latches are designed specifically for storing the contents of the input data bus and providing the capability of reading back the stored data onto the input data bus. The Q outputs are designed with bus-driving capability.

The edge-triggered flip-flops enter the data on the low-to-high transition of the clock (CLK) input when the enable ( ) input is low. Data can be read back onto the data inputs by taking the read ($\overline{RD}$) input low, in addition to having low. When EN\ is high, both the read-back and write modes are disabled. Transitions on should only be made with CLK high to prevent false clocking.

The polarity of the Q outputs can be controlled by the polarity (T/C\) input. When T/C\ is high, Q is the same as is stored in the flip-flops. When T/C\ is low, the output data is inverted. The Q outputs can be placed in the high-impedance state by taking the output-enable ($\overline{OE}$) input high. $\overline{OE}$ does not affect the internal operation of the register. Old data can be retained or new data can be entered while the outputs are off.

A low level at the clear ($\overline{CLR}$) input resets the internal registers low. The clear function is asynchronous and overrides all other register functions.

The -1 version of the SN74ALS996 is identical to the standard version, except that the recommended maximum I_{OL} for the -1 version is increased to 48 mA. There is no -1 version of the SN54ALS996.

The SN54ALS996 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS996 is characterized for operation from 0°C to 70°C.

Product Folder: SN54ALS996, 8-Bit D-type Edge-Triggered Read-Back Latches

TECHNICAL DOCUMENTS

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To view the following documents, Acrobat Reader 4.0 is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

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Full datasheet in Acrobat PDF: sn54als996.pdf (132 KB,Rev.B) (Updated: 01/01/1995)

APPLICATION NOTES

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View Application Notes for Digital Logic

- Advanced Schottky (ALS and AS) Logic Families (SDAA010 - Updated: 08/01/1995)
- Bus-Interface Devices With Output-Damping Resistors Or Reduced-Drive Outputs (Rev. A) (SCBA012A - Updated: 08/01/1997)
- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- Live Insertion (SDYA012 - Updated: 10/01/1996)
- TI IBIS File Creation, Validation, and Distribution Processes (SZZA034 - Updated: 08/29/2002)
- Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sh (Rev. A) (SZZA036A - Updated: 02/27/2003)

MORE LITERATURE

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- Enhanced Plastic Portfolio Brochure (SGZB004, 387 KB - Updated: 08/19/2002)
- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- MicroStar Junior BGA Design Summary (SCET004, 167 KB - Updated: 07/28/2000)
- Military Brief (SGYN138, 803 KB - Updated: 10/10/2000)
- Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet (Rev. A) (SDYZ001A, 138 KB - Updated: 07/01/1996)
- Palladium Lead Finish User's Manual (SDYV001, 2041 KB - Updated: 11/01/1996)
- QML Class V Space Products Military Brief (Rev. A) (SGZN001A, 257 KB - Updated: 10/07/2002)

USER GUIDES

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- LOGIC Pocket Data Book (SCYD013, 4837 KB - Updated: 12/05/2002)

PRICING/AVAILABILITY/PKG

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DEVICE INFORMATION
Updated Daily

ORDERABLE DEVICE	STATUS	PACKAGE TYPE | PINS	TEMP (°C)	DSCC NUMBER	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY
5962-89945013A	ACTIVE	LCCC (FK) | 28	-55 TO 125		View Contents	1KU | 23.94	1
5962-8994501KA	ACTIVE	CFP (W) | 24	-55 TO 125		View Contents	1KU | 8.88	1
5962-8994501LA	ACTIVE	CDIP (JT) | 24	-55 TO 125		View Contents	1KU | 16.22	1
SNJ54ALS996FK	ACTIVE	LCCC (FK) | 28	-55 TO 125	5962-89945013A	View Contents	1KU | 23.94	1

TI INVENTORY STATUS
As Of 09:00 AM GMT, 17 Apr 2003

IN STOCK	IN PROGRESS QTY | DATE	LEAD TIME
9*	3315 | 20 May	8 WKS
	>10k | 27 May	
102*	>10k | 20 May	8 WKS
370*	>10k | 20 May	8 WKS
0*	3315 | 20 May	8 WKS
	>10k | 27 May	

REPORTED DISTRIBUTOR INVENTORY
As Of 09:00 AM GMT, 17 Apr 2003

DISTRIBUTOR COMPANY | REGION	IN STOCK	PURCHASE
Avnet | Americas	74	BUY NOW
None Reported View Distributors		
None Reported View Distributors		
None Reported View Distributors		

Product Folder: SN54ALS996, 8-Bit D-type Edge-Triggered Read-Back Latches

SNJ54ALS996JT	ACTIVE	CDIP (JT)	24	-55 TO 125	5962-8994501LA	View Contents	1KU | 16.22	1	0*	>10k | 20 May	8 WKS	None Reported View Distributors		
SNJ54ALS996W	OBSOLETE	CFP (W)	24	-55 TO 125	5962-8994501KA	View Contents	1KU |		0*		Call**	None Reported View Distributors		

Table Data Updated on: 4/17/2003