OCTAL BUFFER/LINE DRIVER; 3-STATE; INVERTING

FEATURES

- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT240 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT240 are octal inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state. The "240" is identical to the "244" but has inverting outputs.

FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA_n	nY_n
L	L	H
L	H	L
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/$ t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	$C_L = 15$ pF $V_{CC} = 5$ V	9	9	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	30	pF

GND = 0 V; $T_{amb} = 25\ °C$; $t_r = t_f = 6$ ns

Notes

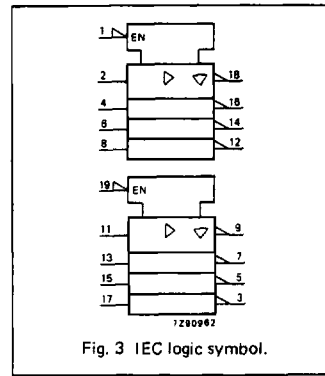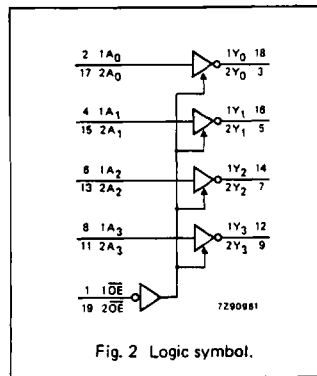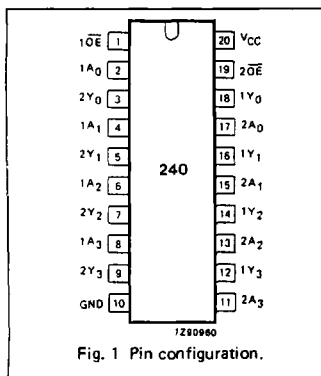1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

   f_i = input frequency in MHz C_L = output load capacitance in pF
   f_o = output frequency in MHz V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC   the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to $V_{CC} - 1.5$ V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	output enable input (active LOW)
2, 4, 6, 8	$1A_0$ to $1A_3$	data inputs
3, 5, 7, 9	$2Y_0$ to $2Y_3$	bus outputs
10	GND	ground (0 V)
17, 15, 13, 11	$2A_0$ to $2A_3$	data inputs
18, 16, 14, 12	$1Y_0$ to $1Y_3$	bus outputs
19	$2\overline{OE}$	output enable input (active LOW)
20	V_{CC}	positive supply voltage

Fig. 1 Pin configuration.

Fig. 2 Logic symbol.

Fig. 3 IEC logic symbol.

Fig. 4 Functional diagram.
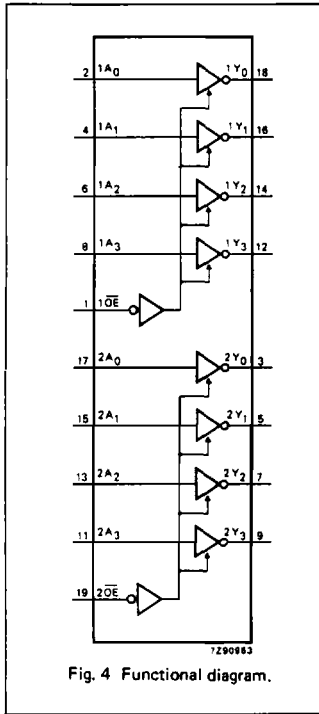
DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	V_{CC} V	WAVEFORMS
		74HC									
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay 1A_n to 1Y_n; 2A_n to 2Y_n		30 11 9	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 5
t_{PZH}/ t_{PZL}	3-state output enable time 1$\overline{OE}$ to 1Y_n; 2$\overline{OE}$ to 2Y_n		39 14 11	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{PHZ}/ t_{PLZ}	3-state output disable time 1$\overline{OE}$ to 1Y_n; 2$\overline{OE}$ to 2Y_n		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 5

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.
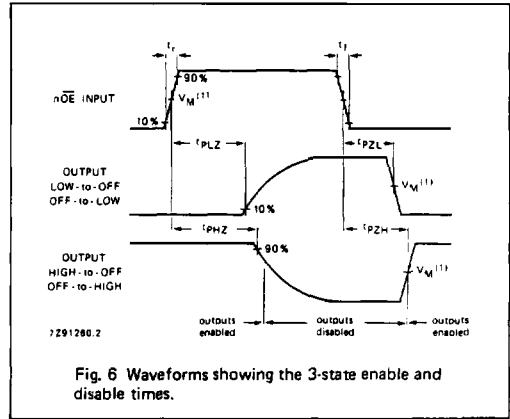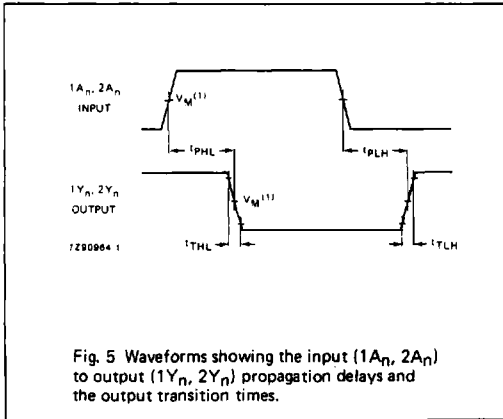
input	unit load coefficient
$1A_n$	1.50
$2A_n$	1.50
$1\overline{OE}$	0.70
$2\overline{OE}$	0.70

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) 74HCT +25			−40 to +85		−40 to +125		UNIT	TEST CONDITIONS V_{CC} V	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
$t_{PHL}/$ t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$		11	20		25		30	ns	4.5	Fig. 5
$t_{PZH}/$ t_{PZL}	3-state output enable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$		13	30		38		45	ns	4.5	Fig. 6
$t_{PHZ}/$ t_{PLZ}	3-state output disable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$		13	25		31		38	ns	4.5	Fig. 6
$t_{THL}/$ t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 5

AC WAVEFORMS

Fig. 5 Waveforms showing the input $(1A_n, 2A_n)$ to output $(1Y_n, 2Y_n)$ propagation delays and the output transition times.

Fig. 6 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = $ GND to V_{CC}.
   HCT: $V_M = 1.3$ V; $V_I = $ GND to 3 V.