



N-Channel 100-V (D-S) MOSFET

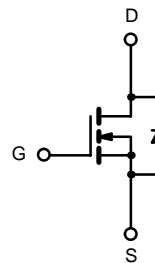
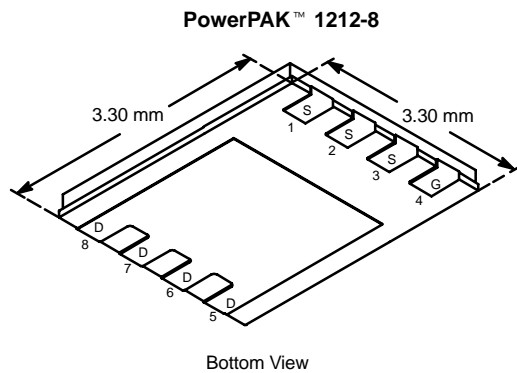
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.062 @ $V_{GS} = 10$ V	5.4
	0.084 @ $V_{GS} = 6$ V	4.6

FEATURES

- TrenchFET® Power MOSFET
- New Low Thermal Resistance
- PowerPAK™ 1212-8 Package with Low 1.07-mm-Profile
- PWM Optimized

APPLICATIONS

- Primary Side Switch
- In-Rush Current Limiter



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	V_{DS}	100		V	
Gate-Source Voltage	V_{GS}	± 20			
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	5.4	3.4	A
		$T_A = 70^\circ\text{C}$	4.3	2.8	
Pulsed Drain Current	I_{DM}	20			
Continuous Source Current (Diode Conduction) ^a	I_S	3.2	1.3		
Single Avalanche Current	$L = 0.1$ mH	I_{AS}	19		
Single Avalanche Energy			E_{AS}	18	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	3.8	1.5	W
		$T_A = 70^\circ\text{C}$	2.0	0.8	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ sec	26	33	$^\circ\text{C/W}$
		Steady State	65	81	
Maximum Junction-to-Case (Drain)	R_{thJC}	1.9	2.4		

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

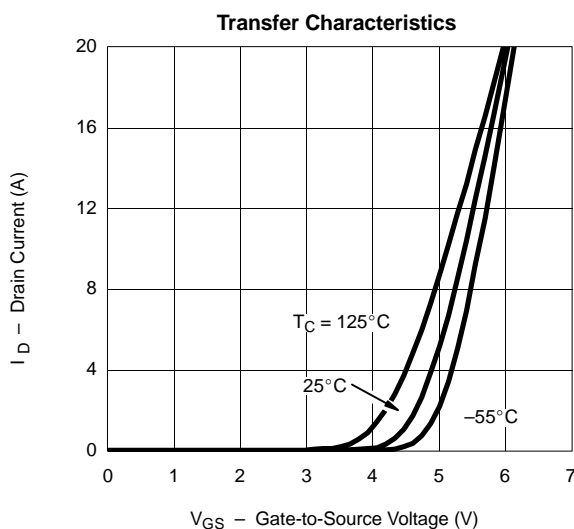
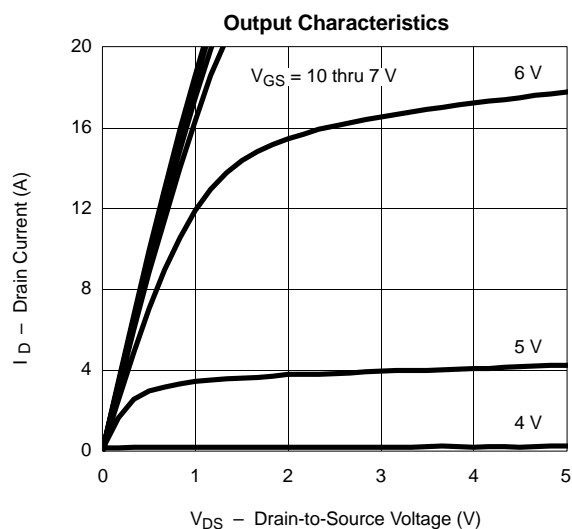
MOSFET SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA
		$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5 \text{ V}, V_{GS} = 10 \text{ V}$	20			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 5.4 \text{ A}$		0.052	0.062	Ω
		$V_{GS} = 6 \text{ V}, I_D = 4.6 \text{ A}$		0.070	0.084	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15 \text{ V}, I_D = 5.4 \text{ A}$		12		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 3.2 \text{ A}, V_{GS} = 0 \text{ V}$		0.78	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 5.4 \text{ A}$		13.5	17	nC
Gate-Source Charge	Q_{gs}			3		
Gate-Drain Charge	Q_{gd}			4.6		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50 \text{ V}, R_L = 50 \Omega$ $I_D \cong 1 \text{ A}, V_{GEN} = 10 \text{ V}, R_G = 6 \Omega$		10	15	ns
Rise Time	t_r			15	25	
Turn-Off Delay Time	$t_{d(off)}$			20	30	
Fall Time	t_f			15	25	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 3.2 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		45	90	

Notes

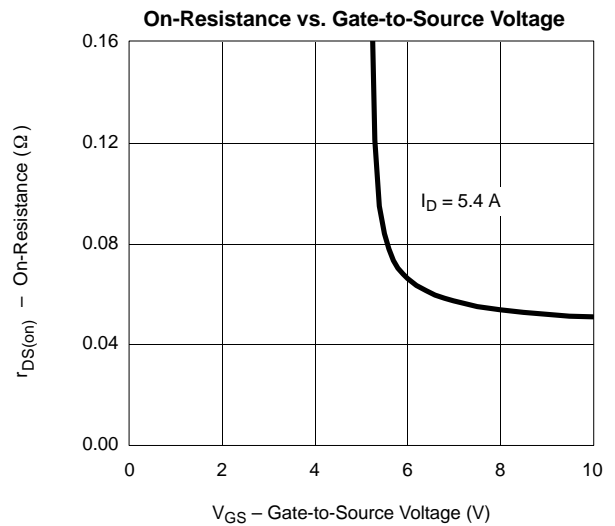
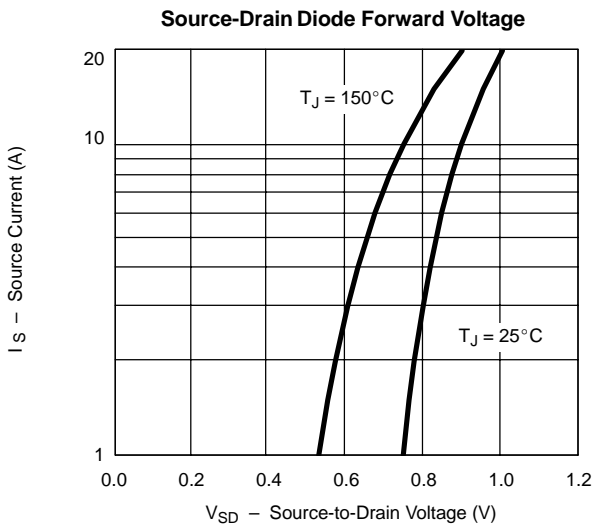
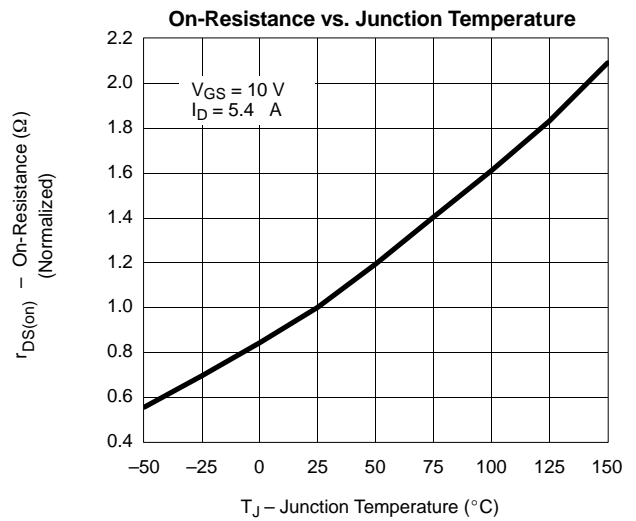
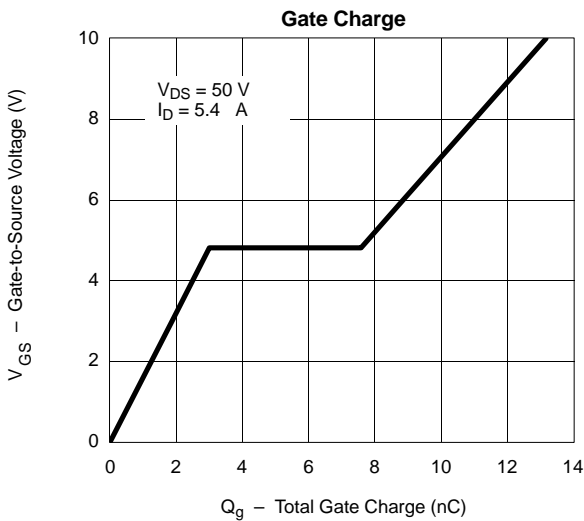
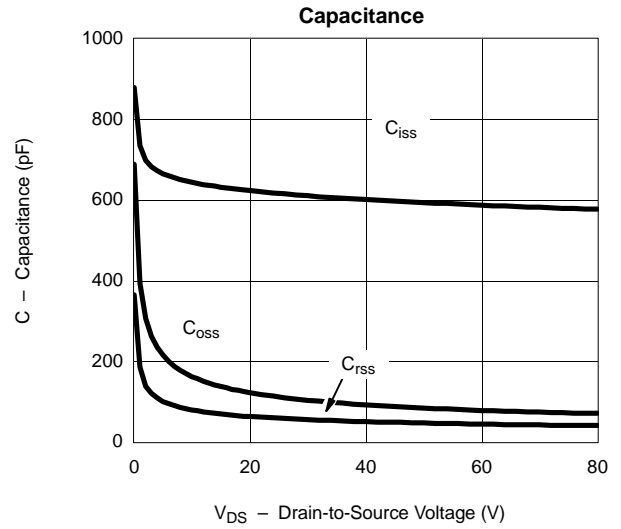
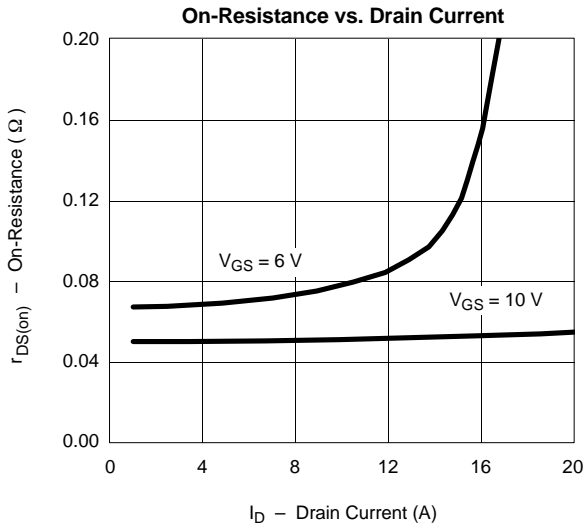
- Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





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