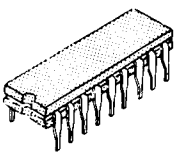
HM472114A-1, HM472114A-2, HM472114AP-1, HM472114AP-2

1024-word × 4-bit Static Random Access Memory

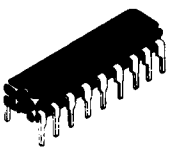
- Fast Access Time ..... HM472114A-1 150ns (max.)
  HM472114A-2 200ns (max.)
- Low Operating Power ..... 200mW (typ.)
- Single +5V Supply
- Completely Static Memory ..... No Clock or Refresh Required
- Fully TTL Compatible ..... All Inputs and Output
- Common Data Input and Output Using Three-state Outputs
- N-channel Si Gate MOS Technology
- Pin Equivalent with Intel 2114L Series

HM472114A-1, HM472114A-2



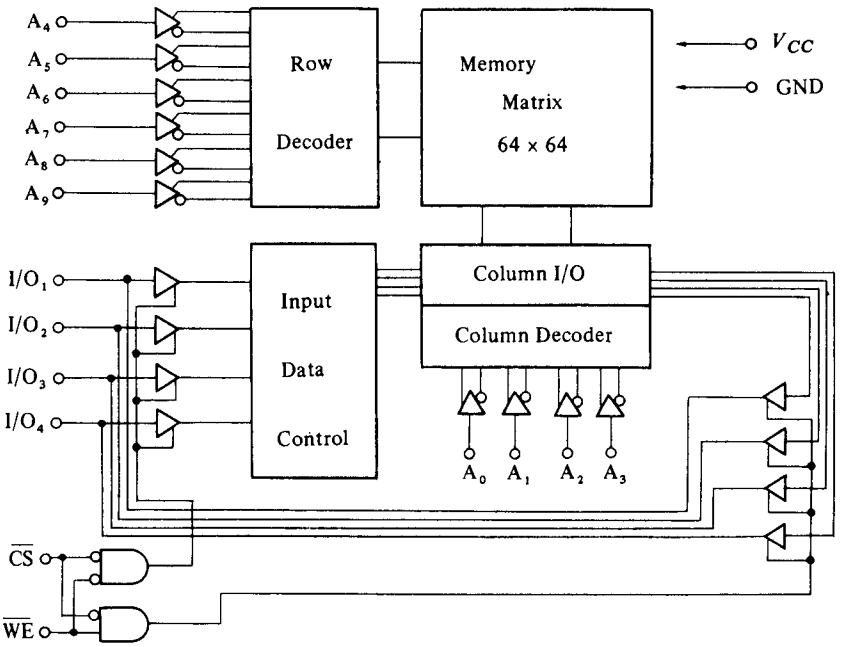
(DG-18)

HM472114AP-1, HM472114AP-2

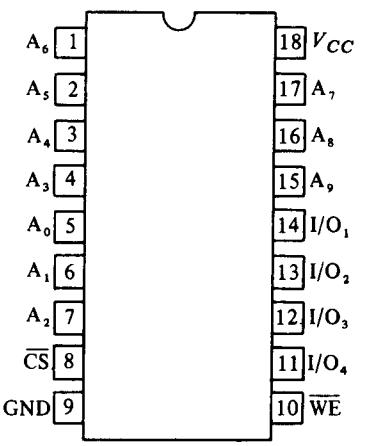


(DP-18)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Terminal Voltage*	V_T	−0.5 to +7	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (Ceramic)	T_{stg}	−65 to +150	°C
Storage Temperature (Plastic)	T_{stg}	−55 to +125	°C

* In respect to GND.

■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IL}	−0.5	—	0.8	V
	V_{IH}	2.0	—	V_{CC}+1.0	V
Operating Temperature	T_{opr}	0	—	70	°C

HITACHI

■ DC AND OPERATING ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70℃)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{in}=0~5.5V	—	—	10	μA
I/O Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=2.0V, $V_{I/O}$=0.4V~V_{CC}	—	—	10	μA
Supply Current	I_{CC}	V_{in}=5.5V, $I_{I/O}$=0mA	—	35	60*	mA
Input Voltage	V_{IL}		−0.5	—	0.8	V
	V_{IH}		2.0	—	V_{CC}+1.0	V
Output Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.4	V
	V_{OH}	I_{OH}=−0.6mA(V_{CC}=4.5V)	2.4	—	—	V
		I_{OH}=−1.0mA(V_{CC}=4.75V)	2.4	—	—	

Note) * : in respect to HM472114A-2. This value of HM472114A-1 is 70mA.

■ CAPACITANCE (Ta=25℃, f=1MHz)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance	C_{in}	V_{in}=0V	—	3	5	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	5	7	pF

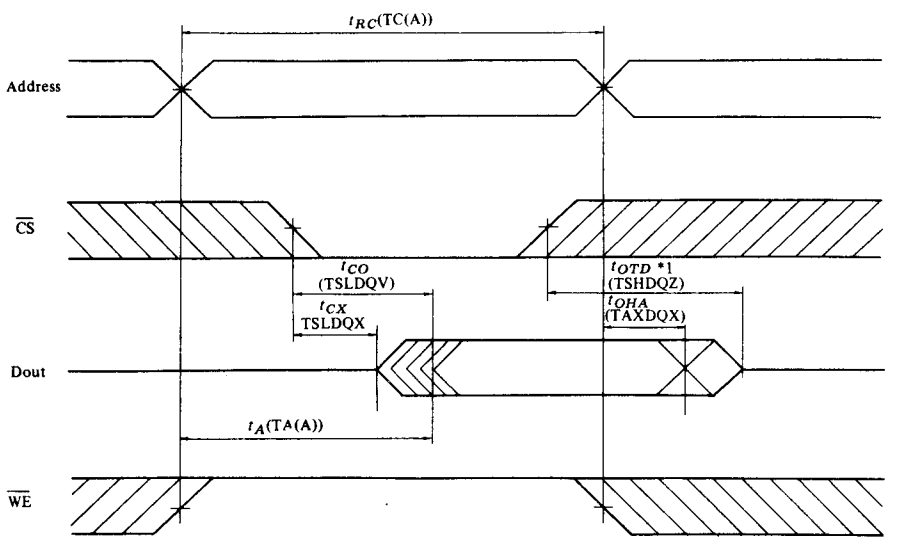
■ AC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70℃)

- **AC TEST CONDITIONS**

Input Pulse Levels ..... 0.8V to 2.4V
Input Rise and Fall Times 10ns
Input and Output Timing Levels 1.5V
Output Load ..... **1 TTL Gate and C_L = 100pF**

- **READ CYCLE**

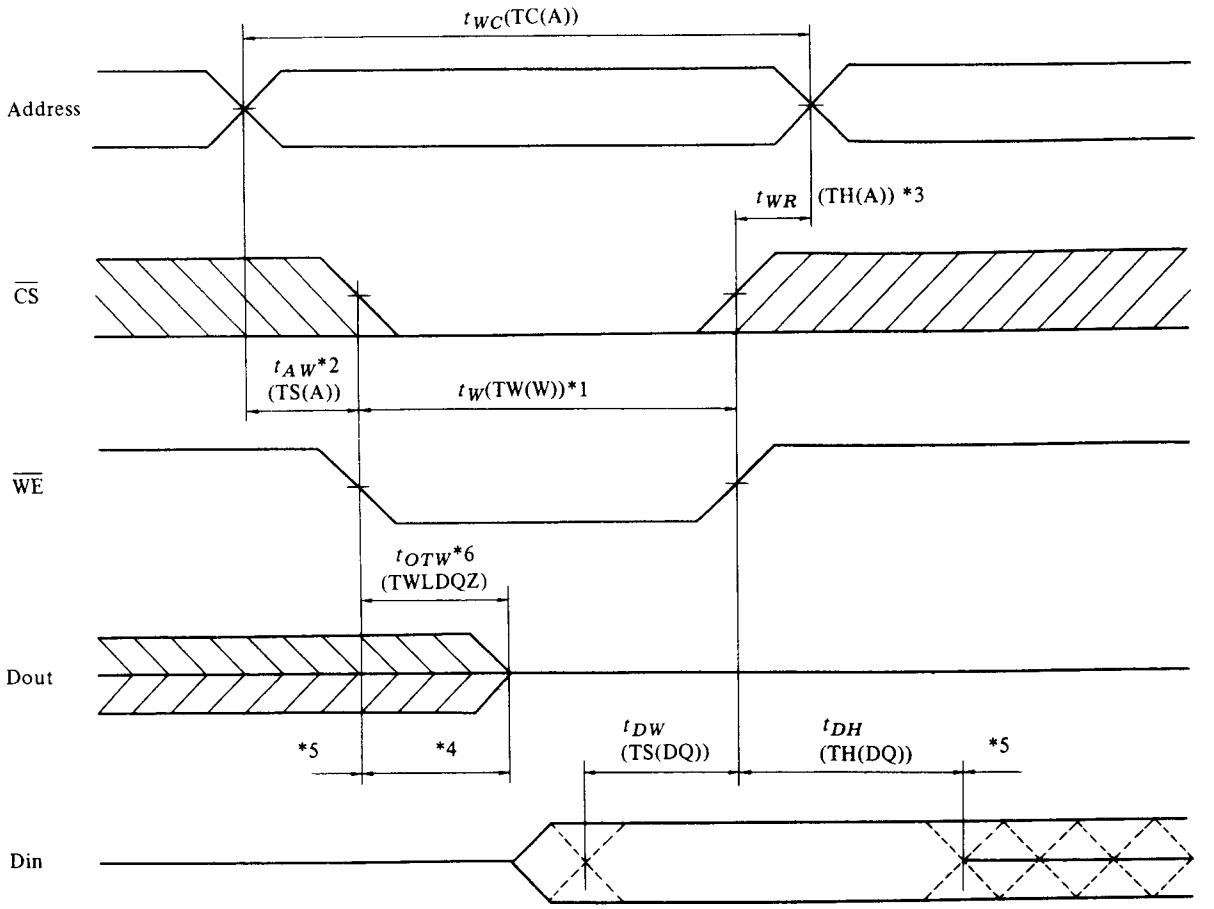
Item	Symbol	HM472114A-1		HM472114A-2		Unit
		min.	max.	min.	max.	
Read Cycle Time	t_{RC}	150	—	200	—	ns
Access Time	t_A	—	150	—	200	ns
$\overline{CS}$ to Output Valid	t_{CO}	—	70	—	70	ns
$\overline{CS}$ to Output Active	t_{CX}	10	—	10	—	ns
Output 3-state from Deselection	t_{OTD}	—	60	—	60	ns
Output Hold from Address Change	t_{OHA}	20	—	50	—	ns



NOTE: 1) t_{OTD} defines the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels.

• WRITE CYCLE

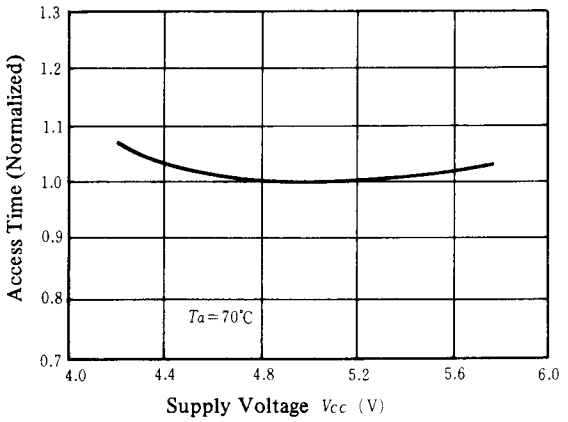
Item	Symbol	HM472114A-1		HM472114A-2		Unit
		min.	max.	min.	max.	
Write Cycle Time	t_{WC}	150	—	200	—	ns
Address to Write Setup Time	t_{AW}	20	—	20	—	ns
Write Pulse Width	t_W	120	—	120	—	ns
Write Release Time	t_{WR}	0	—	0	—	ns
Output 3-state from Write	t_{OTW}	—	60	—	60	ns
Data to Write Time Overlap	t_{DW}	70	—	120	—	ns
Data Hold from Write Time	t_{DH}	0	—	0	—	ns



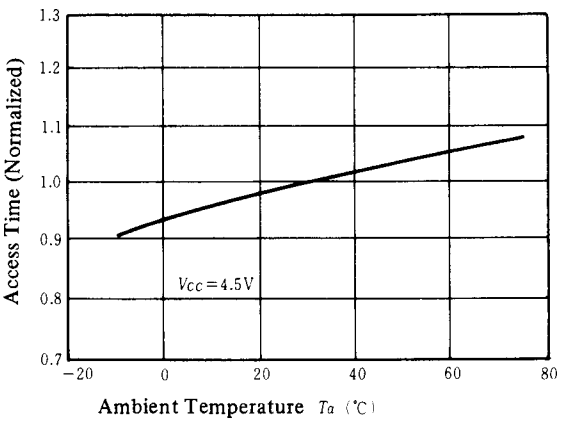
NOTE:

1) A Write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_W).
2) t_{AW} is measured from the address setting to the latter of $\overline{CS}$ or $\overline{WE}$ going low.
3) t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4) During this period I/O pins are in the output state, so that the input signals of opposite phase to the outputs must not be applied to them.
5) If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the input signals of opposite phase to the outputs must not be applied to them.
6) t_{OTW} defines the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels.

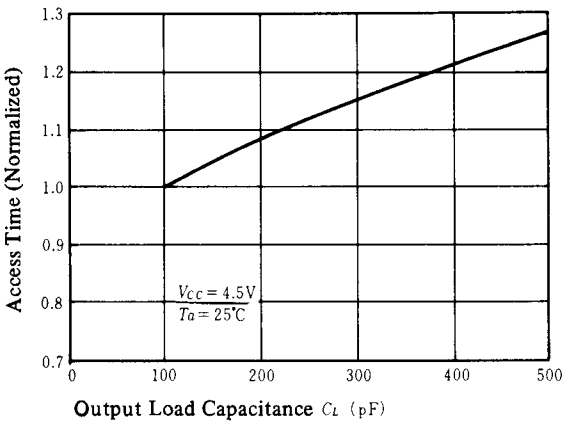
ACCESS TIME vs. SUPPLY VOLTAGE



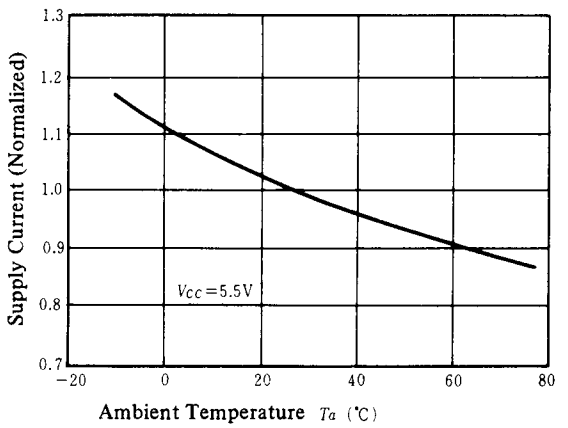
ACCESS TIME vs. AMBIENT TEMPERATURE



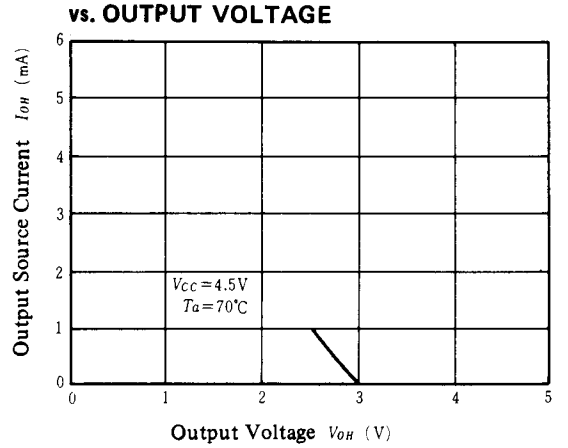
ACCESS TIME vs. OUTPUT LOAD CAPACITANCE



SUPPLY CURRENT vs. AMBIENT TEMPERATURE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE