SN64BCT543
OCTAL REGISTERED BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS
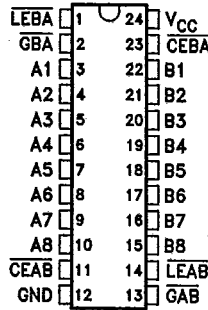
T-52-31

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- State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015
- Package Options Include "Small-Outline" Packages and Standard 300-mil DIPs

description

The SN64BCT543 is a noninverting octal bus transceiver. It contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable ($\overline{LEAB}$ and $\overline{LEBA}$) and output-enable ($\overline{GAB}$ and $\overline{GBA}$) inputs permit independent control for either direction of data flow.

When the A-to-B chip enable ($\overline{CEAB}$) is high, the latches are in storage mode and the B outputs are in the high-impedance state. When $\overline{CEAB}$ is low, latch characteristics and B-output functionality are controlled by $\overline{LEAB}$ and $\overline{GAB}$ as follows:
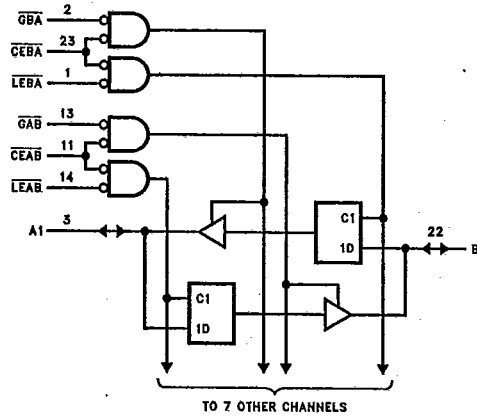
- when $\overline{LEAB}$ is low, the latches are transparent; taking $\overline{LEAB}$ high stores the data present at the A inputs.

- when $\overline{GAB}$ is low, the B outputs are active (high or low logic level) and reflect the data present in the A-to-B latches; when $\overline{GAB}$ is high, the B outputs are in the high-impedance state.

B-to-A data flow is controlled via the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{GBA}$ inputs in a manner analogous to that described above for A-to-B data flow.

The SN64BCT543 featues power-up three-state circuitry for hot-card insertion applications.

The SN64BCT543 is characterized for operation from 0°C to 70°C and from —40°C to 125°C.

DW OR NT PACKAGE
(TOP VIEW)

$\overline{LEBA}$	1	24	V_{CC}
$\overline{GBA}$	2	23	$\overline{CEBA}$
A1	3	22	B1
A2	4	21	B2
A3	5	20	B3
A4	6	19	B4
A5	7	18	B5
A6	8	17	B6
A7	9	16	B7
A8	10	15	B8
$\overline{CEAB}$	11	14	$\overline{LEAB}$
GND	12	13	$\overline{GAB}$

logic diagram (positive logic)

TO 7 OTHER CHANNELS

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