

To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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HD74LV161A

Synchronous 4-bit Binary Counter (Direct Clear)

REJ03D0319-0400Z
 (Previous ADE-205-264B (Z))
 Rev.4.00
 Jun. 04, 2004

Description

The HD74LV161A is 4-bit binary counters. All flip flops are clocked simultaneously on the low to high to transition (positive edge) of the clock input waveform. These counters may be preset using the load input. Presetting of all four flip flops is synchronous to the rising edge of clock. When load is held low counting is disabled and the data on the A, B, C and D inputs is loaded into the counter on the rising edge clock. If the load input is taken high before the positive edge of clock, the count operation will be unaffected.

Low-voltage and high-speed operation is suitable for the battery-powered products (e.g., notebook computers), and the low-power consumption extends the battery life.

Features

- $V_{CC} = 2.0\text{ V}$ to 5.5 V operation
- All inputs $V_{IH} (\text{Max.}) = 5.5\text{ V}$ (@ $V_{CC} = 0\text{ V}$ to 5.5 V)
- All outputs $V_O (\text{Max.}) = 5.5\text{ V}$ (@ $V_{CC} = 0\text{ V}$)
- Typical V_{OL} ground bounce $< 0.8\text{ V}$ (@ $V_{CC} = 3.3\text{ V}$, $T_a = 25^\circ\text{C}$)
- Typical V_{OH} undershoot $> 2.3\text{ V}$ (@ $V_{CC} = 3.3\text{ V}$, $T_a = 25^\circ\text{C}$)
- Output current $\pm 6\text{ mA}$ (@ $V_{CC} = 3.0\text{ V}$ to 3.6 V), $\pm 12\text{ mA}$ (@ $V_{CC} = 4.5\text{ V}$ to 5.5 V)
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LV161AFPEL	SOP-16 pin(JEITA)	FP-16DAV	FP	EL (2,000 pcs/reel)
HD74LV161ARPEL	SOP-16 pin(JEDEC)	FP-16DNV	RP	EL (2,500 pcs/reel)
HD74LV161ATELL	TSSOP-16 pin	TTP-16DAV	T	ELL (2,000 pcs/reel)

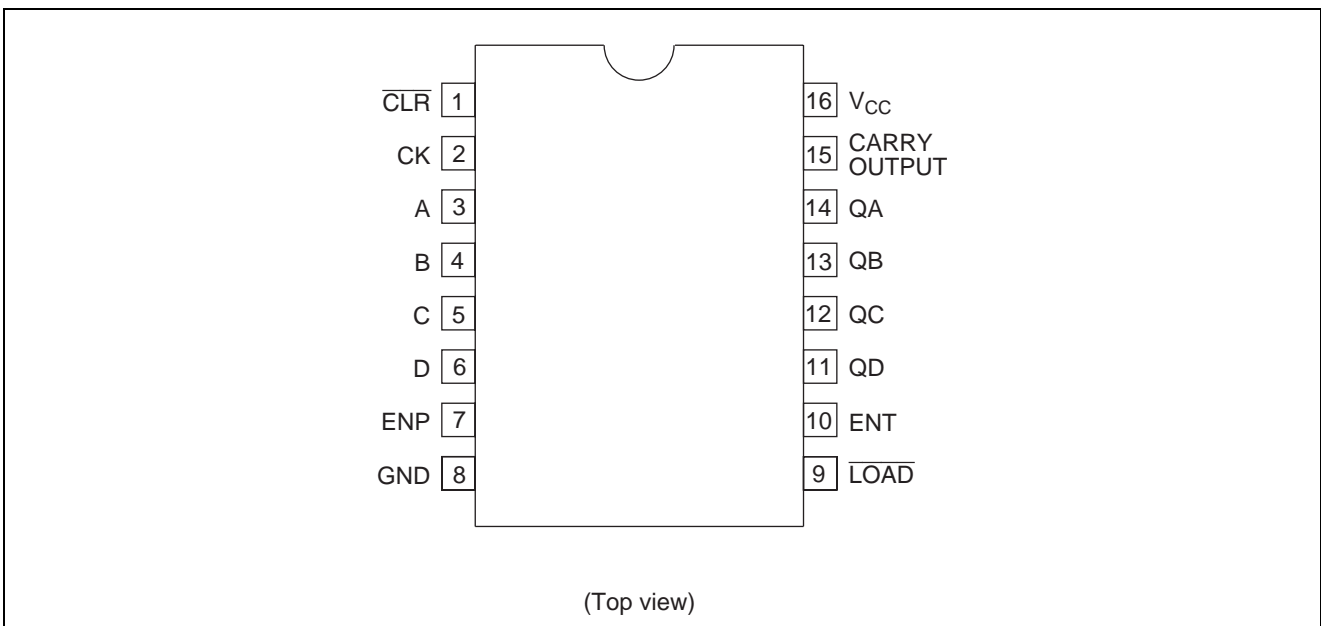
Note: Please consult the sales office for the above package availability.

Function Table

Inputs					Outputs			
CLR	LOAD	ENP	ENT	CLK	QA	QB	QC	QD
L	X	X	X	X	L	L	L	L
H	L	X	X	↑	A	B	C	D
H	H	X	L	↑	No change			
H	H	L	X	↑	No change			
H	H	H	H	↑	Count up			
H	X	X	X	↓	No change			

Note: H: High level
 L: Low level
 X: Immaterial
 ↑: Low to high transition
 ↓: High to low transition
 A, B, C, D: Data input
 Carry = ENT • QA • QB • QC • QD

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CC}	-0.5 to 7.0	V	
Input voltage range* ¹	V_I	-0.5 to 7.0	V	H or L
Output voltage range* ^{1,2}	V_O	-0.5 to $V_{CC} + 0.5$ -0.5 to 7.0	V	Output: H or L V_{CC} : OFF
Input clamp current	I_{IK}	-20	mA	$V_I < 0$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	±25	mA	$V_O = 0$ to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	±50	mA	
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air)* ³	P_T	785 500	mW	SOP TSSOP
Storage temperature	T_{stg}	-65 to 150	°C	

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

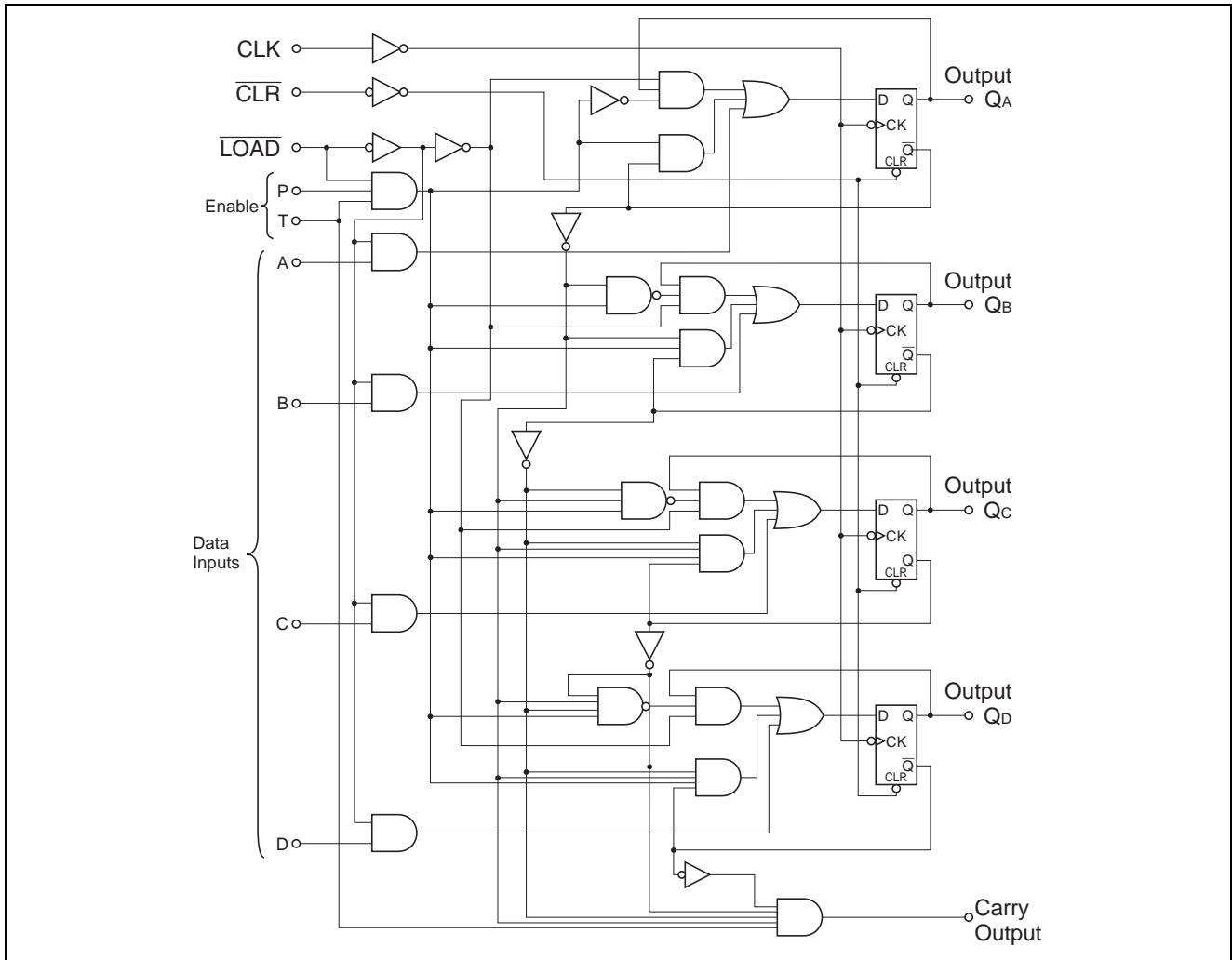
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

Recommended Operating Conditions

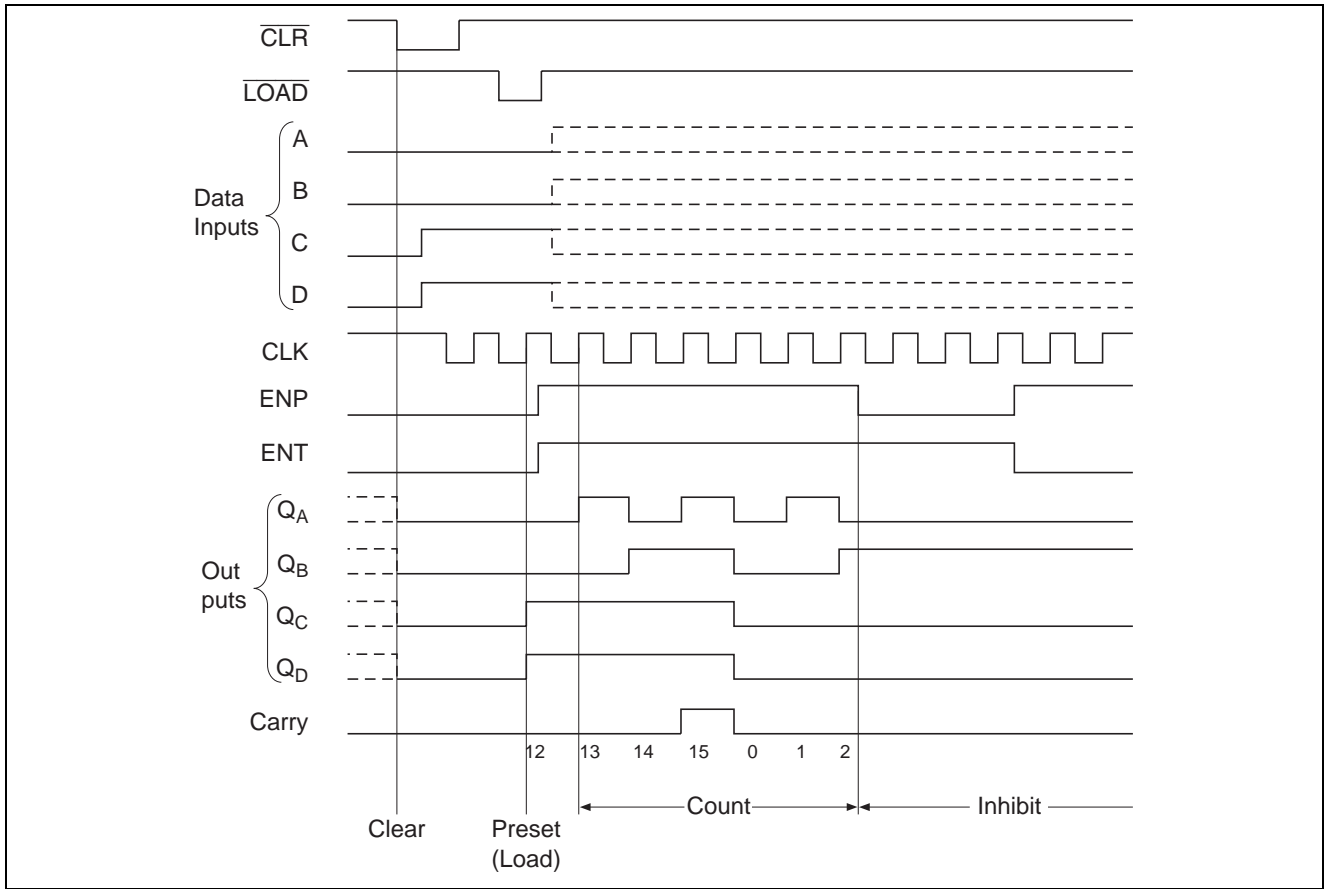
Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	V_{CC}	2.0	5.5	V	
Input voltage range	V_I	0	5.5	V	
Output voltage range	V_O	0	V_{CC}	V	
Output current	I_{OH}	—	-50	μA	$V_{CC} = 2.0\text{ V}$
		—	-2	mA	$V_{CC} = 2.3$ to 2.7 V
		—	-6		$V_{CC} = 3.0$ to 3.6 V
		—	-12		$V_{CC} = 4.5$ to 5.5 V
	I_{OL}	—	50	μA	$V_{CC} = 2.0\text{ V}$
		—	2	mA	$V_{CC} = 2.3$ to 2.7 V
		—	6		$V_{CC} = 3.0$ to 3.6 V
		—	12		$V_{CC} = 4.5$ to 5.5 V
Input transition rise or fall rate	$\Delta t / \Delta v$	0	200	ns/V	$V_{CC} = 2.3$ to 2.7 V
		0	100		$V_{CC} = 3.0$ to 3.6 V
		0	20		$V_{CC} = 4.5$ to 5.5 V
Operating free-air temperature	T_a	-40	85	°C	

Note: Unused or floating inputs must be held high or low.

Logic Diagram



Timing Diagram



DC Electrical Characteristics

Ta = -40 to 85°C

Item	Symbol	V _{CC} (V)*	Min	Typ	Max	Unit	Test Conditions		
Input voltage	V _{IH}	2.0	1.5	—	—	V			
		2.3 to 2.7	V _{CC} × 0.7	—	—				
		3.0 to 3.6	V _{CC} × 0.7	—	—				
		4.5 to 5.5	V _{CC} × 0.7	—	—				
	V _{IL}	2.0	—	—	0.5				
		2.3 to 2.7	—	—	V _{CC} × 0.3				
		3.0 to 3.6	—	—	V _{CC} × 0.3				
		4.5 to 5.5	—	—	V _{CC} × 0.3				
Output voltage	V _{OH}	Min to Max	V _{CC} - 0.1	—	—	V	I _{OL} = -50 μA		
		2.3	2.0	—	—		I _{OL} = -2 mA		
		3.0	2.48	—	—		I _{OL} = -6 mA		
		4.5	3.8	—	—		I _{OL} = -12 mA		
	V _{OL}	Min to Max	—	—	0.1		I _{OL} = 50 μA		
		2.3	—	—	0.4		I _{OL} = 2 mA		
		3.0	—	—	0.44		I _{OL} = 6 mA		
		4.5	—	—	0.55		I _{OL} = 12 mA		
	Input current	I _{IN}	0 to 5.5	—	—		±1	μA	V _{IN} = 5.5 V or GND
	Quiescent supply current	I _{CC}	5.5	—	—		20	μA	V _{IN} = V _{CC} or GND, I _O = 0
Output leakage current	I _{OFF}	0	—	—	5	μA	V _I or V _O = 0 V to 5.5 V		
Input capacitance	C _{IN}	3.3	—	1.7	—	pF	V _I = V _{CC} or GND		

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

V_{CC} = 2.5 ± 0.2 V

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	f _{max}	50	90	—	40	—	MHz	C _L = 15 pF		
		30	60	—	25	—		C _L = 50 pF		
Propagation delay time	t _{PLH} /t _{PHL}	—	11.1	16.2	1.0	19.5	ns	C _L = 15 pF	CLK	Q
		—	14.3	19.2	1.0	22.5		C _L = 50 pF		
	t _{PLH} /t _{PHL} Count mode	—	11.5	17.0	1.0	20.5		C _L = 15 pF	CLK	Carry
		—	14.7	20.0	1.0	23.5		C _L = 50 pF		
	t _{PLH} /t _{PHL} Load mode	—	13.8	20.6	1.0	24.5		C _L = 15 pF	CLK	Carry
		—	17.0	23.6	1.0	27.5		C _L = 50 pF		
	t _{PLH} /t _{PHL}	—	10.3	15.7	1.0	19.0		C _L = 15 pF	ENT	Carry
		—	14.0	18.7	1.0	22.0		C _L = 50 pF		
	t _{PHL}	—	11.7	17.0	1.0	20.5		C _L = 15 pF	$\overline{\text{CLR}}$	Q
		—	14.7	20.0	1.0	23.5		C _L = 50 pF		
t _{PHL}	—	11.2	16.6	1.0	20.0		C _L = 15 pF	CLR	Carry	
	—	14.4	19.6	1.0	23.0		C _L = 50 pF			
Setup time	t _{su}	7.5	—	—	8.5	—	ns		Data before CLK ↑	
		10.0	—	—	11.5	—		$\overline{\text{LOAD}}$ before CLK ↑		
		9.5	—	—	11.0	—		ENT, ENP before CLK ↑		
		4.5	—	—	4.5	—		$\overline{\text{CLR}}$ inactive before CLK ↑		
Hold time	t _h	1.5	—	—	1.5	—	ns			
Pulse width	t _w	7.0	—	—	7.0	—	ns		CLK H or L	
		7.0	—	—	7.0	—		CLR L		

Switching Characteristics (cont)

V_{CC} = 3.3 ± 0.3 V

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	f _{max}	80	130	—	70	—	MHz	C _L = 15 pF		
		55	85	—	50	—		C _L = 50 pF		
Propagation delay time	t _{PLH} /t _{PHL}	—	8.3	12.8	1.0	15.0	ns	C _L = 15 pF	CLK	Q
		—	10.8	16.3	1.0	18.5		C _L = 50 pF		
	t _{PLH} /t _{PHL} Count mode	—	8.7	13.6	1.0	16.0		C _L = 15 pF	CLK	Carry
		—	11.2	17.1	1.0	19.5		C _L = 50 pF		
	t _{PLH} /t _{PHL} Load mode	—	11.0	17.2	1.0	20.0		C _L = 15 pF	CLK	Carry
		—	13.5	20.7	1.0	23.5		C _L = 50 pF		
	t _{PLH} /t _{PHL}	—	7.5	12.3	1.0	14.5		C _L = 15 pF	ENT	Carry
		—	10.5	15.8	1.0	18.0		C _L = 50 pF		
	t _{PHL}	—	8.9	13.6	1.0	16.0		C _L = 15 pF	CLR	Q
		—	11.2	17.1	1.0	19.5		C _L = 50 pF		
t _{PHL}	—	8.4	13.2	1.0	15.5		C _L = 15 pF	CLR	Carry	
	—	10.9	16.7	1.0	19.0		C _L = 50 pF			
Setup time	t _{su}	5.5	—	—	6.5	—	ns		Data before CLK ↑	
		8.0	—	—	9.5	—			LOAD before CLK ↑	
		7.5	—	—	9.0	—			ENT, ENP before CLK ↑	
		2.5	—	—	2.5	—			CLR inactive before CLK ↑	
Hold time	t _h	1.0	—	—	1.0	—	ns			
Pulse width	t _w	5.0	—	—	5.0	—	ns		CLK H or L	
		5.0	—	—	5.0	—			CLR L	

Switching Characteristics (cont)

V_{CC} = 5.0 ± 0.5 V

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	f _{max}	135	185	—	115	—	MHz	C _L = 15 pF		
		95	125	—	85	—		C _L = 50 pF		
Propagation delay time	t _{PLH} /t _{PHL}	—	4.9	8.1	1.0	9.5	ns	C _L = 15 pF	CLK	Q
		—	8.7	10.1	1.0	11.5		C _L = 50 pF		
	t _{PLH} /t _{PHL}	—	4.9	8.1	1.0	9.5		C _L = 15 pF	CLK	Carry
	Count mode	—	6.4	10.1	1.0	11.5		C _L = 50 pF		
	t _{PLH} /t _{PHL}	—	6.2	10.3	1.0	12.0		C _L = 15 pF	CLK	Carry
	Load mode	—	7.7	12.3	1.0	14.0		C _L = 50 pF		
	t _{PLH} /t _{PHL}	—	4.9	8.1	1.0	9.5		C _L = 15 pF	ENT	Carry
		—	6.4	10.1	1.0	11.5		C _L = 50 pF		
	t _{PHL}	—	5.5	9.0	1.0	10.5		C _L = 15 pF	CLR	Q
		—	7.0	11.0	1.0	12.5		C _L = 50 pF		
t _{PHL}	—	5.0	8.6	1.0	10.0		C _L = 15 pF	CLR	Carry	
	—	6.5	10.6	1.0	12.0		C _L = 50 pF			
Setup time	t _{su}	4.5	—	—	4.5	—	ns		Data before CLK ↑	
		5.0	—	—	6.0	—			LOAD before CLK ↑	
		5.0	—	—	6.0	—			ENT, ENP before CLK ↑	
		1.5	—	—	1.5	—			CLR inactive before CLK ↑	
Hold time	t _h	1.0	—	—	1.0	—	ns			
Pulse width	t _w	5.0	—	—	5.0	—	ns		CLK H or L	
		5.0	—	—	5.0	—			CLR L	

Operating Characteristics

C_L = 50 pF

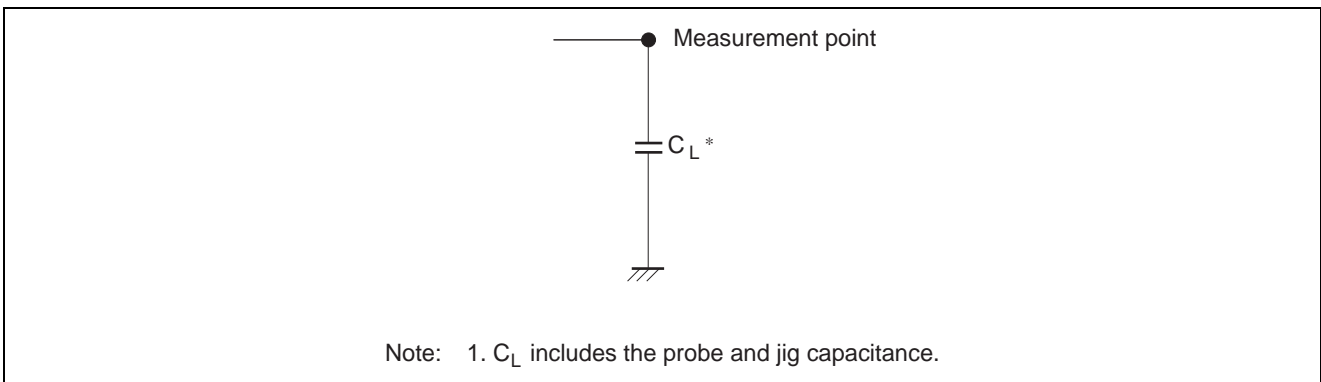
Item	Symbol	V _{CC} (V)	Ta = 25°C			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	C _{PD}	3.3	—	17.0	—	pF	f = 10 MHz
		5.0	—	20.4	—		

Noise Characteristics

$C_L = 50 \text{ pF}$

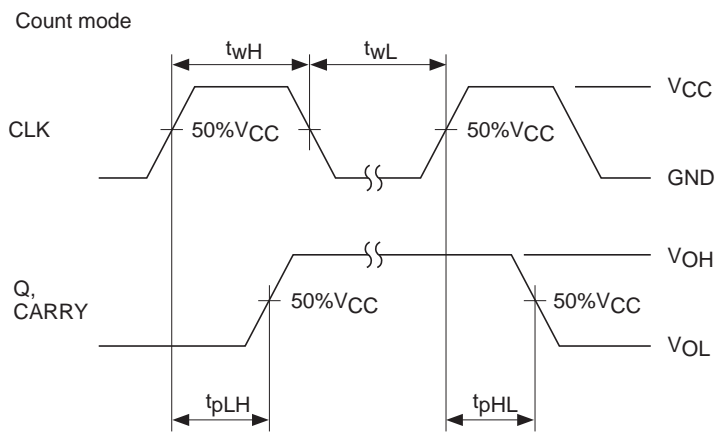
Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			Unit	Test Conditions
			Min	Typ	Max		
Quiet output, maximum dynamic V_{OL}	$V_{OL(P)}$	3.3	—	0.3	0.8	V	
Quiet output, minimum dynamic V_{OL}	$V_{OL(V)}$	3.3	—	-0.3	-0.8	V	
Quiet output, minimum dynamic V_{OH}	$V_{OH(V)}$	3.3	—	3.0	—	V	
High-level dynamic input voltage	$V_{IH(D)}$	3.3	2.31	—	—	V	
Low-level dynamic input voltage	$V_{IL(D)}$	3.3	—	—	0.99	V	

Test Circuit

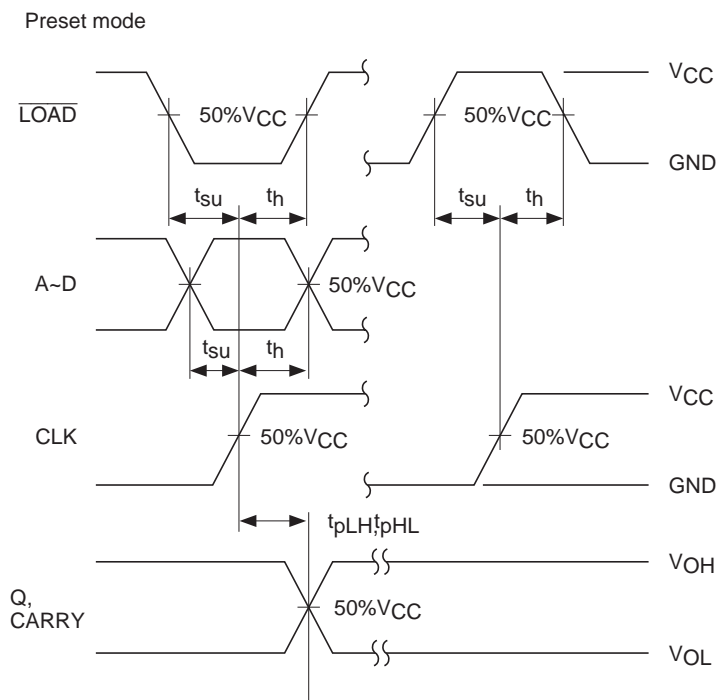


Waveforms

Waveform – 1

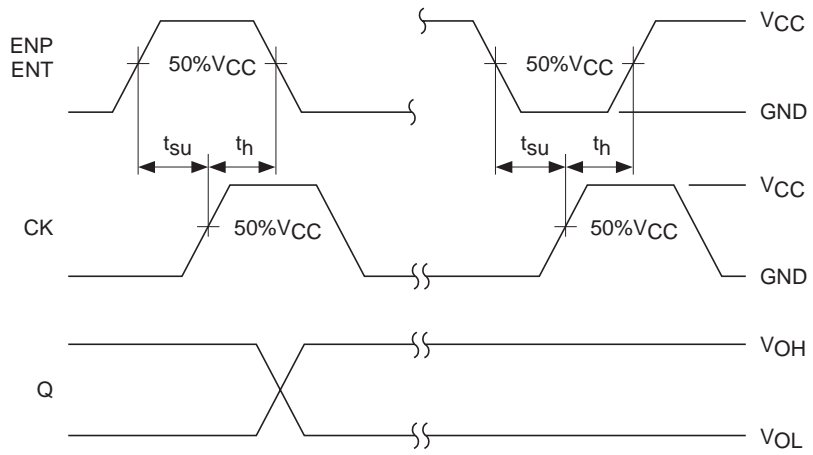


Waveform – 2



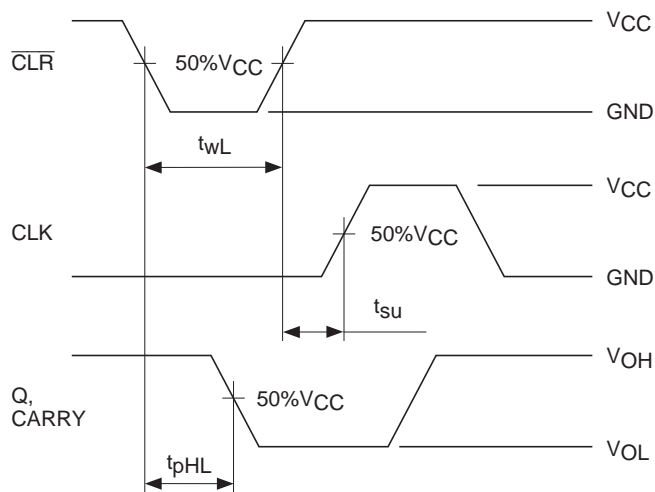
Waveform – 3

Count enable mode



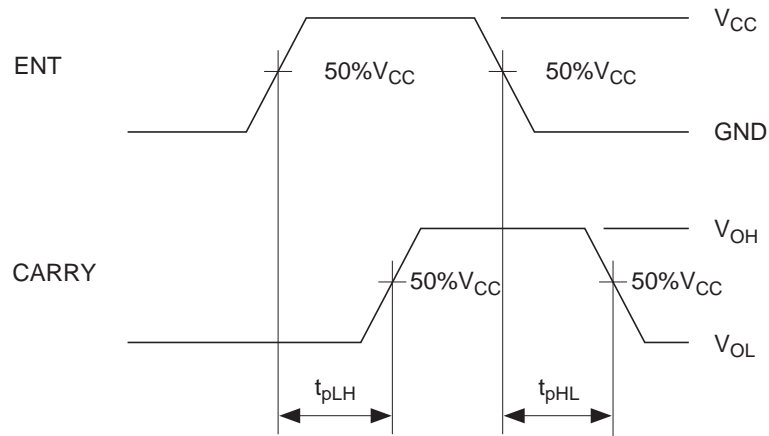
Waveform – 4

Clear mode



Waveform – 5

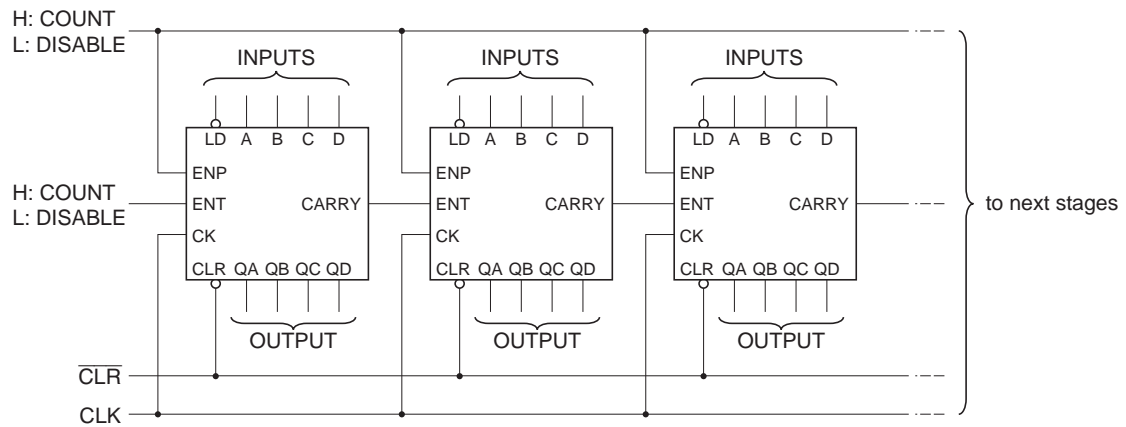
Cascade mode
(Set to maximum count number)



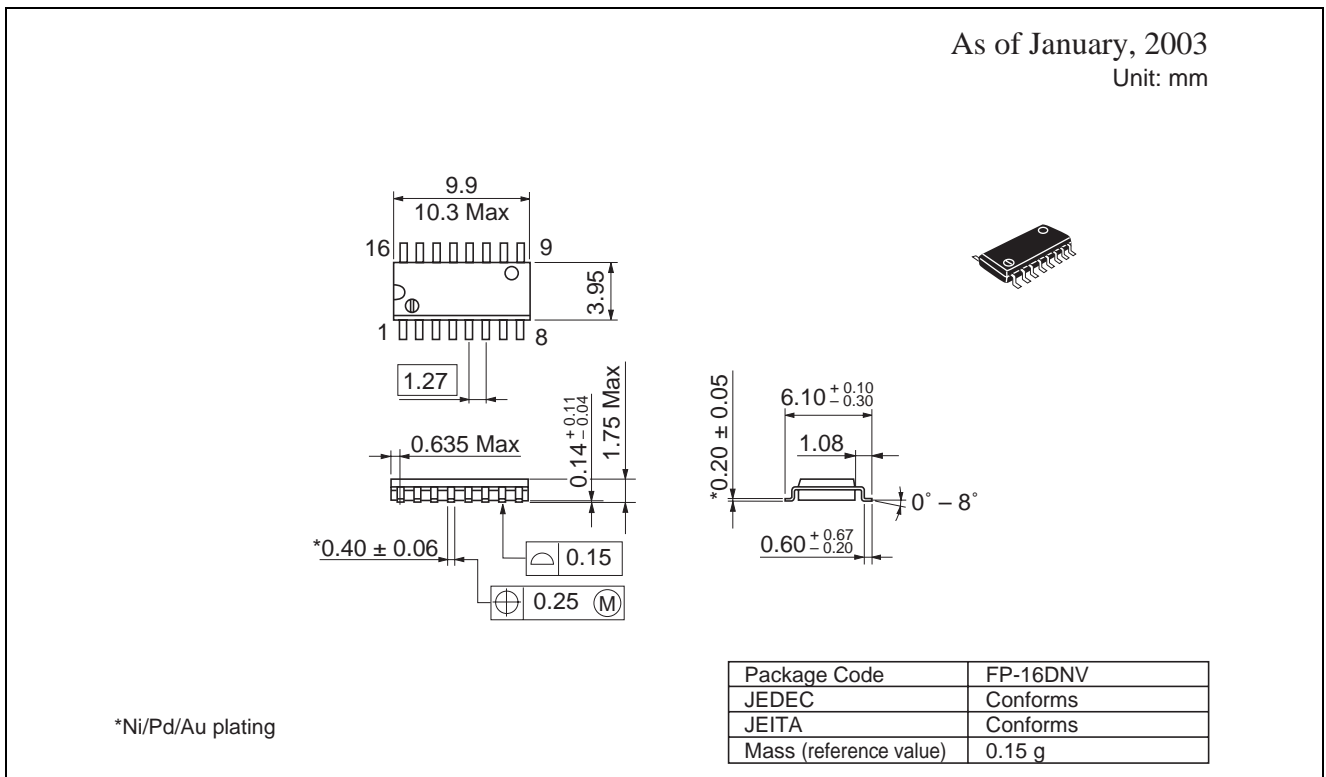
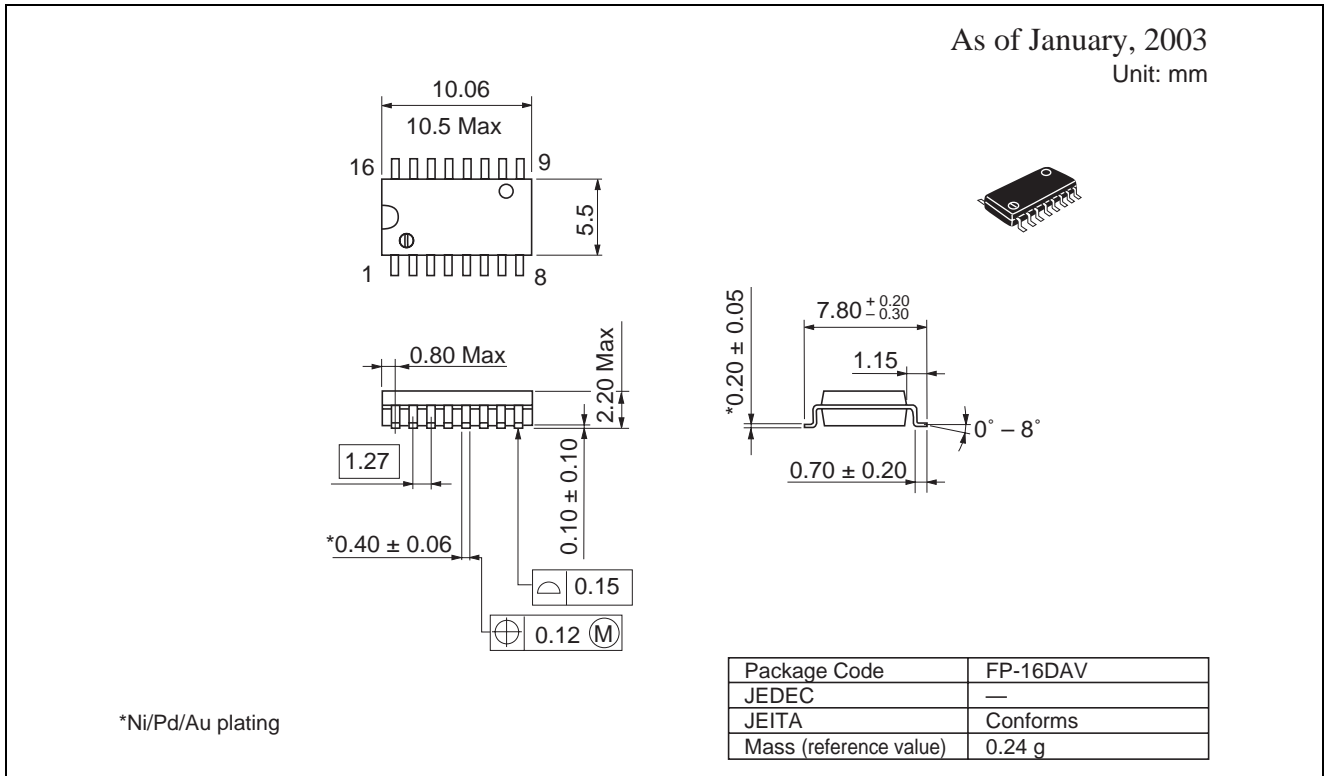
Note: 1. Input waveform: PRR ≤ 1 MHz, Z_o = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns

Application

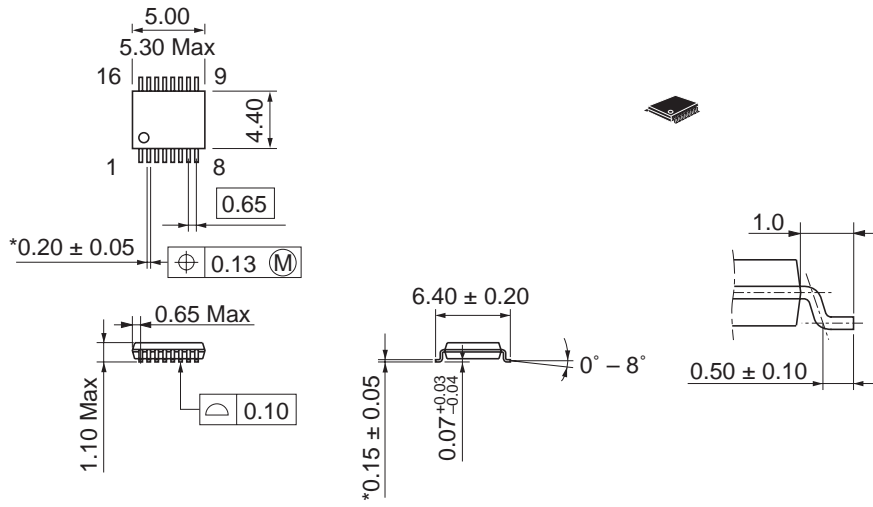
Cascade circuitry



Package Dimensions



As of January, 2003
Unit: mm



*Ni/Pd/Au plating

Package Code	TTP-16DAV
JEDEC	—
JEITA	—
Mass (reference value)	0.05 g

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