MOSFET N-channel depletion switching transistor BSD22

DESCRIPTION

Symmetrical insulated-gate silicon MOS field-effect transistor of the n-channel depletion mode type.The transistor is sealed in a SOT143 envelope and features a low ON-resistance and low capacitances.The transistor is protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

Marking code: M32

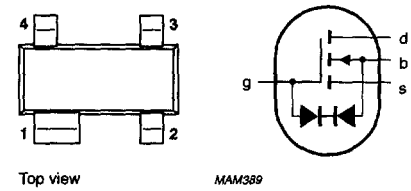

Fig.1 Simplified outline and symbol.

Applications:

- analog and/or digital switch
- switch driver
- convertor
- chopper

PINNING

1 = substrate (b)
2 = source
3 = drain
4 = gate

Note

1. Drain and source are interchangeable

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Gate-source voltage	V_{GS}	max.	+ 15	V
			− 40	V
Drain current (DC)	I_D	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	230	mW
Junction temperature	T_j	max.	125	°C
Drain-source ON-resistance				
V_{GS} = 10 V; V_{SB} = 0; I_D = 1 mA	R_{DSon}	max.	30	Ω
Feed-back capacitance				
V_{GS} = V_{BS} = −5 V; V_{DS} = 10 V; f = 1 MHz	C_{rss}	typ.	0.6	pF

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Source-drain voltage	V_{SD}	max.	20	V
Drain-substrate voltage	V_{DB}	max.	25	V
Source-substrate voltage	V_{SB}	max.	25	V
Gate-substrate voltage	V_{GB}	max.	± 15	V
Gate-source voltage	V_{GS}	max.	+ 15 − 40	V V
Drain current (DC)	I_D	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C[1]	P_{tot}	max.	230	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	125	°C

THERMAL RESISTANCE

From junction to ambient in free air[1]	$R_{th\ j\text{-}a}$	=	430	K/W

Note

1. Device mounted on a ceramic subtrate of 8 mm × 10 mm × 0.7 mm.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Drain-source breakdown voltage				
$V_{GS} = V_{BS} = -5$ V; I_S = 10 nA	$V_{(BR)DSX}$	min.	20	V
Source-drain breakdown voltage				
$V_{GD} = V_{BD} = -5$ V; I_D = 10 nA	$V_{(BR)SDX}$	min.	20	V
Drain-substrate breakdown voltage				
V_{GB} = 0; I_D = 10 nA; open source	$V_{(BR)DBO}$	min.	25	V
Source-substrate breakdown voltage				
V_{GB} = 0; I_S = 10 nA; open drain	$V_{(BR)SBO}$	min.	25	V
Drain-source leakage current				
$V_{GS} = V_{BS} = -5$ V; V_{DS} = 10 V	I_{DSoff}	typ.	1.0	nA
Source-drain leakage current				
$V_{GD} = V_{BD}$ = 5 V; V_{SD} = 10 V	I_{SDoff}	typ.	1.0	nA
Gate-substrate leakage current				
$V_{DB} = V_{SB}$ = 0; V_{GB} = ± 15 V	I_{GBS}	max.	10	nA
Forward transconductance at f = 1 kHz				
V_{DS} = 10 V; V_{SB} = 0; I_D = 20 mA	g_{fs}	min.	10	mS
		typ.	15	mS
Gate-source cut-off voltage				
V_{DS} = 10 V; V_{SB} = 0; I_D = 10 μA	$-V_{(P)GS}$	max.	2.0	V

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Drain-source ON-resistance				
I_D = 1 mA; V_{SB} = 0;				
V_{GS} = 5 V	R_{DSon}	typ.	25	Ω
		max.	50	Ω
V_{GS} = 10 V	R_{DSon}	typ.	15	Ω
		max.	30	Ω
Capacitances at f = 1 MHz				
$V_{GS} = V_{BS}$ = −5 V; V_{DS} = 10 V				
Feed-back capacitance	C_{rss}	typ.	0.6	pF
Input capacitance	C_{iss}	typ.	1.5	pF
Output capacitance	C_{oss}	typ.	1.0	pF
Switching times (see Fig.3)				
V_{DD} = 10 V; V_i = −5 V to + 5 V	t_{on}	typ.	1.0	ns
	t_{off}	typ.	5.0	ns

$C_{iss} = C_{gs} + C_{gd} + C_{gb}$
$C_{oss} = C_{gd} + C_{bd}$
$C_{rss} = C_{gd}$

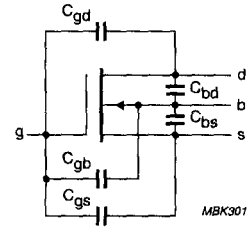
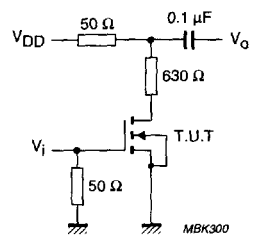


Fig.2 Capacitances model.



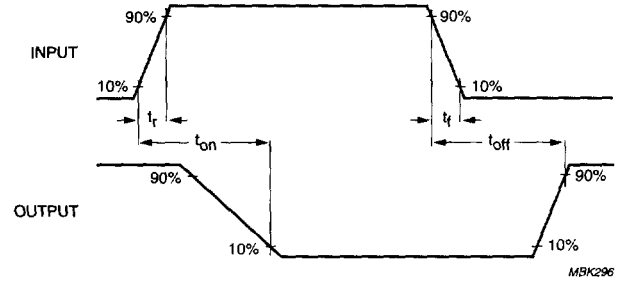


Fig.3 Switching times and input and output waveforms; R_i = 50 Ω; t_r < 0.5 ns; t_f < 1.0 ns; t_p = 20 ns; δ < 0.01.