

FEATURES:

- One high precision N and SSC programmable PLL for CPU
- One high precision N and SSC programmable PLL for SRC[2:1]
- One high precision N and SSC programmable PLL for SRC0 [7:3] (PCI Express)
- One high precision PLL for 48MHz
- Band-gap circuit for differential outputs
- Support multiple spread spectrum modulation, down and center
- Support SMBus block read/write, index read/write
- Selectable output strength for REF, PCI, 48MHz, HTT66
- Available in SSOP and TSSOP packages

KEY SPECIFICATION:

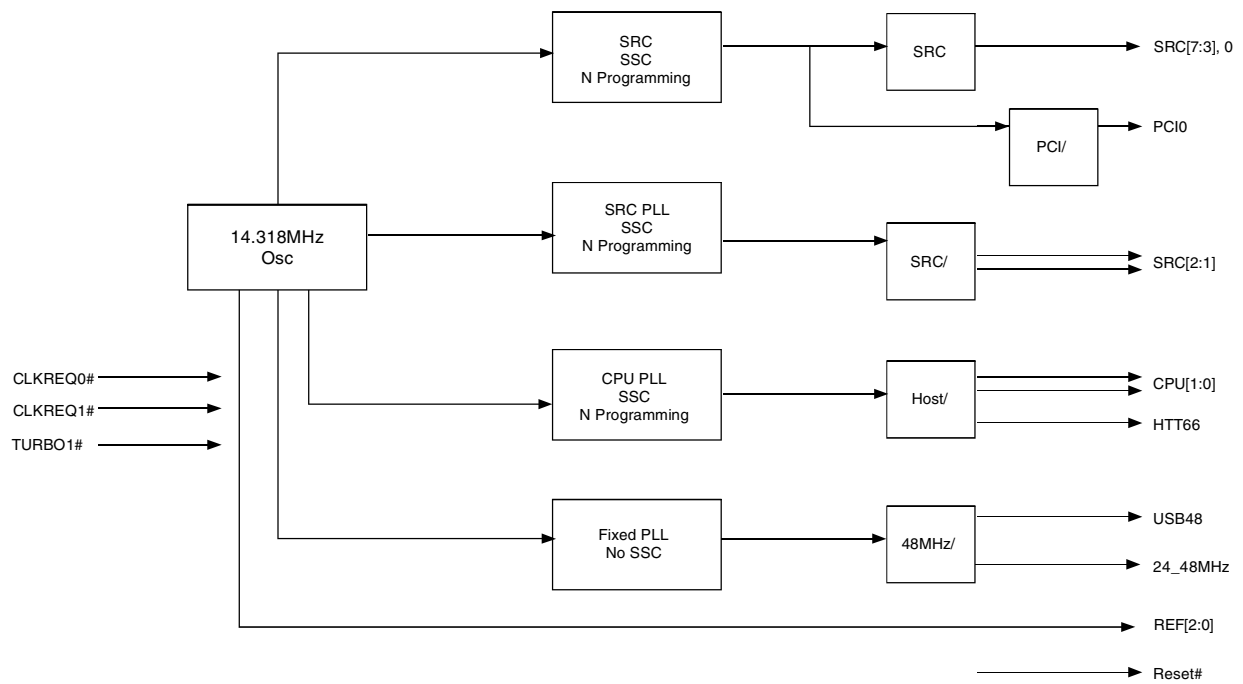
- CPU CLK cycle to cycle jitter < 85ps
- SRC CLK cycle to cycle jitter < 100ps

DESCRIPTION:

IDTCV137 is a 56 pin clock device for AMD advance K8 processors. The CPU output buffer is designed to support up to 400MHz processor. This device also implements Band-gap referenced IREF to reduce the impact of VDD variation on differential outputs, which can provide more robust system performance.

Each CPU/SRC clock has its own Spread Spectrum selection, which allows for isolated changes instead of affecting other clock groups.

FUNCTIONAL BLOCK DIAGRAM

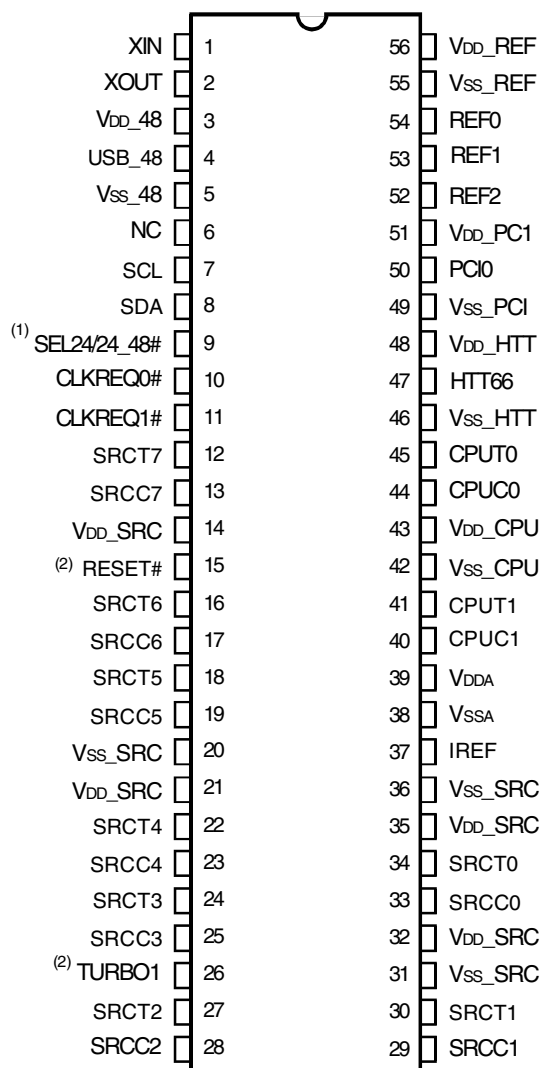


OUTPUT TABLE

| CPU | CLKREQ | SRC | HTT66 | PCI | TURBO | USB48 | 24_48 | REF | RESET# |
|-----|--------|-----|-------|-----|-------|-------|-------|-----|--------|
| 2 | 2 | 8 | 1 | 1 | 1 | 1 | 1 | 3 | 1 |

The IDT logo is a registered trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



CPU AND SRC SPREAD SPECTRUM MAGNITUDE CONTROL

| SMC[2:0] | % |
|----------|--------|
| 000 | OFF |
| 001 | -0.25 |
| 010 | -0.5 |
| 011 | -0.75 |
| 100 | ±0.125 |
| 101 | ±0.25 |
| 110 | ±0.375 |
| 111 | ±0.5 |

SE SIGNAL STRENGTH SELECTION

| Str[1:0] | Strength |
|----------|----------|
| 00 | 0.6x |
| 01 | 0.8x |
| 10 | 1x |
| 11 | 1.2x |

PCI (BASED ON SRC = 100MHz)

| PCIS[1:0] | PCI |
|-----------|-------|
| 00 | 33.33 |
| 01 | 36.36 |
| 10 | 40 |
| 11 | 30.77 |

NOTES:

1. Internal 130KΩ pull-down resistor.
2. Tristate at power on to be compatible with AT1 pin definition.

SSOP/ TSSOP
TOP VIEW

PIN DESCRIPTION

| Pin Name | Type | Pin # | Description |
|------------------------|------------|--|--|
| XIN | IN | 1 | XTAL in |
| XOUT | OUT | 2 | XTAL out |
| PCI0 | OUT | 50 | PCI clock |
| HTT66 | OUT | 47 | 66.66 MHz |
| USB48 | OUT | 4 | 48MHz |
| Turbo1 | IN | 26 | Turbo frequency select |
| CPUC[1:0] CPUT[1:0] | OUT | 40, 41, 44, 45 | Differential clock |
| SRCC[7:0] SRCT[7:0] | OUT | 12, 13, 16, 17, 18, 19, 22, 23, 24, 25, 27, 28, 29, 30, 33, 34 | Differential clock |
| IREF | OUT | 37 | Differential clock reference current |
| REF[0:1] | I/O | 53, 54 | 14.318MHz |
| REF2 | OUT | 52 | 14.318MHz |
| CLKREQ0# | IN | 10 | SRC OE control, see bytes 3, 4 |
| CLKREQ1# | IN | 11 | SRC OE control, see bytes 3, 4 |
| SDA | I/O | 8 | SMBus data |
| SCL | IN | 7 | SMBus clock |
| SEL24/24_48# | IN | 9 | Latched select input for 24 or 48MHz output. 1 = 24MHz, 0 = 48MHz. |
| RESET# | OUT, OD | 15 | Reset output signal, Open Drain |

SM PROTOCOL

INDEX BLOCK WRITE PROTOCOL

| Bit | # of bits | From | Description |
|-------|-----------|--------|--------------------------------------|
| 1 | 1 | Master | Start |
| 2-9 | 8 | Master | D2h |
| 10 | 1 | Slave | Ack (Acknowledge) |
| 11-18 | 8 | Master | Register offset byte (starting byte) |
| 19 | 1 | Slave | Ack (Acknowledge) |
| 20-27 | 8 | Master | Byte count, N (0 is not valid) |
| 28 | 1 | Slave | Ack (Acknowledge) |
| 29-36 | 8 | Master | first data byte (Offset data byte) |
| 37 | 1 | Slave | Ack (Acknowledge) |
| 38-45 | 8 | Master | 2nd data byte |
| 46 | 1 | Slave | Ack (Acknowledge) |
| | | | : |
| | | Master | Nth data byte |
| | | Slave | Acknowledge |
| | | Master | Stop |

INDEX BLOCK READ PROTOCOL

Master can stop reading any time by issuing the stop bit without waiting until Nth byte (byte count bit30-37).

| Bit | # of bits | From | Description |
|-------|-----------|--------|---|
| 1 | 1 | Master | Start |
| 2-9 | 8 | Master | D2h |
| 10 | 1 | Slave | Ack (Acknowledge) |
| 11-18 | 8 | Master | Register offset byte (starting byte) |
| 19 | 1 | Slave | Ack (Acknowledge) |
| 20 | 1 | Master | Repeated Start |
| 21-28 | 8 | Master | D3h |
| 29 | 1 | Slave | Ack (Acknowledge) |
| 30-37 | 8 | Slave | Byte count, N (block read back of N bytes), power on is 8 |
| 38 | 1 | Master | Ack (Acknowledge) |
| 39-46 | 8 | Slave | first data byte (Offset data byte) |
| 47 | 1 | Master | Ack (Acknowledge) |
| 48-55 | 8 | Slave | 2nd data byte |
| | | | Ack (Acknowledge) |
| | | | : |
| | | Master | Ack (Acknowledge) |
| | | Slave | Nth data byte |
| | | | Not acknowledge |
| | | Master | Stop |

INDEX BYTE WRITE

Setting bit[11:18] = starting address, bit[20:27] = 01h.

INDEX BYTE READ

Setting bit[11:18] = starting address. After reading back the first data byte, master issues Stop bit.

BYTE 0

| Bit | Output(s) Affected | Description/Function | 0 | 1 | Type | Power On |
|-----|--------------------|----------------------|----------|--------|------|----------|
| 7 | SRCT7, SRCC7 | Output enable | Tristate | Enable | RW | 1 |
| 6 | SRCT6, SRCC6 | Output enable | Tristate | Enable | RW | 1 |
| 5 | SRCT5, SRCC5 | Output enable | Tristate | Enable | RW | 1 |
| 4 | SRCT4, SRCC4 | Output enable | Tristate | Enable | RW | 1 |
| 3 | SRCT3, SRCC3 | Output enable | Tristate | Enable | RW | 1 |
| 2 | SRCT2, SRCC2 | Output enable | Tristate | Enable | RW | 1 |
| 1 | SRCT1, SRCC1 | Output enable | Tristate | Enable | RW | 1 |
| 0 | SRCT0, SRCT0 | Output enable | Tristate | Enable | RW | 1 |

BYTE 1

| Bit | Output(s) Affected | Description/Function | 0 | 1 | Type | Power On |
|-----|--------------------|----------------------|----------|--------|------|----------|
| 7 | USB48 | Output enable | Tristate | Enable | RW | 1 |
| 6 | REF2 | Output enable | Tristate | Enable | RW | 1 |
| 5 | REF1 | Output enable | Tristate | Enable | RW | 1 |
| 4 | REF0 | Output enable | Tristate | Enable | RW | 1 |
| 3 | 24_48MHz | Output enable | Tristate | Enable | RW | 1 |
| 2 | CPUT1, CPUC1 | Output enable | Tristate | Enable | RW | 1 |
| 1 | CPUT0, CPUC0 | Output enable | Tristate | Enable | RW | 1 |
| 0 | HTT66 | Output enable | Tristate | Enable | RW | 1 |

BYTE 2

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|--------------------|------------------------|---|---|------|----------|
| 7 | Reserved | | | | RW | 1 |
| 6 | Reserved | | | | RW | 0 |
| 5 | PCI0 SEL1 | see PCI select table | | | RW | 0 |
| 4 | PCI0 SEL0 | | | | RW | 0 |
| 3 | Reserved | | | | RW | 0 |
| 2 | Reserved | | | | RW | 0 |
| 1 | Reserved | | | | RW | 0 |
| 0 | Reserved | | | | RW | 0 |

BYTE 3

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|--------------------|---------------------------------------|----------|----------|------|----------|
| 7 | SRC7 | Controlled by CLKREQB# or CLKREQA# | CLKREQ0# | CLKREQ1# | RW | 0 |
| 6 | SRC6 | | CLKREQ0# | CLKREQ1# | RW | 0 |
| 5 | SRC5 | | CLKREQ0# | CLKREQ1# | RW | 0 |
| 4 | SRC4 | | CLKREQ0# | CLKREQ1# | RW | 0 |
| 3 | SRC3 | | CLKREQ0# | CLKREQ1# | RW | 0 |
| 2 | Reserved | | | | RW | 0 |
| 1 | Reserved | | | | RW | 0 |
| 0 | SRC0 | Controlled by CLKREQB# or CLKREQA# | CLKREQ0# | CLKREQ1# | RW | 0 |

BYTE 4

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|--------------------|--|----------------|------------|------|----------|
| 7 | SRC7 | When CLKREQ is HIGH, Output is Hi-Z | Not Controlled | Controlled | RW | 0 |
| 6 | SRC6 | | Not Controlled | Controlled | RW | 0 |
| 5 | SRC5 | | Not Controlled | Controlled | RW | 0 |
| 4 | SRC4 | | Not Controlled | Controlled | RW | 0 |
| 3 | SRC3 | | Not Controlled | Controlled | RW | 0 |
| 2 | Reserved | | | | RW | 0 |
| 1 | Reserved | | | | RW | 0 |
| 0 | SRC0 | When CLKREQ is HIGH, Output is Hi-Z | Not Controlled | Controlled | RW | 0 |

BYTE 5

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|--------------------|-----------------------------|---|---|------|----------|
| 7 | HTT66 | HTT66 strength selection | | | RW | 1 |
| 6 | HTT66 | | | | RW | 0 |
| 5 | PCIStrC1 | PCI strength selection | | | RW | 1 |
| 4 | PCIStrC0 | | | | RW | 0 |
| 3 | REFStr1 | REF strength selection | | | RW | 1 |
| 2 | REFStr0 | | | | RW | 0 |
| 1 | 48MHStr1 | USB48MHz strength selection | | | RW | 1 |
| 0 | 48MHzStr0 | | | | RW | 0 |

BYTE 6

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|---------------------|---|---|---|------|----------|
| 7 | Reserve | | | | RW | 0 |
| 6 | SRC0, SR[7:3], SMC2 | SRC0, SRC[7:3] SSC control (see SMC table) | | | RW | 0 |
| 5 | SRC0, SR[7:3], SMC1 | | | | RW | 0 |
| 4 | SRC0, SR[7:3], SMC0 | | | | RW | 0 |
| 3 | Reserved | | | | RW | 0 |
| 2 | SRC[2:1], SMC2 | SRC[2:1] control (see SMC table) | | | RW | 0 |
| 1 | SRC[2:1], SMC1 | | | | RW | 0 |
| 0 | SRC[2:1], SMC0 | | | | RW | 0 |

BYTE 7

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|--------------------|------------------------|---|---|------|----------|
| 7 | | Revision ID | | | R | 0 |
| 6 | | Revision ID | | | R | 0 |
| 5 | | Revision ID | | | R | 0 |
| 4 | | Revision ID | | | R | 0 |
| 3 | | Vendor ID | | | R | 0 |
| 2 | | Vendor ID | | | R | 1 |
| 1 | | Vendor ID | | | R | 0 |
| 0 | | Vendor ID | | | R | 1 |

BYTE 8 (INDEX BLOCK READ BYTE COUNT)

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|--------------------|------------------------|---|---|------|----------|
| 7 | | | | | RW | 0 |
| 6 | | | | | RW | 0 |
| 5 | | | | | RW | 0 |
| 4 | | | | | RW | 1 |
| 3 | | | | | RW | 0 |
| 2 | | | | | RW | 1 |
| 1 | | | | | RW | 1 |
| 0 | | | | | RW | 0 |

BYTE 9

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|--------------------|--|---|---|------|----------|
| 7 | Reserved | | | | RW | 0 |
| 6 | Reserved | | | | RW | 0 |
| 5 | Reserved | | | | RW | 0 |
| 4 | Reserved | | | | RW | 0 |
| 3 | Reserved | | | | RW | 0 |
| 2 | CPU_SMC2 | CPU PLL SSC control (see SMC table) | | | RW | 0 |
| 1 | CPU_SMC1 | | | | RW | 0 |
| 0 | CPU_SMC0 | | | | RW | 0 |

BYTE 10

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|--------------------|---|---|---|------|----------|
| 7 | WD_1_Timer7 | WatchDog_1_Alarm timer Default is 11*290ms | | | RW | 0 |
| 6 | WD_1_Timer6 | | | | RW | 0 |
| 5 | WD_1_Timer5 | | | | RW | 0 |
| 4 | WD_1_Timer4 | | | | RW | 0 |
| 3 | WD_1_Timer3 | | | | RW | 1 |
| 2 | WD_1_Timer2 | | | | RW | 0 |
| 1 | WD_1_Timer1 | | | | RW | 1 |
| 0 | WD_1_Timer0 | | | | RW | 1 |

BYTE 11

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|-----------------------|---|---------|--------------|------|----------|
| 7 | CPU_N8 | | | | RW | 0 |
| 6 | Reserved | | | | RW | 0 |
| 5 | Reserved | | | | RW | 0 |
| 4 | Reserved | | | | RW | 0 |
| 3 | WDRB | Alarm read back, reset by WD disable | | Alarm | R | 0 |
| 2 | RESET# ⁽¹⁾ | Reset Enable | Disable | Reset Enable | RW | 0 |
| 1 | Reserved | | | | RW | 0 |
| 0 | Watch Dog Enable | Watch Dog Enable | Disable | Enable | RW | 0 |

BYTE 12

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|--------------------|---|---|---|------|----------|
| 7 | CPU_N7 | CPU CLK = N*Resolution Resolution = 1.3333 | | | RW | 1 |
| 6 | CPU_N6 | | | | RW | 0 |
| 5 | CPU_N5 | | | | RW | 0 |
| 4 | CPU_N4 | | | | RW | 1 |
| 3 | CPU_N3 | | | | RW | 0 |
| 2 | CPU_N2 | | | | RW | 1 |
| 1 | CPU_N1 | | | | RW | 1 |
| 0 | CPU_N0, LSB | | | | RW | 0 |

BYTE 13

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|--------------------|--|---|---|------|----------|
| 7 | SRC1_N7, MSB | SRC2, SRC1 SRC CLK = N*Resolution Resolution = 0.66667 | | | RW | 1 |
| 6 | SRC1_N6 | | | | RW | 0 |
| 5 | SRC1_N5 | | | | RW | 0 |
| 4 | SRC1_N4 | | | | RW | 1 |
| 3 | SRC1_N3 | | | | RW | 0 |
| 2 | SRC1_N2 | | | | RW | 1 |
| 1 | SRC1_N1 | | | | RW | 1 |
| 0 | SRC1_N0, LSB | | | | RW | 0 |

BYTE 14

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|--------------------|--|---|---|------|----------|
| 7 | SRC0_N7, MSB | SRC[7:3], SRC0 SRC CLK = N*Resolution Resolution = 0.66667 | | | RW | 1 |
| 6 | SRC0_N6 | | | | RW | 0 |
| 5 | SRC0_N5 | | | | RW | 0 |
| 4 | SRC0_N4 | | | | RW | 1 |
| 3 | SRC0_N3 | | | | RW | 0 |
| 2 | SRC0_N2 | | | | RW | 1 |
| 1 | SRC0_N1 | | | | RW | 1 |
| 0 | SRC0_N0, LSB | | | | RW | 0 |

BYTE 15

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|-------------------------------------|------------------------|-------------|------------|------|----------|
| 7 | | | Disable | Enable | RW | 0 |
| 6 | CPU N programming enable | | Disable | Enable | RW | 0 |
| 5 | SRC1, SRC2 N Programming enable | | Disable | Enable | RW | 0 |
| 4 | SRC0, SRC[7:3] N Programming enable | | Disable | Enable | RW | 0 |
| 3 | Turbo1 enable | | Disable | Enable | RW | 0 |
| 2 | Turbo | Turbo Active Selection | Active HIGH | Active LOW | RW | 0 |
| 1 | Reserved | | | | RW | 0 |
| 0 | T1CN8 | | | | RW | 0 |

BYTE 16

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|--------------------|---|---|---|------|----------|
| 7 | T1CN7 | Turbo1 CPU PLL N setting CLK = N*Resolution Resolution = 1.3333 | | | RW | 1 |
| 6 | T1CN6 | | | | RW | 0 |
| 5 | T1CN5 | | | | RW | 0 |
| 4 | T1CN4 | | | | RW | 1 |
| 3 | T1CN3 | | | | RW | 0 |
| 2 | T1CN2 | | | | RW | 1 |
| 1 | T1CN1 | | | | RW | 1 |
| 0 | T1CN0 | | | | RW | 0 |

BYTE 17

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|--------------------|--|---|---|------|----------|
| 7 | TSRC1_N7, MSB | Turbo1 SRC2, SRC1 SRC CLK = N*Resolution Resolution = 0.66667 | | | RW | 1 |
| 6 | TSRC1_N6 | | | | RW | 0 |
| 5 | TSRC1_N5 | | | | RW | 0 |
| 4 | TSRC1_N4 | | | | RW | 1 |
| 3 | TSRC1_N3 | | | | RW | 0 |
| 2 | TSRC1_N2 | | | | RW | 1 |
| 1 | TSRC1_N1 | | | | RW | 1 |
| 0 | TSRC1_N0, LSB | | | | RW | 0 |

BYTE 18 (RESERVED FOR USER)

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|--------------------|------------------------|---|---|------|----------|
| 7 | | | | | RW | 0 |
| 6 | | | | | RW | 0 |
| 5 | | | | | RW | 0 |
| 4 | | | | | RW | 0 |
| 3 | | | | | RW | 0 |
| 2 | | | | | RW | 0 |
| 1 | | | | | RW | 0 |
| 0 | | | | | RW | 0 |

BYTE 19 (RESERVED FOR USER)

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|--------------------|------------------------|---|---|------|----------|
| 7 | | | | | RW | 0 |
| 6 | | | | | RW | 0 |
| 5 | | | | | RW | 0 |
| 4 | | | | | RW | 0 |
| 3 | | | | | RW | 0 |
| 2 | | | | | RW | 0 |
| 1 | | | | | RW | 0 |
| 0 | | | | | RW | 0 |

BYTE 20 (RESERVED FOR USER)

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|--------------------|------------------------|---|---|------|----------|
| 7 | | | | | RW | 0 |
| 6 | | | | | RW | 0 |
| 5 | | | | | RW | 0 |
| 4 | | | | | RW | 0 |
| 3 | | | | | RW | 0 |
| 2 | | | | | RW | 0 |
| 1 | | | | | RW | 0 |
| 0 | | | | | RW | 0 |

BYTE 21

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|--------------------|--------------------------|--------|--|------|----------|
| 7 | Reserved | | | | RW | 0 |
| 6 | Reserved | | | | RW | 0 |
| 5 | Reserved | | | | RW | 0 |
| 4 | Reserved | | | | RW | 0 |
| 3 | Reserved | | | | RW | 0 |
| 2 | Reserved | | | | RW | 0 |
| 1 | Test_scl | On chip test mode enable | Normal | SCLK = 1, CLK outputs = 1 SCLK = 0, CLK outputs = 0 | RW | 0 |
| 0 | Test_hiz | CLK outputs enable | Normal | CLK outputs = Tristate | RW | 0 |

BYTE 62 = 70h

BYTE 63 = 13h

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Description | Min | Max | Unit |
|------------------|--|------|------|------|
| V _{DDA} | 3.3V Core Supply Voltage | | 4.6 | V |
| V _{DD} | 3.3V I/O Supply Voltage | | 4.6 | V |
| V _{IH} | 3.3V Input HIGH | | 4.6 | V |
| V _{IL} | 3.3V Input LOW | -0.5 | | V |
| T _s | Storage Temperature | -65 | +150 | °C |
| ESD Prot | Input ESD Protection Human Body Model | 2000 | | V |

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS - INPUT / SUPPLY / COMMON OUTPUT PARAMETERS

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, Supply Voltage: $V_{DD} = 3.3\text{V} \pm 5\%$

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---------------|--------------------------------------|---|----------------|----------|----------------|---------------|
| V_{IH} | Input HIGH Voltage | $3.3\text{V} \pm 5\%$ | 2 | — | $V_{DD} + 0.3$ | V |
| V_{IL} | Input LOW Voltage | $3.3\text{V} \pm 5\%$ | $V_{SS} - 0.3$ | — | 0.8 | V |
| V_{IH_FS} | 3.3V Input HIGH Voltage | V_{DD} | 0.7 | — | $V_{DD} + 0.3$ | V |
| V_{IL_FS} | 3.3V Input LOW Voltage | | $V_{SS} - 0.3$ | — | 0.35 | V |
| I_{IH} | Input HIGH Current | $V_{IN} = V_{DD}$ | -5 | — | 5 | μA |
| I_{IL1} | Input LOW Current | $V_{IN} = 0\text{V}$, inputs with no pull-up resistors | -5 | — | — | μA |
| I_{IL2} | Input LOW Current | $V_{IN} = 0\text{V}$, inputs with pull-up resistors | -200 | — | — | μA |
| $I_{DD3.3OP}$ | Operating Supply Current | Full active, $C_L = \text{full load}$ | — | — | 400 | mA |
| F_I | Input Frequency ⁽¹⁾ | $V_{DD} = 3.3\text{V}$ | — | 14.31818 | — | MHz |
| L_{PIN} | Pin Inductance ⁽²⁾ | | — | — | 7 | nH |
| C_{IN} | Input Capacitance ⁽²⁾ | Logic inputs | — | — | 5 | pF |
| C_{OUT} | | Output pin capacitance | — | — | 6 | |
| C_{INX} | | X1 and X2 pins | — | — | 5 | |
| T_{STAB} | Clock Stabilization ^(2,3) | From V_{DD} power-up | — | — | 1.8 | ms |
| | Modulation Frequency ⁽²⁾ | Triangular modulation | 30 | — | 33 | KHz |

NOTES:

1. Input frequency should be measured at the REF output pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.
2. This parameter is guaranteed by design, but not 100% production tested.
3. See TIMING DIAGRAMS for timing requirements.

ELECTRICAL CHARACTERISTICS - SRC 0.7 CURRENT MODE DIFFERENTIAL PAIR

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, Supply Voltage: $V_{DD} = 3.3\text{V} \pm 5\%$; $C_L = 2\text{pF}$

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|-------------|--|---|-------|------|--------|----------|
| Zo | Current Source Output Impedance ⁽¹⁾ | $V_O = V_X$ | 3000 | — | — | Ω |
| VOH3 | Output HIGH Voltage | $I_{OH} = -1\text{mA}$ | 2.4 | — | — | V |
| VOL3 | Output LOW Voltage | $I_{OL} = 1\text{mA}$ | — | — | 0.4 | V |
| VHIGH | Voltage HIGH ⁽¹⁾ | Statistical measurement on single-ended signal using oscilloscope math function | 660 | — | 1150 | mV |
| VLOW | Voltage LOW ⁽¹⁾ | | -300 | — | 150 | |
| VOVS | Max Voltage ⁽¹⁾ | Measurement on single-ended signal using absolute value | — | — | 1150 | mV |
| VUDS | Min Voltage ⁽¹⁾ | | -300 | — | — | |
| VCROSS(ABS) | Crossing Voltage (abs) ⁽¹⁾ | | 250 | — | 550 | mV |
| d - VCROSS | Crossing Voltage (var) ⁽¹⁾ | Variation of crossing over all edges | — | — | 140 | mV |
| ppm | Long Accuracy ^(1,2) | See TPERIOD Min. - Max. values | -300 | — | 300 | ppm |
| TPERIOD | Average Period ⁽²⁾ | 100MHz nominal | 9.997 | — | 10.003 | ns |
| TABSMIN | Absolute Min Period ^(1,2) | 100MHz nominal | 9.912 | — | — | ns |
| tr | Rise Time ⁽¹⁾ | $V_{OL} = 0.175\text{V}$, $V_{OH} = 0.525\text{V}$ | 175 | — | 700 | ps |
| tf | Fall Time ⁽¹⁾ | $V_{OL} = 0.175\text{V}$, $V_{OH} = 0.525\text{V}$ | 175 | — | 700 | ps |
| d-tr | Rise Time Variation ⁽¹⁾ | | — | — | 125 | ps |
| d-tf | Fall Time Variation ⁽¹⁾ | | — | — | 125 | ps |
| dt3 | Duty Cycle ⁽¹⁾ | Measurement from differential waveform | 45 | — | 55 | % |
| tcyc-cyc | Jitter, Cycle to Cycle ⁽¹⁾ | Measurement from differential waveform | — | — | 125 | ps |
| SKEW | Pin-to-Pin Skew ⁽¹⁾ | $V_T = 50\%$ | — | — | 250 | ps |
| | Tsu_SRC ^(1,3) | SRC STOP response to CLKREQ# | — | — | 60 | ns |
| | Tdrive_SRC ^(1,3) | SRC START response to CLKREQ# | — | — | 60 | ns |

NOTES:

1. This parameter is guaranteed by design, but not 100% production tested.
2. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.
3. See TIMING DIAGRAMS for timing requirements.

ELECTRICAL CHARACTERISTICS - CPU DIFFERENTIAL PAIR (SSC ENABLE AND DISABLE)

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, Supply Voltage: $V_{DD} = 3.3\text{V} \pm 5\%$; $C_L = 2\text{pF}$

| Symbol | Parameter ⁽¹⁾ | Test Conditions | Min. | Typ. | Max. | Unit |
|-------------------|---------------------------------------|-------------------------------------|--------|------|--------|----------|
| t_r | Rise Edge Rate | | 2 | — | 10 | V/ns |
| t_f | Fall Edge Rate | | 2 | — | 10 | V/ns |
| V_{DIFF} | Differential Voltage (single end) | | 0.4 | 1.25 | 2.3 | V |
| ΔV_{DIFF} | Change in V_{DIFF_DC} Magnitude | | -150 | — | +150 | mV |
| V_{CM} | Common Mode Voltage | | 1.05 | 1.25 | 1.45 | V |
| ΔV_{CM} | Change in Common Mode Voltage | | -200 | — | +200 | mV |
| $t_{CCJITTER}$ | Jitter, Cycle to Cycle | | — | — | 200 | ps |
| t_{JA} | Jitter Accumulated | | -1000 | — | +1000 | ps |
| t_{FS} | Frequency Stabilization from Power-Up | | — | — | 3 | ms |
| R_{ON} | Output Impedance | | 15 | 35 | 55 | Ω |
| Duty Cycle | Duty Cycle | | 47 | 50 | 53 | % |
| ppm | Long Accuracy ⁽²⁾ | See T_{PERIOD} Min. - Max. values | -300 | — | +300 | ppm |
| T_{PERIOD} | Average Period ⁽²⁾ | 200MHz nominal | 4.9985 | — | 5.0015 | ns |
| | | 250MHz nominal | 3.9988 | — | 4.0012 | |

NOTES:

- Parameters guaranteed by design, but not 100% production tested.
- All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

ELECTRICAL CHARACTERISTICS - PCICLK / PCICLK_F, HTT66

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = 0°C to +70°C, Supply Voltage: VDD = 3.3V ± 5%; CL = 10 - 30pF

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|----------|---------------------------------------|--------------------------------|--------|------|---------|------|
| ppm | Long Accuracy ^(1,2) | See Tperiod Min. - Max. values | — | — | 300 | ppm |
| TPERIOD | Clock Period ⁽²⁾ | 33.33MHz output nominal | 29.991 | — | 30.009 | ns |
| | | 33.33MHz output spread | 29.991 | — | 30.1598 | |
| VOH | Output HIGH Voltage | IOH = -1mA | 2.4 | — | — | V |
| VOL | Output LOW Voltage | IOL = 1mA | — | — | 0.55 | V |
| IOH | Output HIGH Current | VOH at Min. = 1V | -33 | — | — | mA |
| | | VOH at Max. = 3.135V | — | — | -33 | |
| IOL | Output LOW Current | VOL at Min. = 1.95V | 30 | — | — | mA |
| | | VOL at Max. = 0.4V | — | — | 38 | |
| | Edge Rate ⁽¹⁾ | Rising edge rate | 1 | — | 4 | V/ns |
| | Edge Rate ⁽¹⁾ | Falling edge rate | 1 | — | 4 | V/ns |
| tr1 | Rise Time ⁽¹⁾ | VOL = 0.8V, VOH = 2V | 0.3 | — | 1.2 | ns |
| tf1 | Fall Time ⁽¹⁾ | VOL = 0.8V, VOH = 2V | 0.3 | — | 1.2 | ns |
| dT1 | Duty Cycle ⁽¹⁾ | VT = 1.5V | 45 | — | 55 | % |
| tCYC-CYC | Jitter, Cycle to Cycle ⁽¹⁾ | VT = 1.5V | — | — | 500 | ps |

NOTES:

1. This parameter is guaranteed by design, but not 100% production tested.
2. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

ELECTRICAL CHARACTERISTICS - 24_48MHZ, 48MHZ, USB

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = 0°C to +70°C, Supply Voltage: VDD = 3.3V ± 5%; CL = 10 - 20pF

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|----------|---------------------------------------|--------------------------------|---------|------|--------|------|
| ppm | Long Accuracy ^(1,2) | See Tperiod Min. - Max. values | — | — | 300 | ppm |
| TPERIOD | Clock Period ⁽²⁾ | 48MHz output nominal | 20.8257 | — | 20.834 | ns |
| VOH | Output HIGH Voltage | IOH = -1mA | 2.4 | — | — | V |
| VOL | Output LOW Voltage | IOL = 1mA | — | — | 0.55 | V |
| IOH | Output HIGH Current | VOH at Min. = 1V | -29 | — | — | mA |
| | | VOH at Max. = 3.135V | — | — | -23 | |
| IOL | Output LOW Current | VOL at Min. = 1.95V | 29 | — | — | mA |
| | | VOL at Max. = 0.4V | — | — | 27 | |
| | Edge Rate ⁽¹⁾ | Rising edge rate | 1 | — | 2 | V/ns |
| | Edge Rate ⁽¹⁾ | Falling edge rate | 1 | — | 2 | V/ns |
| tr1 | Rise Time ⁽¹⁾ | VOL = 0.8V, VOH = 2V | 0.5 | — | 1.2 | ns |
| tf1 | Fall Time ⁽¹⁾ | VOL = 0.8V, VOH = 2V | 0.5 | — | 1.2 | ns |
| dT1 | Duty Cycle ⁽¹⁾ | VT = 1.5V | 45 | — | 55 | % |
| tCYC-CYC | Jitter, Cycle to Cycle ⁽¹⁾ | VT = 1.5V | — | — | 350 | ps |

NOTES:

1. This parameter is guaranteed by design, but not 100% production tested.
2. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

ELECTRICAL CHARACTERISTICS - REF-14.318MHZ

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, Supply Voltage: $V_{DD} = 3.3\text{V} \pm 5\%$; $C_L = 10 - 20\text{pF}$

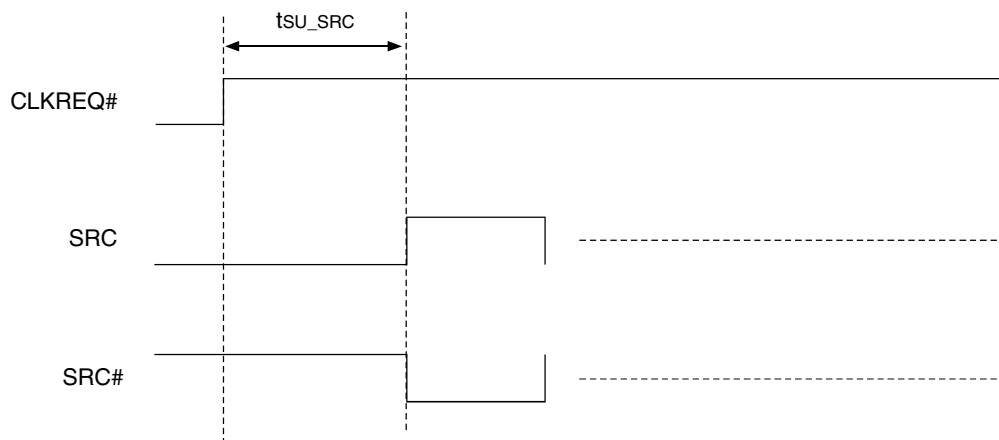
| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|----------|---------------------------------------|---|--------|------|--------|------|
| ppm | Long Accuracy ⁽¹⁾ | See Tperiod Min. - Max. values | — | — | 0 | ppm |
| TPERIOD | Clock Period | 14.318MHz output nominal | 69.827 | — | 69.855 | ns |
| VOH | Output HIGH Voltage ⁽¹⁾ | $I_{OH} = -1\text{mA}$ | 2.4 | — | — | V |
| VOL | Output LOW Voltage ⁽¹⁾ | $I_{OL} = 1\text{mA}$ | — | — | 0.4 | V |
| IOH | Output HIGH Current | V_{OH} at Min. = 1V | -33 | — | — | mA |
| | | V_{OH} at Max. = 3.135V | — | — | -33 | |
| IOL | Output LOW Current | V_{OL} at Min. = 1.95V | 30 | — | — | mA |
| | | V_{OL} at Max. = 0.4V | — | — | 38 | |
| | Edge Rate ⁽¹⁾ | Rising edge rate | 1 | — | 4 | V/ns |
| | Edge Rate ⁽¹⁾ | Falling edge rate | 1 | — | 4 | V/ns |
| t_{R1} | Rise Time ⁽¹⁾ | $V_{OL} = 0.8\text{V}$, $V_{OH} = 2\text{V}$ | 0.3 | — | 1.2 | ns |
| t_{F1} | Fall Time ⁽¹⁾ | $V_{OL} = 0.8\text{V}$, $V_{OH} = 2\text{V}$ | 0.3 | — | 1.2 | ns |
| dT1 | Duty Cycle ⁽¹⁾ | $V_T = 1.5\text{V}$ | 45 | — | 55 | % |
| lcyc-cyc | Jitter, Cycle to Cycle ⁽¹⁾ | $V_T = 1.5\text{V}$ | — | — | 1000 | ps |

NOTE:

1. This parameter is guaranteed by design, but not 100% production tested.

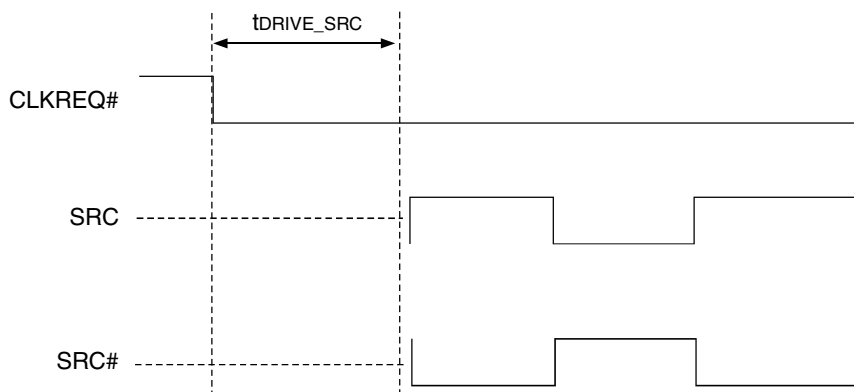
CLKREQ# ASSERTION

The clock samples the CLKREQ# signal on a rising edge of SRC clock. After detecting the CLKREQ# assertion low, all controlled SRC clocks will be tristate on their next high to low transition.

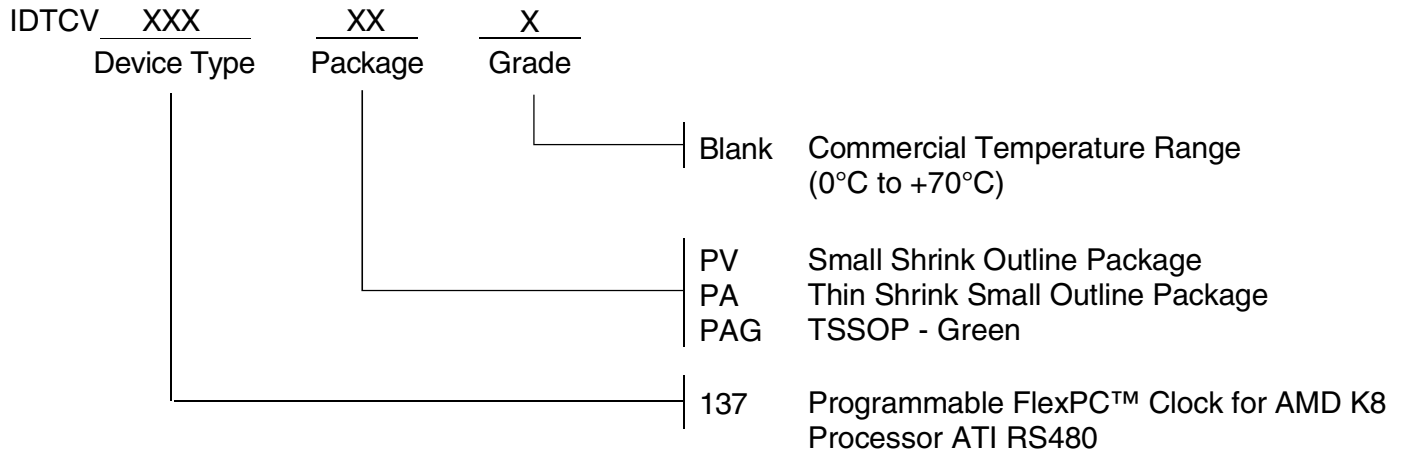


CLKREQ# - DE-ASSERTION

The de-assertion of the CLKREQ# signal is to be sampled on the rising edge of the SRC free running clock domain. After detecting CLKREQ# de-assertion, all controlled SRC clocks will resume in a glitch free manner.



ORDERING INFORMATION



IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.