

Features

512Kx32 bit CMOS Static

Random Access Memory

- Fast Access Times: 20*, 25, 35, 45 and 55ns
- Data Retention Functionality (LP Version)
- Individual Byte Selects (x8, x16, x32)
- Output Enable Function
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

66 Lead PGA, No. 334

- Multiple Ground Pins for Maximum Noise Immunity

Single +5V (±10%) Supply Operation

* Advanced Information

512Kx32 CMOS, High Speed Static RAM

The EDI8M32512CA, a high speed, high performance, 16 megabit density Static RAM organized as 512Kx32 bits, contains four 512Kx8 SRAMs.

Four Chip Enables are provided to independently enable each of the four bytes. Reading or writing can be executed on an individual byte or any combination of bytes through proper use of the chip and write enables.

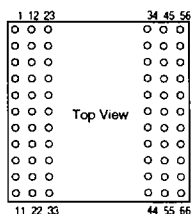
Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation and providing equal access and cycle times for ease of use.

The EDI8M32512CA is offered in 66 lead PGA. The EDI8M32512CA is a pin for pin upgrade of the EDI8C32128C. Pins 8 and 28 which are no connects on the EDI8C32128C become A17 and A18 respectively on the EDI8M32512CA.

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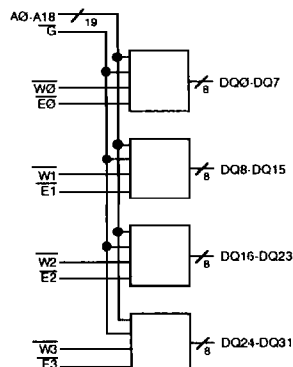
Pin Configurations and Block Diagram

Pin No./Name	Pin No./Name	Pin No./Name	Pin No./Name	Pin No./Name	Pin No./Name
1 D08	12 $\overline{W1}$	23 DQ15	34 DQ24	45 VCC	56 DQ31
2 D09	13 E1	24 DQ14	35 DQ25	46 $\overline{E3}$	57 DQ30
3 DQ10	14 VSS	25 DQ13	36 DQ26	47 $\overline{W3}$	58 DQ29
4 A13	15 DQ11	26 DQ12	37 A6	48 DQ27	59 DQ28
5 A14	16 A10	27 \overline{G}	38 A7	49 A3	60 A0
6 A15	17 A11	28 A18	39 NC	50 A4	61 A1
7 A16	18 A12	29 $\overline{W0}$	40 A8	51 A5	62 A2
8 A17	19 VCC	30 DQ7	41 A9	52 $\overline{W2}$	63 DQ23
9 DQ0	20 E0	31 DQ6	42 DQ16	53 E2	64 DQ22
10 DQ1	21 NC	32 DQ5	43 DQ17	54 VSS	65 DQ21
11 DQ2	22 DQ3	33 DQ4	44 DQ18	55 DQ19	66 DQ20



Pin Names

- A0-A18 Address Inputs
- $\overline{E0-E3}$ Chip Enables
- $\overline{W0-W3}$ Write Enables
- \overline{G} Output Enable
- DQ0-DQ31 Common Data Input/Output
- VCC Power (+5V±10%)
- VSS Ground
- NC No Connection



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Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Military	-55 °C to +125°C
Storage Temperature	-65°C to +150°C
Power Dissipation	4.5 Watts
Output Current	40 mA
Junction Temperature	175°C

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

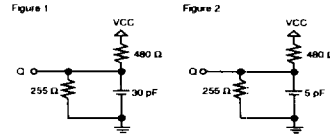
Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	VCC+0.5	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

(note: For TEHQZ.TGHQZ and TWLQZ, Figure 2)



DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Typ	Max	Units
Operating Power	ICC1	$\bar{W} = VIL, I/O = 0mA$	20ns*	775	900	mA
Supply Current – x32		(4) $\bar{E} = VIL$	25-55ns	630	800	mA
Operating Power	ICC1	$\bar{W} = VIL, I/O = 0mA$	20ns*	500	570	mA
Supply Current – x16		(2) $\bar{E} = VIL, (2) \bar{E} \geq VCC - 0.2V$	25-55ns	370	520	mA
Operating Power	ICC1	$\bar{W} = VIL, I/O = 0mA$	20ns*	300	400	mA
Supply Current – x8		(1) $\bar{E} = VIL, (3) \bar{E} \geq VCC - 0.2V$	25-55ns	250	370	mA
Standby (TTL) Power	ICC2	(All) $\bar{E} \geq VIH, VIL \geq VIN \geq VIH$		150	240	mA
Supply Current						
Full Standby Power	ICC3	(All) $\bar{E} \geq VCC - 0.2V$	C	25	40	mA
Supply Current		$VIN \geq VCC - 0.2V$ or $VIN \leq 0.2V$	LP	10	20	mA
Input Leakage Current	ILI	$VIN = 0V$ to VCC	--	--	±10	µA
Output Leakage Current	ILO	$V I/O = 0V$ to VCC	--	--	±10	µA
Output High Voltage	VOH	$I/OH = -4.0mA$		2.4		V
Output Low Voltage	VOL	$I/OL = 8.0mA$			0.45	V

* Advanced Information
Typical: TA=25°C, VCC=5.0V

Truth Table

\bar{G}	\bar{E}	\bar{W}	Mode	Output	Power
X	H	X	Standby	HIGH Z	ICC2, ICC3
H	L	H	Output Deselect	HIGH Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CI	50	pF
Data Lines	CD/Q	20	pF
Chip & Write Enable Lines	\bar{E}, \bar{W}	20	pF
Output Enable Line	\bar{G}	50	pF

These parameters are sampled, not 100% tested.

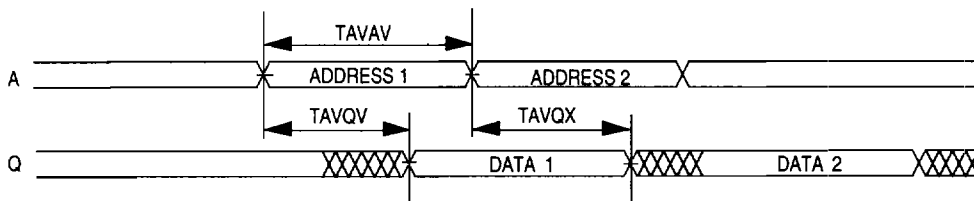
AC Characteristics Read Cycle

Parameter	Symbol	Alt	20ns*		25ns		35ns		45ns		55ns		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	TRC	20		25		35		45		55		ns
Address Access Time	TAVQV	TAA		20		25		35		45		55	ns
Chip Enable Access Time	TELQV	TACS		20		25		35		45		55	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		10		12		20		20		20	ns
Output Hold from Address Change	TAVQX	TOH		5		5		5		5		5	ns
Output Enable to Output Valid	TGLQV	TOE		10		12		20		25		30	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		0		0		ns
Output Disable to Output in High Z (1)	TGHQZ	TOHZ		8		10		20		20		20	ns
Chip Enable to Power Up	TELICCH	TPU	0		0		0		0		0		ns
Chip Enable to Power Down	TEHICCL	TPD		20		25		35		45		55	ns

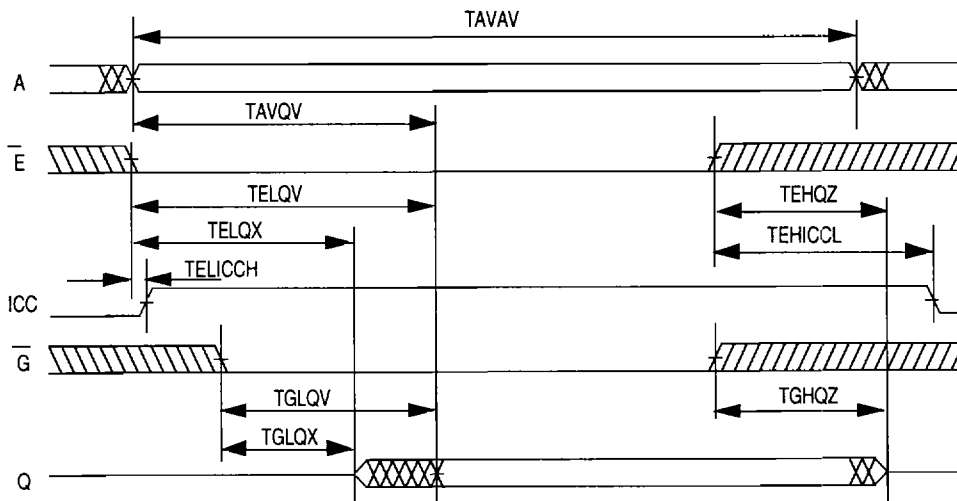
*Advanced Information

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1 - W High, G, E Low



Read Cycle 2 - W High



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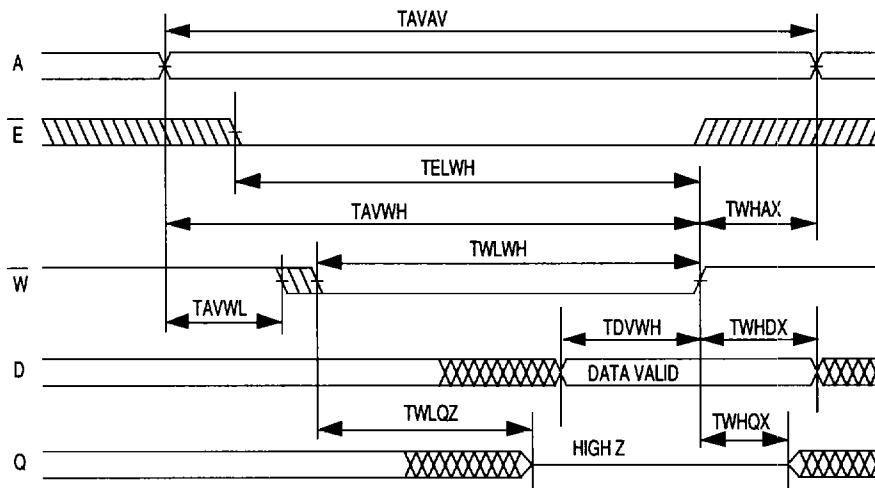
AC Characteristics Write Cycle

Parameter	Symbol	JEDEC Alt.	20ns*		25ns		35ns		45ns		55ns		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
Write Cycle Time	TAVAV	TWC	20	25	35	45	55					ns	
Chip Enable to End of Write	TELWH/TELEH	TCW	15	20	30	35	50					ns	
Address Setup Time	TAVWL/TAVEL	TAS	0	0	0	0	0					ns	
Address Valid to End of Write	TAVWH/TAVEH	TAW	15	20	30	35	50					ns	
Write Pulse Width	TWLWH/TWLEH	TWP	15	20	30	35	45					ns	
Write Recovery Time	TWHAX/TEHAX	TWR	0	0	0	0	0					ns	
Data Hold Time	TWHDX/TEHDX	TDH	0	0	0	0	0					ns	
Write to Output in High Z (1)	TWLQZ	TWHZ	0	8	0	10	0	15	0	20	0	25	ns
Data to Write Time	TDVWH/TDVEH	TDW	12	15	20	25	30					ns	
Output Active from End of Write (1)	TWHQX	TWLZ	3	3	3	3	3					ns	

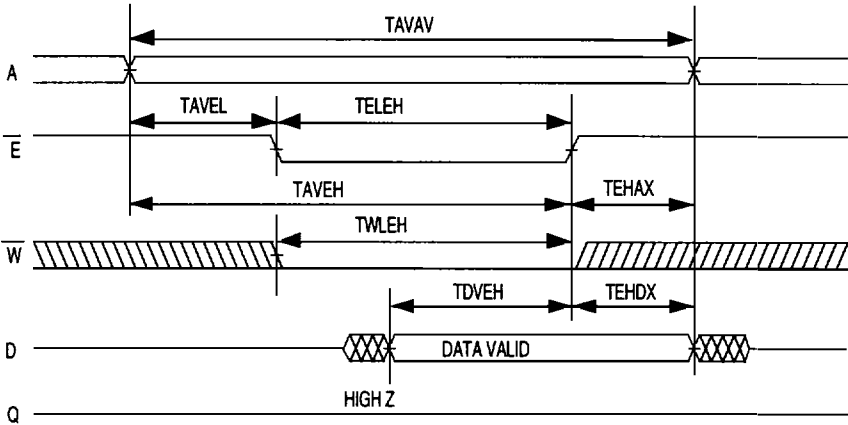
*Advanced Information

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1 - W Controlled



Write Cycle 2 - E Controlled



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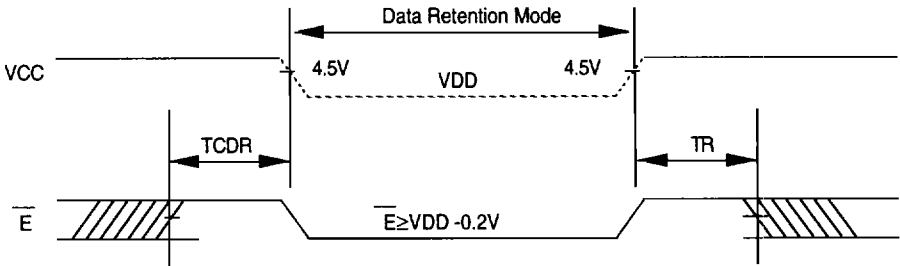
Data Retention Characteristics

EDI8M32512CA

Characteristic	Sym	Test Conditions	VDD	Min	Typ	Max	Unit
Data Retention Voltage	VDD	$\bar{E} \geq VDD - 0.2V$		2	-	-	V
Data Retention Quiescent Current	ICCDR		2V	-	-	8	mA
Chip Disable to Data Retention Time	TCDR	$V_{IN} \geq VDD - 0.2V$		0	-	-	ns
Operation Recovery Time	TR	or $V_{IN} \leq 0.2V$		TAVAV	-	-	ns

*Read Cycle Time

Data Retention E Controlled



Ordering Information

Mil-Temp-Only, Standard Power

Part No.	Speed ns	Package No.
ED18M32512CA20GM	20	334
ED18M32512CA25GM	25	334
ED18M32512CA35GM	35	334
ED18M32512CA45GM	45	334
ED18M32512CA55GM	55	334

Mil-Temp-Only, Low Power

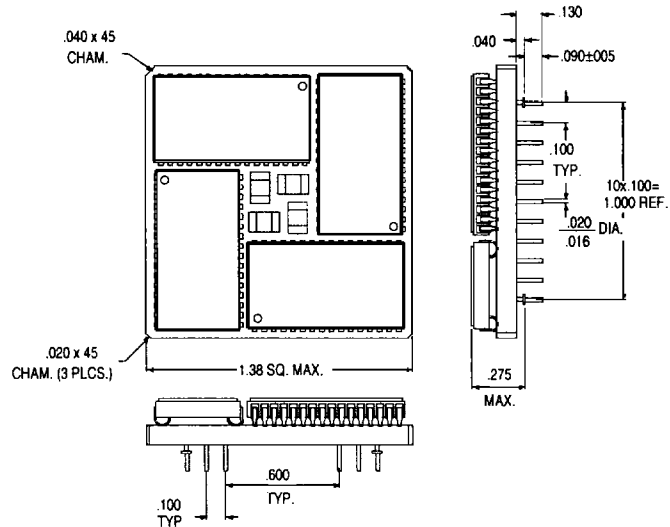
Part No.	Speed ns	Package No.
ED18M32512LPA20GM	20	334
ED18M32512LPA25GM	25	334
ED18M32512LPA35GM	35	334
ED18M32512LPA45GM	45	334
ED18M32512LPA55GM	55	334

Package Description

Package No. 334

66 Pin PGA

Weight = 18g



Mil-PRF-38535 Appendix A

Compliant CSOJs Standard Power

Part No.	Speed ns	Package No.
ED18M32512CA20GB	20	334
ED18M32512CA25GB	25	334
ED18M32512CA35GB	35	334
ED18M32512CA45GB	45	334
ED18M32512CA55GB	55	334

Mil-PRF-38535 Appendix A

Compliant CSOJs Low, Power

Part No.	Speed ns	Package No.
ED18M32512LPA20GB	20	334
ED18M32512LPA25GB	25	334
ED18M32512LPA35GB	35	334
ED18M32512LPA45GB	45	334
ED18M32512LPA55GB	55	334

Note: For Commercial or Industrial Temp grade product use C or I, respectively, to replace B in the suffix of the part number, e.g. ED18M32512LPA20GB becomes ED18M32512LPA20GI (Industrial Temp Range).

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