

## 74F273 Octal D Flip-Flop

### General Description

The 'F273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset (MR) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the MR input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

### Features

- Ideal buffer for MOS microprocessor or memory
- Eight edge-triggered D flip-flops
- Buffered common clock
- Buffered, asynchronous Master Reset
- See 'F377 for clock enable version
- See 'F373 for transparent latch version
- See 'F374 for 3-STATE version
- Guaranteed 4000V minimum ESD protection

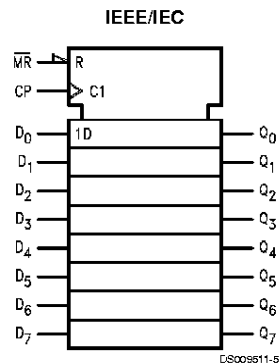
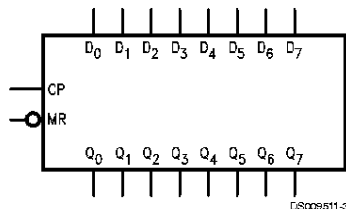
### Ordering Code:

Commercial	Military	Package Number	Package Description
74F273PC		N20A	20-Lead (0.300" Wide) Molded Dual-In-Line
	54F273DM (Note 2)	J20A	20-Lead Ceramic Dual-In-Line
74F273SC (Note 1)		M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F273SJ (Note 1)		M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F273FM (Note 2)	W20A	20-Lead Cerpack
	54F273LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

**Note 1:** Devices also available in 13" reel. Use suffix = SCX and SJX

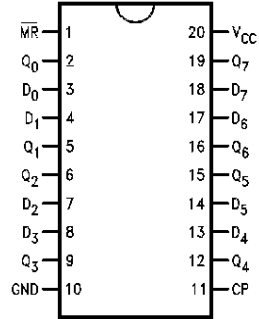
**Note 2:** Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB

### Logic Symbols



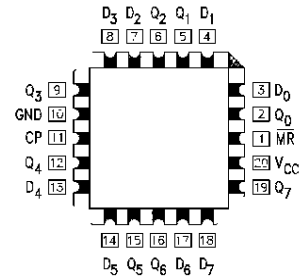
## Connection Diagrams

Pin Assignment for  
DIP, SOIC and Flatpak



CS00S11-1

Pin Assignment  
for LCC



CS00S11-2

## Unit Loading/Fan Out

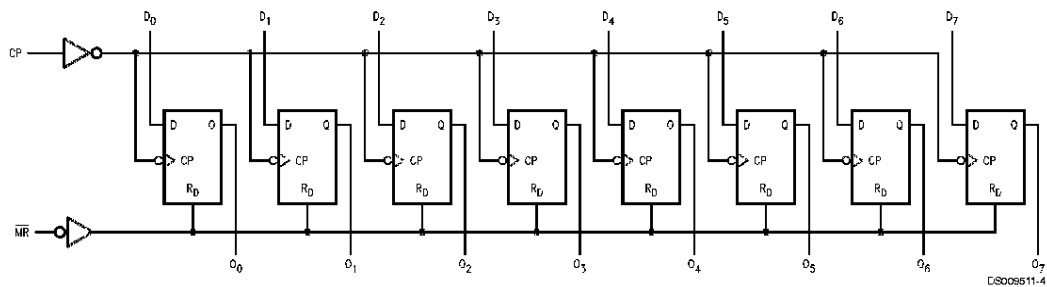
Pin Names	Description	54F74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
D <sub>0</sub> -D <sub>7</sub>	Data Inputs	1.0/1.0	20 $\mu$ A/-0.6 mA
MR	Master Reset (Active LOW)	1.0/1.0	20 $\mu$ A/-0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A/-0.6 mA
Q <sub>0</sub> -Q <sub>7</sub>	Data Outputs	50/33.3	-1 mA/20 mA

## Mode Select-Function Table

Operating Mode	Inputs			Output
	MR	CP	D <sub>n</sub>	Q <sub>n</sub>
Reset (Clear)	L	X	X	L
Load "1"	H	↗	h	H
Load "0"	H	↗	l	L

H = HIGH Voltage Level steady state  
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition  
L = LOW Voltage Level steady state  
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH clock transition  
X = Immaterial  
↗ = LOW-to-HIGH clock transition

## Logic Diagram



CS00S11-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays

## Absolute Maximum Ratings (Note 3)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 4)	-0.5V to +7.0V
Input Current (Note 4)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

ESD Last Passing Voltage (min)

4000V


## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**Note 3:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 4:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	Mil	2.5		V	Min	I <sub>OH</sub> = -1 mA
		10% V <sub>CC</sub>	2.5				
		5% V <sub>CC</sub>	2.7				
V <sub>OL</sub>	Output LOW Voltage	Mil		0.5	V	Min	I <sub>OL</sub> = 20 mA
		10% V <sub>CC</sub>		0.5			
		5% V <sub>CC</sub>		0.5			
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Breakdown Test Current	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All other pins grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>ID</sub> = 150 mV All other pins grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current			-60	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current			44	mA	Max	CP = 
I <sub>CCL</sub>				56			D <sub>n</sub> = $\overline{\text{MR}}$ = HIGH

## AC Electrical Characteristics

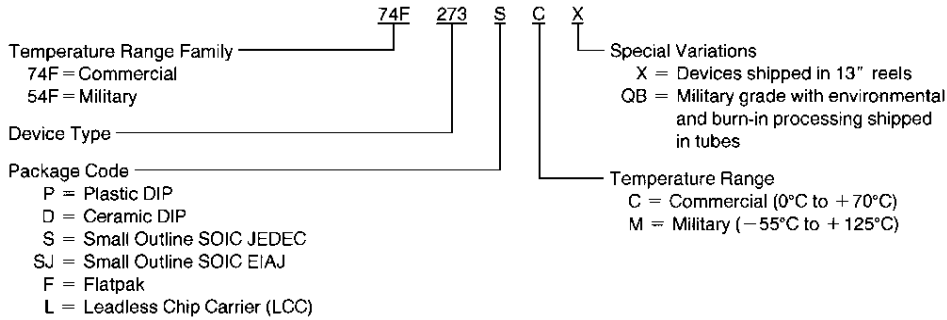
Symbol	Parameter	74F			54F		74F		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	Min	Max	
$f_{\text{max}}$	Maximum Clock Frequency	160			95		130		MHz
$t_{\text{PLH}}$	Propagation Delay	3.0		7.0	2.5	9.5	2.5	7.5	ns
$t_{\text{PHL}}$	Clock to Output	4.0		9.00	3.0	11.0	3.5	9.0	ns
$t_{\text{PLH}}$	Propagation Delay	4.5		9.5	3.0	11.0	4.0	10.0	ns
$t_{\text{PHL}}$	MR to Output								

## AC Operating Requirements

Symbol	Parameter	74F		54F		74F		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$		
		Min	Max	Min	Max	Min	Max	
$t_s(\text{H})$	Setup Time, HIGH or LOW	3.0		3.5		3.0		ns
$t_s(\text{L})$	Data to CP	3.5		4.0		3.5		
$t_h(\text{H})$	Hold Time, HIGH or LOW	0.5		1.0		0.5		ns
$t_h(\text{L})$	Data to CP	1.0		1.0		1.0		
$t_w(\text{L})$	MR Pulse Width, LOW	6.0		4.0		6.0		ns
$t_w(\text{H})$	CP Pulse Width	6.0		5.0		6.0		ns
$t_w(\text{L})$	HIGH or LOW	6.0		5.0		6.0		ns
$t_{\text{rec}}$	Recovery Time, MR to CP	3.0		4.5		3.5		ns

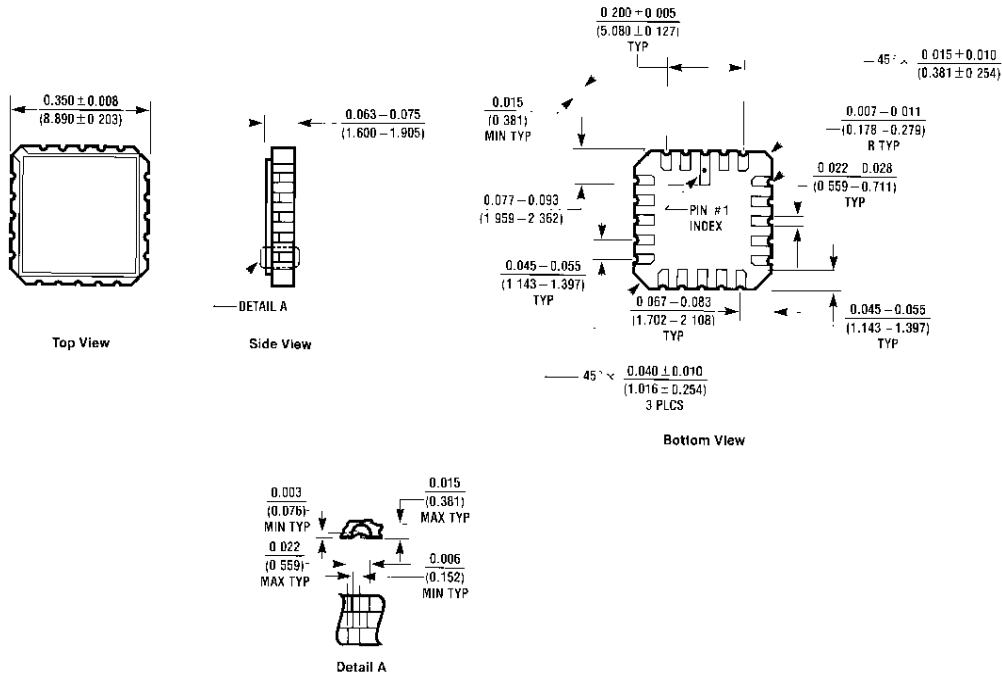
## Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:



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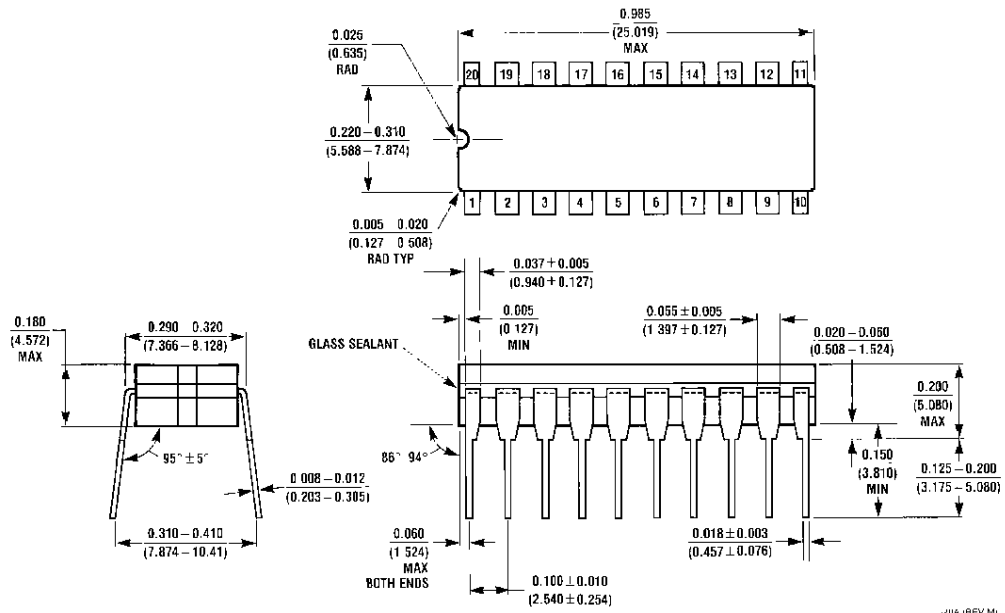
## Physical Dimensions inches (millimeters) unless otherwise noted



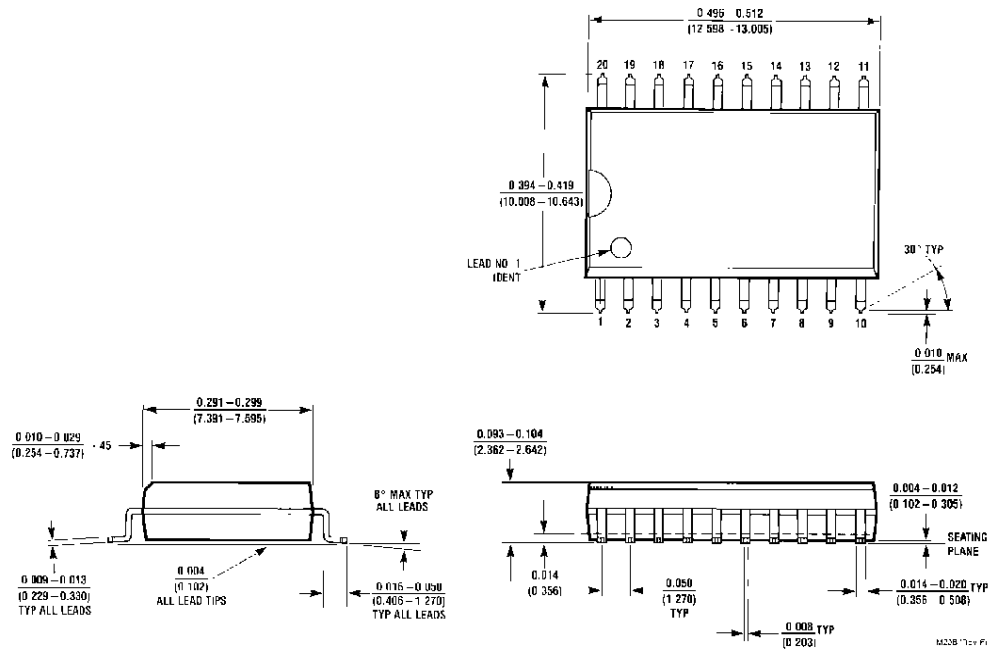
LS-00000-3

**20-Lead Ceramic Leadless Chip Carrier (LCC)  
Package Number E20A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

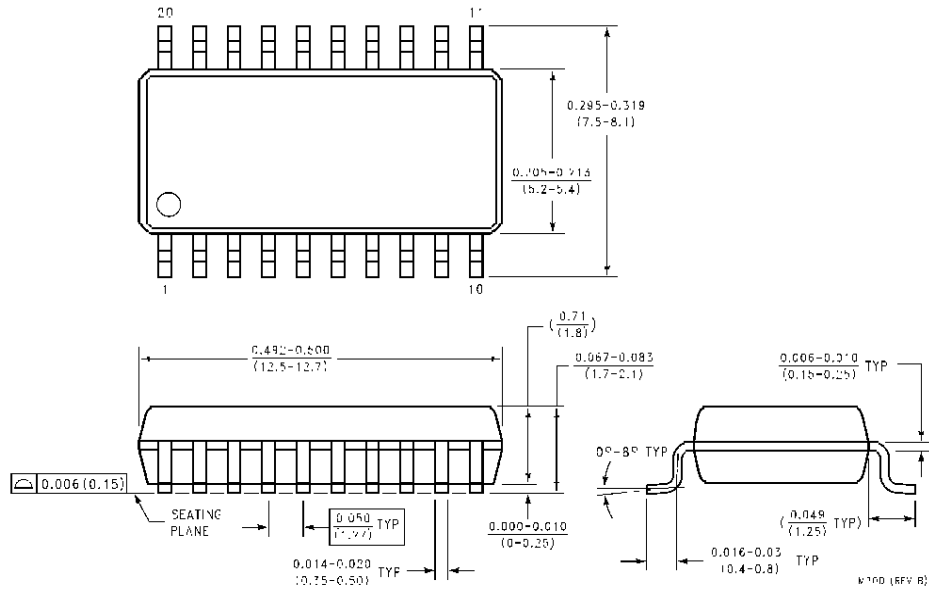


**20-Lead Ceramic Dual-In-Line Package (D)  
 Package Number J20A**

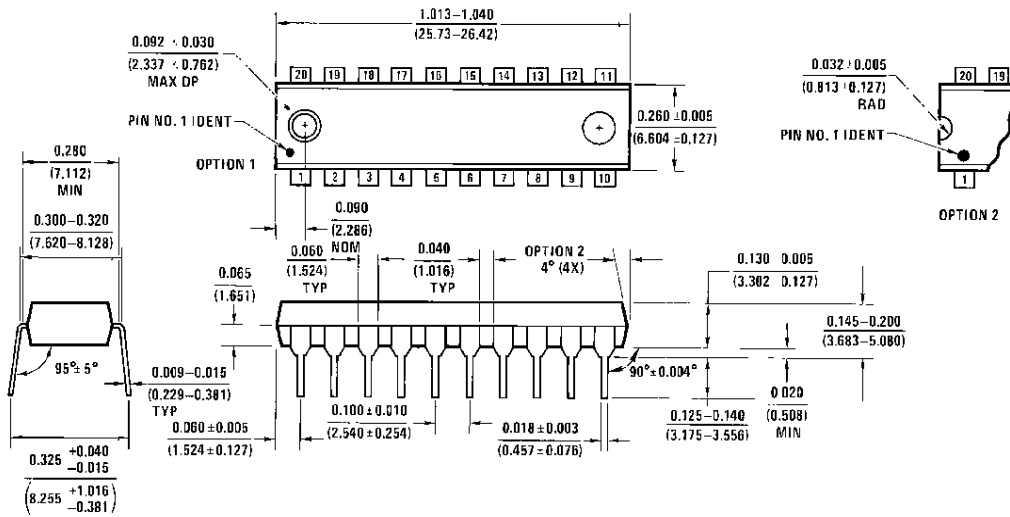


**20-Lead (0.300" Wide) Molded Small Outline Package, JEDEC (S)  
 Package Number M20B**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



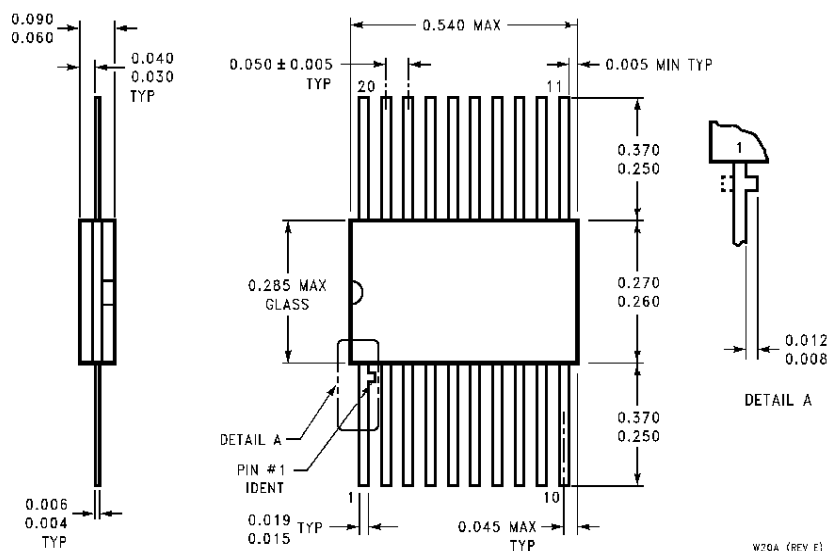
Lit. # 114645



**20-Lead (0.300" Wide) Molded Dual-In-Line Package (P)**  
**Package Number N20A**

N20A (REV G)

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**20-Lead Ceramic Flatpak (F)  
Package Number W20A**

W20A (REV E)

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