



**Military 10531**

# Dual D Type Master Slave Flip-Flop

**ELECTRICALLY TESTED PER:  
MIL-M-38510/06101**

The 10531 is a dual master-slave type D flip-flop. Asynchronous Set (S) and Reset (R) override Clock (C) and Clock Enable (CE) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

- 325 mW Max/Pkg (No Load)
- $f_{tog} = 125$  MHz typ
- $t_{pd} = 3.0$  ns typ
- $t_r, t_f = 2.5$  ns typ (20% - 80%)

**PIN ASSIGNMENTS**

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V <sub>CC1</sub>	1	5	2	GND
Q <sub>1</sub>	2	6	3	51 Ω TO V <sub>TT</sub>
$\overline{Q}_1$	3	7	4	51 Ω TO V <sub>TT</sub>
R <sub>1</sub>	4	8	5	51 Ω TO V <sub>TT</sub>
S <sub>1</sub>	5	9	7	GND
$\overline{CE}_1$	6	10	8	OPEN
D <sub>1</sub>	7	11	9	OPEN
V <sub>EE</sub>	8	12	10	V <sub>EE</sub>
C <sub>C</sub>	9	13	12	OPEN
D <sub>2</sub>	10	14	13	OPEN
$\overline{CE}_2$	11	15	14	OPEN
S <sub>2</sub>	12	16	15	GND
R <sub>2</sub>	13	1	17	51 Ω TO V <sub>TT</sub>
$\overline{Q}_2$	14	2	18	51 Ω TO V <sub>TT</sub>
Q <sub>2</sub>	15	3	19	51 Ω TO V <sub>TT</sub>
V <sub>CC2</sub>	16	4	20	GND

**BURN - IN CONDITIONS:**

V<sub>TT</sub> = - 2.0 V MAX / - 2.2 V MIN

V<sub>EE</sub> = - 5.7 V MAX / - 5.2 V MIN

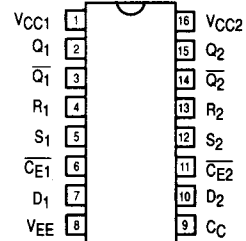


**AVAILABLE AS**

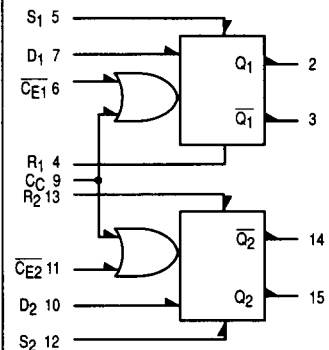
- 1) JAN: JM 38510/06101
  - 2) SMD: N/A
  - 3) 883: 10531/BXAJC
- X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E  
CERFLAT: F  
LCC: 2

The letter "M" appears before the slash on LCC.



**LOGIC DIAGRAM**



**3**

R-S TRUTH TABLE

R	S	$Q_{n+1}$
L	L	$Q_n$
L	H	H
H	L	L
H	H	N. D.

N. D. = Not Defined

A clock H is a clock transition from a Low to a High state

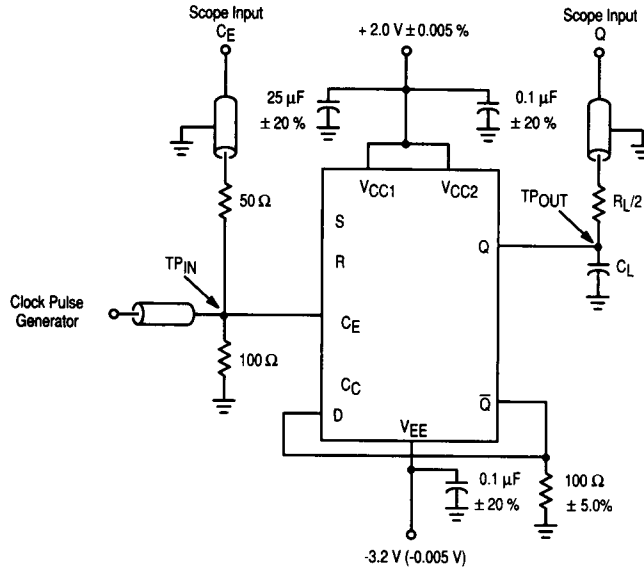
CLOCKED TRUTH TABLE

C	D	$Q_{n+1}$
L	∅	$Q_n$
H	L	L
H	H	H

∅ = Don't Care

$C = C_E + C_C$

3



NOTES

1. Perform test in accordance with test table: each output is tested separately.
2. All input and output cables are equal lengths of 50 Ω coaxial cables. Wire length should be  $\leq 0.250$  (6.35 mm) from tp in to input pin and tp out to output pin.
3. Outputs not under test should be connected to a 100 Ω resistor to ground.
4. Note that observed pulse amplitude is attenuated by one half.
5.  $R_L/2 = 50 \Omega \pm 5.0\%$ .
6.  $t_r = t_f = 2.0 \text{ ns}$  (20% - 80%).
7. Scope Input = 50 Ω GND.
8.  $C_L$  (test Jig)  $\leq 5.0 \text{ pF}$ .

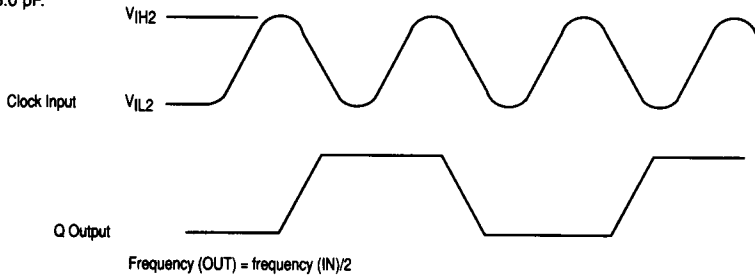
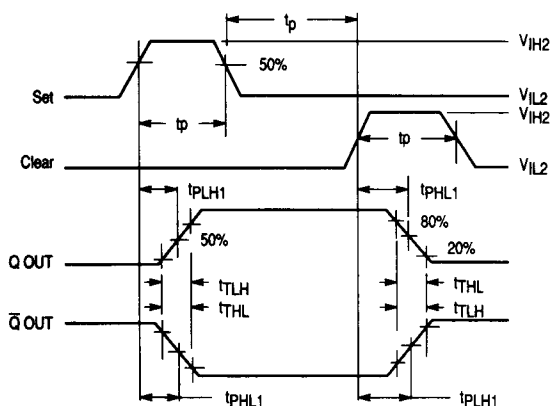
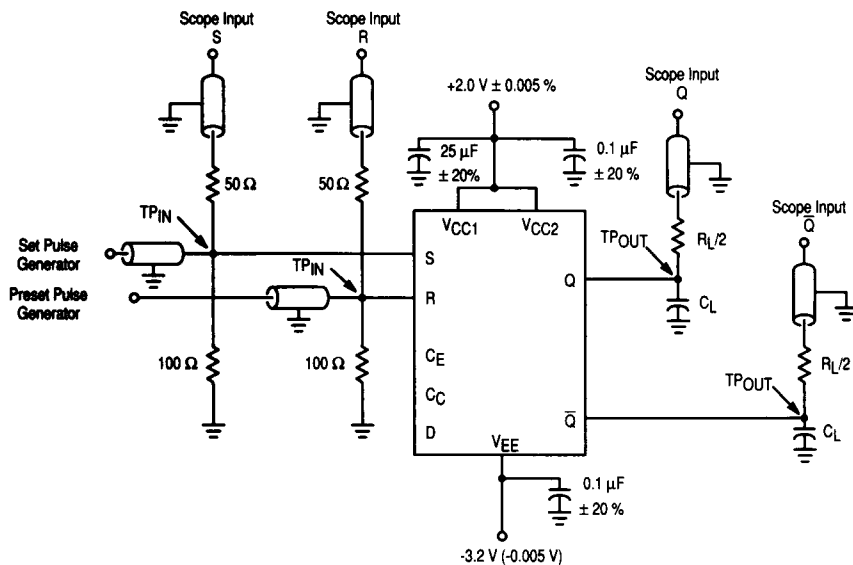
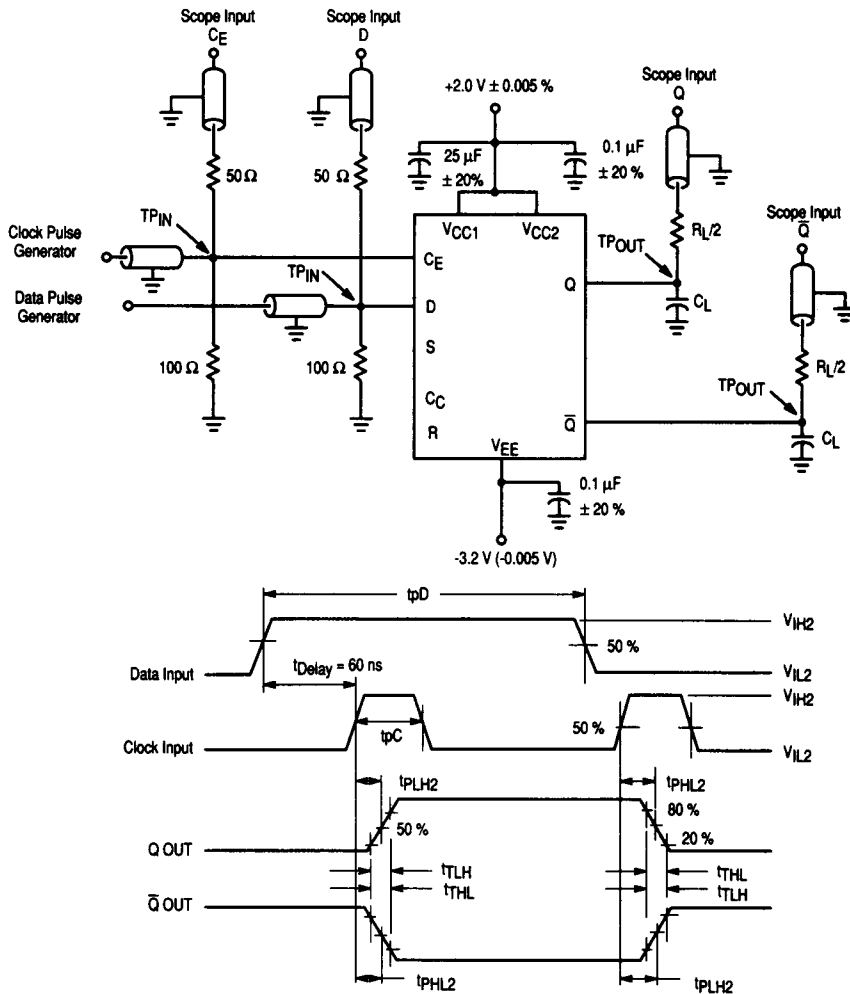


Figure 1. FMAX Test Circuit and Clock Input Sinewave

**NOTES**

1. Perform test in accordance with test table: each output is tested separately.
2. All input and output cables are equal lengths of 50  $\Omega$  coaxial cables. Wire length should be  $\leq 0.250$  (6.35 mm) from  $t_{p\text{ in}}$  to input pin and  $t_{p\text{ out}}$  to output pin.
3. Outputs not under test should be connected to a 100  $\Omega$  resistor to ground.
4. Note that observed pulse amplitude is attenuated by one half.
5.  $R_{L/2} = 50 \Omega \pm 5.0\%$ .
6.  $Z_{\text{OUT}} = 50 \Omega$ .
7.  $t_p$  (Set & Reset) = 40 ns.
8. PRR = 1.0 MHz.
9. Scope Input = 50  $\Omega$  to GND.
10.  $C_L$  (test Jig)  $\leq 5.0$  pF.

Figure 2. Set and Reset Switching Test Circuit

**NOTES**

1. Perform test in accordance with test table: each output is tested separately.
2. All input and output cables are equal lengths of 50  $\Omega$  coaxial cables. Wire length should be  $\leq 0.250$  (6.35 mm) from  $t_{p}$  in to input pin and  $t_{p}$  out to output pin.
3. Outputs not under test should be connected to a 100  $\Omega$  resistor to ground.
4. Note that observed pulse amplitude is attenuated by one half.
5.  $R_L/2 = 50 \Omega \pm 5.0\%$ .
6.  $Z_{OUT} = 50 \Omega$ .
7.  $t_{pD}(\text{Data}) = 150 \text{ ns}$ ,  $t_{pC}(\text{Clock}) = 40 \text{ ns}$ .
8. PRR = 1.0 MHz.
9. Scope Input = 50  $\Omega$  to GND.
10.  $C_L(\text{test Jig}) \leq 5.0 \text{ pF}$ .

**Figure 3. Synchronous Switching Test Circuit and Waveform**

# 10531 QUIESCENT LIMIT TABLE \*

## \* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)									
	V <sub>IH1</sub>	V <sub>IL1</sub>	V <sub>IH2</sub>	V <sub>IL2</sub>	V <sub>IH2</sub>	V <sub>IL2</sub>	V <sub>IHL</sub>	V <sub>ITL</sub>	V <sub>IHL</sub>	V <sub>VEE</sub>
T <sub>A</sub> = 25 °C	- 0.780	- 1.850	+ 1.11	+ 0.31	- 1.475	- 1.105	- 1.105	- 1.475	- 1.105	- 5.2
T <sub>A</sub> = 125 °C	- 0.630	- 1.820	+ 1.24	+ 0.36	- 1.400	- 1.000	- 1.000	- 1.400	- 1.000	- 5.2
T <sub>A</sub> = - 55 °C	- 0.880	- 1.920	+ 1.01	+ 0.28	- 1.510	- 1.255	- 1.255	- 1.510	- 1.255	- 5.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW									
		+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V <sub>CC</sub> = 0 V, Output Load = 100 Ω to - 2.0 V									
		Subgroup 1	Subgroup 2	Subgroup 3	Subgroup 1	Subgroup 2	Subgroup 3		V <sub>IH1</sub>	V <sub>IL1</sub>	V <sub>IH2</sub>	V <sub>IL2</sub>	V <sub>IHL</sub>	V <sub>ITL</sub>	V <sub>VEE</sub>	V <sub>CC</sub>	P. U. T.	
V <sub>OH</sub>	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	4, 5, 12, 13	4 - 7, 9 - 13			8	1, 16	2, 3, 14, 15			
V <sub>OL</sub>	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V	4, 5, 12, 13	4 - 7, 9 - 13			8	1, 16	2, 3, 14, 15			
V <sub>OH1</sub>	High Output Voltage	- 0.95		- 0.845		- 1.10		V	4, 5, 12, 13	4, 7, 9 - 13	4, 5, 12, 13	4 - 7, 9 - 13	8	1, 16	2, 3, 14, 15			
V <sub>OL1</sub>	Low Output Voltage		- 1.60		- 1.525		- 1.635	V	4, 5, 12, 13	4 - 7, 9 - 13	4, 5, 12, 13	4 - 7, 9 - 13	8	1, 16	2, 3, 14, 15			
I <sub>EE</sub>	Power Supply Current	- 56		- 62		- 62		mA					8	1, 16	8			
I <sub>IH</sub>	Input Current High		265		450		450	μA	9				8	1, 16	9			
I <sub>IH1</sub>	Input Current High		220		375		375	μA	6, 11				8	1, 16	6, 11			
I <sub>IH2</sub>	Input Current High		330		565		565	μA	4, 5, 12, 13				8	1, 16	4, 5, 12, 13			
I <sub>IH3</sub>	Input Current High		245		420		420	μA	7, 10				8	1, 16	7, 10			
I <sub>IL</sub>	Input Current Low	0.5		0.3		0.5		μA					8	1, 16	4 - 7, 9 - 13			

## 10531 QUIESCENT LIMIT TABLE \*

### \* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100  $\Omega$  resistor to - 2.0 volts.

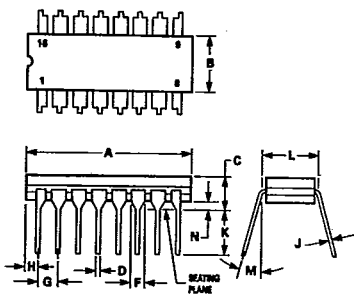
Test Temperature	Test Voltage Values (Volts)							
	V <sub>IH1</sub>	V <sub>IL1</sub>	V <sub>IH2</sub>	V <sub>IL2</sub>	V <sub>IHL</sub>	V <sub>ITH</sub>	VEE	VEE1
T <sub>A</sub> = 25 °C	- 0.780	- 1.850	+ 1.11	+ 0.31	- 1.475	- 1.105	- 5.2	- 3.2
T <sub>A</sub> = 125 °C	- 0.630	- 1.820	+ 1.24	+ 0.36	- 1.400	- 1.000	- 5.2	- 3.2
T <sub>A</sub> = - 55 °C	- 0.880	- 1.920	+ 1.01	+ 0.28	- 1.510	- 1.255	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
		+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V <sub>CC</sub> = 2.0 V, Output Load = 100 $\Omega$ to GND					
		Subgroup 9		Subgroup 10		Subgroup 11			V <sub>IN</sub>	V <sub>OUT</sub>	V <sub>CC</sub>	V <sub>EEL</sub>	P. U. T.	
t <sub>TLH</sub>	Rise Time	1.1	4.5	1.1	4.9	1.0	4.6	ns	4 - 7, 10 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15	
t <sub>THL</sub>	Fall Time	1.1	4.5	1.1	4.9	1.0	4.6	ns	4 - 7, 10 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15	
t <sub>pLH1</sub>	Propagation Delay	1.2	4.3	1.2	4.9	1.1	4.5	ns	4 - 7, 10 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15	
t <sub>pLH2</sub>	Propagation Delay	1.5	4.5	1.5	5.0	1.4	4.6	ns	4 - 7, 10 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15	
t <sub>pHL1</sub>	Propagation Delay	1.2	4.3	1.2	4.9	1.1	4.5	ns	4 - 7, 10 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15	
t <sub>pHL2</sub>	Propagation Delay	1.5	4.5	1.5	5.0	1.4	4.6	ns	4 - 7, 10 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15	
f <sub>log</sub>	Toggle Frequency (max)	125		125		105		MHz	6, 11	2, 15	1, 16	8	2, 3, 14, 15	

# PACKAGE OUTLINE DIMENSIONS

A letter suffix to the MECL logic function part number is used to specify the package style (see drawings below). See appropriate selector guide for specific packaging available for a given device type.

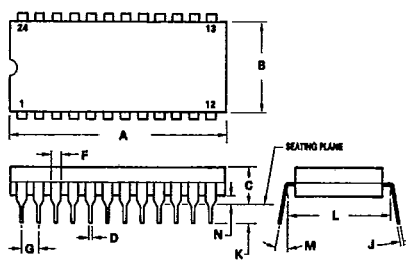
**L SUFFIX  
CERAMIC PACKAGE  
CASE 620-09**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.95	19.81	0.790	0.780
B	6.32	6.28	0.249	0.247
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	2.27	2.27	0.290	0.310
M	— 15°		— 15°	
N	0.51	1.02	0.020	0.040

- NOTES:
- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
  - PACKAGE INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
  - DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

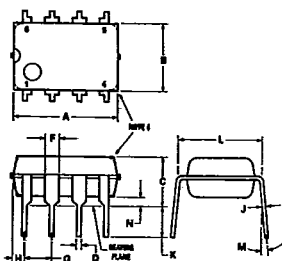
**L SUFFIX  
CERAMIC PACKAGE  
CASE 623-05** (LW SUFFIX FOR MC10H181 ONLY)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.77	1.92	0.070	0.076
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0° 15°		0° 15°	
N	0.51	1.27	0.020	0.050

- NOTES:
- DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
  - LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

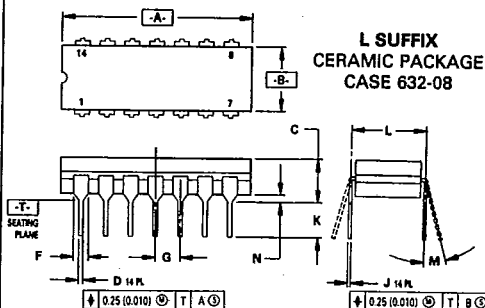
**P SUFFIX  
PLASTIC PACKAGE  
CASE 626-04**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	— 10°		— 10°	
N	0.51	0.76	0.020	0.030

- NOTES:
- LEAD POSITIONAL TOLERANCE:  
⊕ 0.13 (0.005) ⊕ T | A ⊕ B ⊕
  - DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  - PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
  - DIMENSIONS A AND B ARE DATUMS.
  - DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

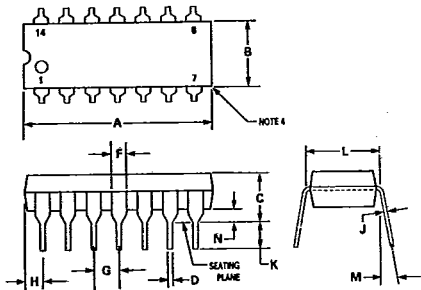
**L SUFFIX  
CERAMIC PACKAGE  
CASE 632-08**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.23	7.11	0.245	0.280
C	3.94	5.08	0.155	0.200
D	0.38	0.50	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	3.18	4.31	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0° 15°		0° 15°	
N	0.51	1.01	0.020	0.040

- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - CONTROLLING DIMENSION: INCH.
  - DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  - DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

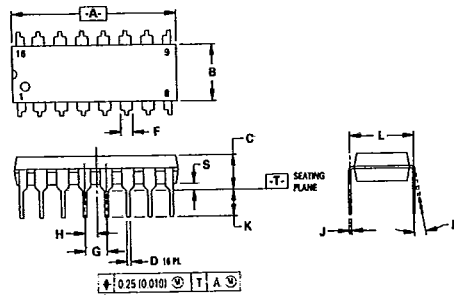
**P SUFFIX  
PLASTIC PACKAGE  
CASE 646-06**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.29	1.01	0.015	0.039

- NOTES:
- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
  - DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
  - DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
  - ROUNDED CORNERS OPTIONAL.

**P SUFFIX  
PLASTIC PACKAGE  
CASE 648-08**

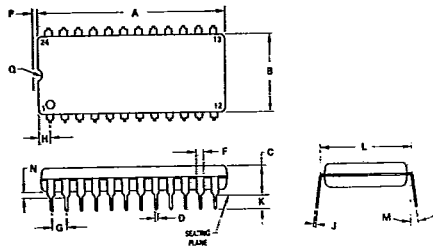


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - CONTROLLING DIMENSION: INCH.
  - DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
  - DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
  - ROUNDED CORNERS OPTIONAL.

**P SUFFIX  
PLASTIC PACKAGE  
CASE 649-03**

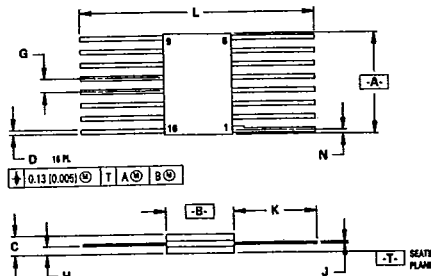
**(PW SUFFIX  
FOR MC10H181  
ONLY)**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	10°		10°	
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

- NOTES:
- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
  - DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

**F SUFFIX  
CERAMIC PACKAGE  
CASE 650-05**

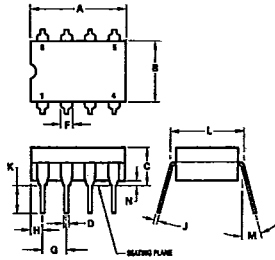


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	9.90	0.370	0.390
B	6.73	6.80	0.265	0.269
C	1.53	2.15	0.060	0.085
D	0.38	0.48	0.014	0.019
G	1.27 BSC		0.050 BSC	
H	0.64	0.01	0.025	0.040
J	0.11	0.17	0.004	0.007
K	6.35	9.39	0.250	0.370
L	18.93	—	0.745	—
N	—	0.50	—	0.020

- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - CONTROLLING DIMENSION: INCH.
  - DIMENSION "A" AND "B" ALLOW FOR LID MISMATCH, AND GLASS MENISCUS.
  - DIMENSION "H" SHALL BE MEASURED AT THE POINT OF EXIT OF THE LEAD FROM THE BODY.
  - LEAD NUMBER 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER.
  - DIMENSION "J" INCLUDES SOLDER LEAD FINISH.
  - LEAD NUMBERS SHOWN FOR REFERENCE ONLY.



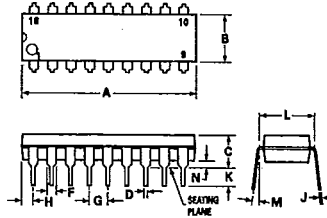
**L SUFFIX  
CERAMIC PACKAGE  
CASE 693-02**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.91	10.92	0.390	0.430
B	6.22	6.99	0.245	0.275
C	4.32	5.08	0.170	0.200
D	0.41	0.51	0.016	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	1.14	1.65	0.045	0.065
J	0.20	0.30	0.008	0.012
K	3.18	4.08	0.125	0.160
L	7.37	7.87	0.290	0.310
M	—	15°	—	15°
N	0.51	1.02	0.020	0.040

- NOTES:  
 1. LEADS WITHIN 0.13 mm (0.005) RAD OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.  
 2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

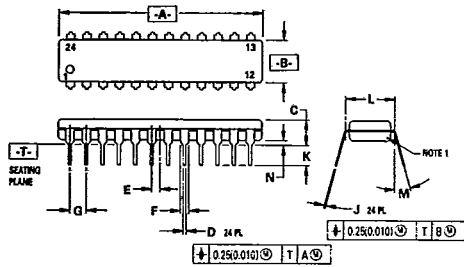
**P SUFFIX  
PLASTIC PACKAGE  
CASE 707-02**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.27	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

- NOTES:  
 1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.  
 2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.  
 3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

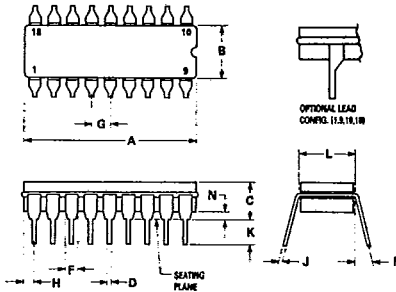
**P SUFFIX  
PLASTIC PACKAGE  
CASE 724-03**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.25	32.13	1.230	1.265
B	6.35	6.85	0.250	0.270
C	3.68	4.44	0.145	0.175
D	0.38	0.51	0.015	0.020
E	1.27 BSC		0.050 BSC	
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
J	0.18	0.30	0.007	0.012
K	2.80	3.56	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

- NOTES:  
 1. CHAMFERED CONTOUR OPTIONAL.  
 2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.  
 3. DIMENSIONS AND TOLERANCES PER ANSI Y14.84, 1982.  
 4. CONTROLLING DIMENSION: INCH.

**L SUFFIX  
CERAMIC PACKAGE  
CASE 726-04**



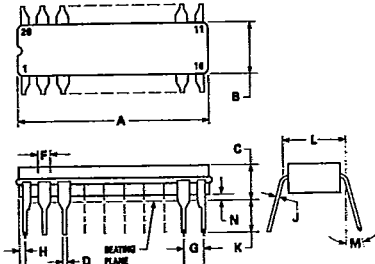
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.35	23.11	0.880	0.910
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

- NOTES:  
 1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.  
 2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.  
 3. DIM "A" & "B" INCLUDES MENISCUS.  
 4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 9, 10, AND 18.

PACKAGE OUTLINE DIMENSIONS (continued)

1

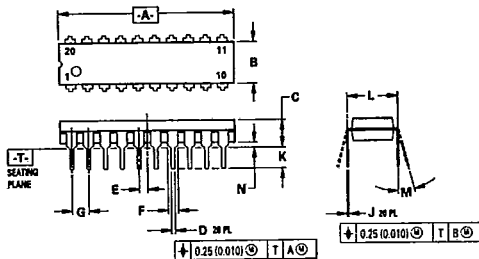
**L SUFFIX  
CERAMIC PACKAGE  
CASE 732-03**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.80	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

- NOTES:  
 1. LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.  
 2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.  
 3. DIM A AND B INCLUDES MENISCUS.

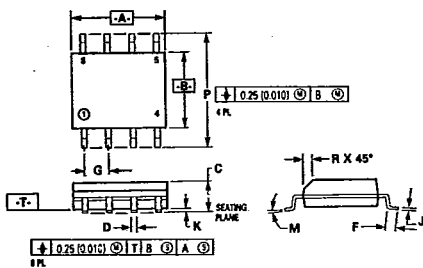
**P SUFFIX  
PLASTIC PACKAGE  
CASE 738-03**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	25.55	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.81	4.57	0.150	0.180
D	0.38	0.56	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

- NOTES:  
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
 2. CONTROLLING DIMENSION: INCH.  
 3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.  
 4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.

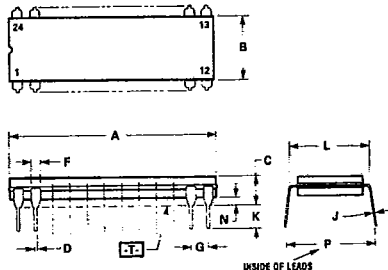
**D SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751-03**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.90	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.015	0.049
G	0.27 BSC		0.050 BSC	
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

- NOTES:  
 1. DIMENSIONS "A" AND "B" ARE DATUMS AND "T" IS A DATUM SURFACE.  
 2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
 3. CONTROLLING DIM: MILLIMETER.  
 4. DIMENSION "A" AND "B" DO NOT INCLUDE MOLD PROTRUSION.  
 5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

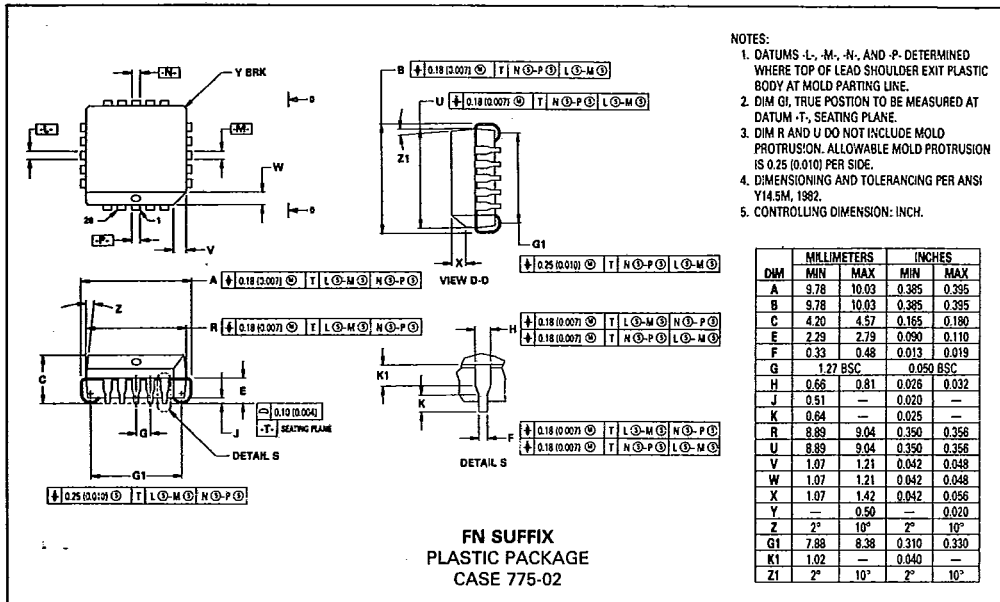
**L SUFFIX  
CERAMIC PACKAGE  
CASE 758-01**



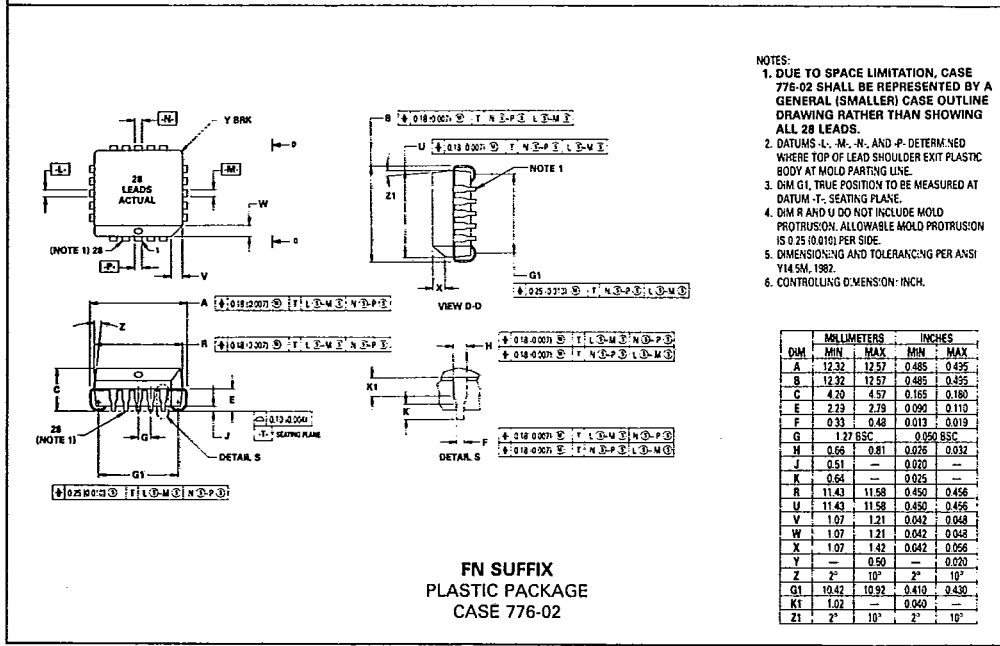
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.50	32.64	1.240	1.285
B	7.24	7.75	0.285	0.305
C	3.68	4.44	0.145	0.175
D	0.38	0.53	0.015	0.021
F	1.14	1.97	0.045	0.062
G	2.54 BSC		0.100 BSC	
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	7.62	7.87	0.300	0.310
N	0.51	1.27	0.020	0.050
P	9.14	10.16	0.360	0.400

- NOTES:  
 1. DIMENSION A IS DATUM.  
 2. POSITIONAL TOLERANCE FOR LEADS: 24 PLACES  $\pm 0.25(0.010) \text{ } \textcircled{T} \text{ } \textcircled{A} \text{ } \textcircled{B}$   
 3. [T] IS SEATING PLANE.  
 4. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.  
 5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

1



- NOTES:
1. DATUMS -L-, M-, N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
  2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
  3. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
  4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  5. CONTROLLING DIMENSION: INCH.



- NOTES:
1. DUE TO SPACE LIMITATION, CASE 776-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 28 LEADS.
  2. DATUMS -L-, M-, N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
  3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
  4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
  5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  6. CONTROLLING DIMENSION: INCH.

## MECL Logic Surface Mount

### WHY SURFACE MOUNT?

Surface Mount Technology is now being utilized to offer answers to many problems that have been created in the use of insertion technology.

Limitations have been reached with insertion packages and PC board technology. Surface Mount Technology offers the opportunity to continue to advance the State-of-the-Art designs that cannot be accomplished with Insertion Technology.

Surface Mount Packages allow more optimum device performance with the smaller Surface Mount configuration. Internal lead lengths, parasitic capacitance and inductance that placed limitations on chip performance have been reduced.

The lower profile of Surface Mount Packages allows more boards to be utilized in a given amount of space. They are stacked closer together and utilize less total volume than insertion populated PC boards.

Printed circuit costs are lowered with the reduction of the number of board layers required. The elimination or reduction of the number of plated through holes in the board, contribute significantly to lower PC board prices.

Surface Mount assembly does not require the preparation of components that are common on insertion technology lines. Surface Mount components are sent directly to the assembly line, eliminating an intermediate step.

Automatic placement equipment is available that can place Surface Mount components at the rate of a few thousand per hour to hundreds of thousands of components per hour.

Surface Mount Technology is cost effective, allowing the manufacturer the opportunity to produce smaller units and offer increased functions with the same size product.

### MECL AVAILABILITY IN SURFACE MOUNT

Motorola is now offering MECL 10K and MECL 10KH in the PLCC (Plastic Leaded Chip Carrier) packages.

MECL in PLCC may be ordered in conventional plastic rails or on Tape and Reel. Refer to the Tape and Reel section for ordering details.

### TAPE AND REEL

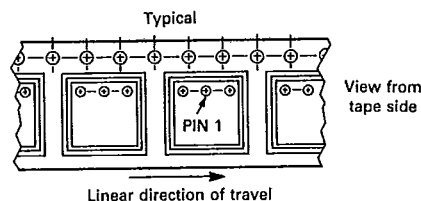
Motorola has now added the convenience of Tape and Reel packaging for our growing family of standard Integrated Circuit products. The packaging fully conforms to

the latest EIA RS-481A specification. The antistatic embossed tape provides a secure cavity sealed with a peel-back cover tape.

### GENERAL INFORMATION

- Reel Size 13 inch (330 mm) Suffix: R2
- Tape Width 16 mm
- Units/Reel 1000

### MECHANICAL POLARIZATION



### ORDERING INFORMATION

- Minimum Lot Size/Device Type = 3000 Pieces.
- No Partial Reel Counts Available.
- To order devices which are to be delivered in Tape and Reel, add the appropriate suffix to the device number being ordered.

#### EXAMPLE:

#### ORDERING CODE

MC10100FN  
 MC10100FNR2  
 MC10H100FN  
 MC10H100FNR2  
 MC12015D  
 MC12015DR2

#### SHIPMENT METHOD

Magazines (Rails)  
 13 inch Tape and Reel  
 Magazines (Rails)  
 13 inch Tape and Reel  
 Magazines (Rails)  
 13 inch Tape and Reel

### DUAL-IN-LINE PACKAGE TO PLCC PIN CONVERSION DATA

The following tables give the equivalent I/O pinouts of Dual-In-Line (DIL) packages and Plastic Leaded Chip Carrier (PLCC) packages.

#### Conversion Tables

16 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
20 PIN PLCC	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20

20 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
20 PIN PLCC	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

24 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
28 PIN PLCC	2	3	4	5	6	7	9	10	11	12	13	14	16	17	18	19	20	21	23	24	25	26	27	28