



128K × 8 CMOS STATIC RAM

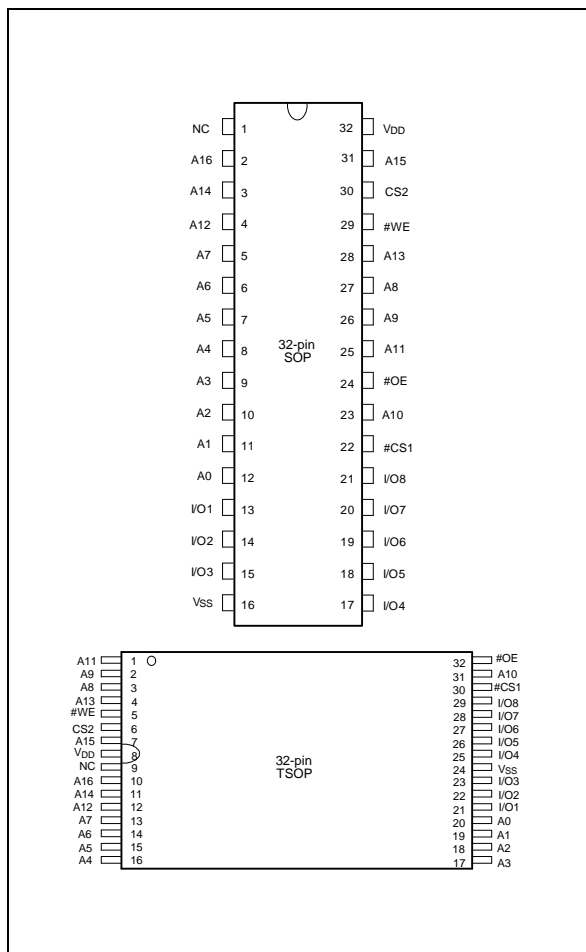
GENERAL DESCRIPTION

The W24L11 is a normal-speed, very low-power CMOS static RAM organized as 131072 × 8 bits that operates on a wide voltage range from 3.3V to 5V power supply. This device is manufactured using Winbond's high performance CMOS technology.

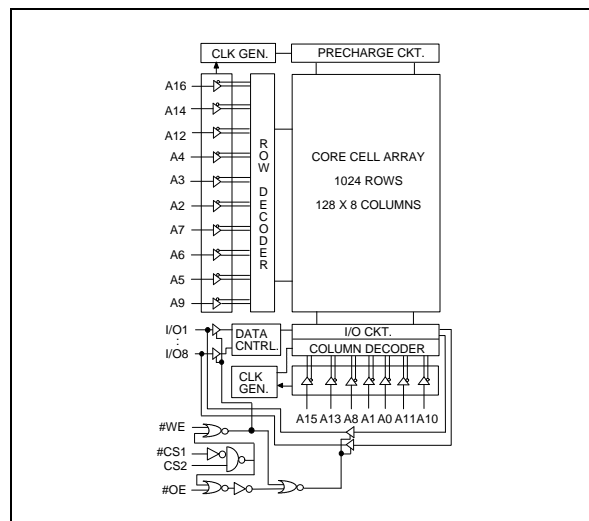
FEATURES

- Low power consumption
- Access time: 55/70 nS
- 3.3V/5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Battery back-up operation capability
- Data retention voltage: 2V (min.)
- Packaged 450 mil SOP, standard type one, TSOP (8 mm × 20 mm), small type one and TSOP (8 mm × 13.4 mm)

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A16	Address Inputs
I/O1–I/O8	Data Inputs/Outputs
#CS1, CS2	Chip Select Input
#WE	Write Enable Input
#OE	Output Enable Input
VDD	Power Supply
VSS	Ground
NC	No Connection

TRUTH TABLE

#CS1	CS2	#OE	#WE	MODE	I/O1- I/O8	VDD CURRENT
H	X	X	X	Not Selected	High Z	ISB, ISB1
X	L	X	X	Not Selected	High Z	ISB, ISB1
L	H	H	H	Output Disable	High Z	IDD
L	H	L	H	Read	Data Out	IDD
L	H	X	L	Write	Data In	IDD

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER		RATING		UNIT
		3.3V	5V	
Supply Voltage to VSS Potential		-0.5 to +4.6	-0.5 to +7.0	V
Input/Output to VSS Potential		-0.5 to VDD +0.5		V
Allowable Power Dissipation		1.0		W
Storage Temperature		-65 to +150		°C
Operating Temperature	L/LL	0 to 70		°C
	LE	-20 to 85		

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(VDD = 5V ±10%; VDD = 3.3V ±5%; VSS = 0V; TA (°C) = 0 to 70 for LL, -20 to 85 for LE)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	MAX.	UNIT	
Input Low Voltage	VIL	-	3.3V	-0.5	+0.6	V
			5V	-0.5	+0.8	
Input High Voltage	VIH	-	+2.0	VDD +0.5	V	
Input Leakage Current	ILI	VIN = VSS to VDD	-1	+1	μA	
Output Leakage Current	ILO	V/I/O = VSS to VDD, #CS1 = VIH (min.) or CS2 = VIL (max.) or #OE = VIH (min.) or #WE = VIL (max.)	-1	+1	μA	
Output Low Voltage	VOL	IOL = +2.1 mA	-	0.4	V	



Operating Characteristics, continued

PARAMETER	SYM.	TEST CONDITIONS	3.3V		5V		UNIT		
			MIN.	MAX.	MIN.	MAX.			
Output High Voltage	VOH	IOH = -1.0 mA	2.2	-	2.4	-	V		
Operating Power Supply Current	IDD	#CS1= VIL (max.) and CS2 = VIH (min.), I/O = 0 mA, Cycle = min. Duty =100%	55	-	50	-	80	mA	
			70	-	40	-	70		
Standby Power Supply Current	ISB	#CS1= VIH (min.) or CS2 = VIL (max.) Cycle = min. Duty = 100%	-	1	-	3	mA		
	ISB1	#CS1 ≥ VDD -0.2V or CS2 ≤ 0.2V	LL/LE	-	50	-		50/70	μA
			L	-	100	-		100	

Note: Typical parameter is measured under ambient temperature TA = 25° C and VDD = 3.3V/5V

CAPACITANCE

(VDD = 5V ±10%; VDD = 3.3V ±5%, TA = 25° C, f = 1 MHz)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	CIN	VIN = 0V	6	pF
Input/Output Capacitance	Ci/O	VOUT = 0V	8	pF

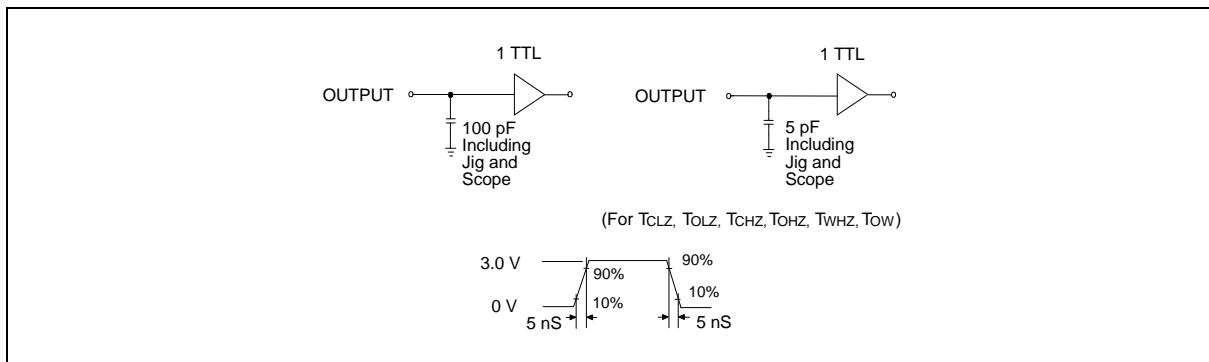
Note: These parameters are sampled but not 100% tested.

AC Characteristics

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V
Output Load	See the drawing below

AC Test Loads and Waveform





AC Characteristics, continued

(V_{DD} = 5V ±10%; V_{DD} = 3.3V ±5%; V_{SS} = 0V; T_A (°C) = 0 to 70 for LL, -20 to 85 for LE)**Read Cycle**

PARAMETER	SYM.	3.3V/5V				UNIT
		55		70		
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	TRC	55	-	70	-	nS
Address Access Time	TAA	-	55	-	70	nS
Chip Select Access Time	TACS	-	55	-	70	nS
Output Enable to Output Valid	TAOE	-	30	-	35	nS
Chip Selection to Output in Low Z	TCLZ*	10	-	10	-	nS
Output Enable to Output in Low Z	TOLZ*	5	-	5	-	nS
Chip Deselection to Output in High Z	TCHZ*	-	25	-	30	nS
Output Disable to Output in High Z	TOHZ*	-	25	-	30	nS
Output Hold from Address Change	TOH	10	-	10	-	nS

* These parameters are sampled but not 100% tested

Write Cycle

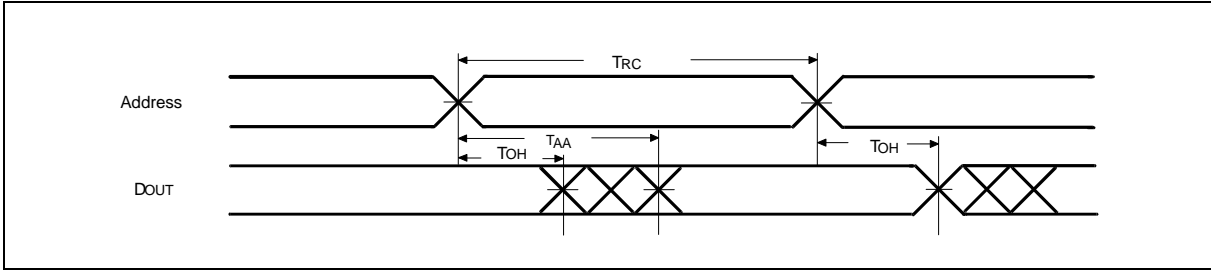
PARAMETER	SYM.	3.3/5V				UNIT
		55		70		
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	TWC	55	-	70	-	nS
Chip Selection to End of Write	TCW	40	-	50	-	nS
Address Valid to End of Write	TAW	40	-	50	-	nS
Address Setup Time	TAS	0	-	0	-	nS
Write Pulse Width	TWP	45	-	50	-	nS
Write Recovery Time	#CS1, CS2, #WE	TWR	0	0	-	nS
Data Valid to End of Write	TDW	40/25	-	45/30	-	nS
Data Hold from End of Write	TDH	0	-	0	-	nS
Write to Output in High Z	TWHZ*	-	25	-	25	nS
Output Disable to Output in High Z	TOHZ*	-	25	-	25	nS
Output Active from End of Write	TOW	5	-	5	-	nS

* These parameters are sampled but not 100% tested

TIMING WAVEFORMS

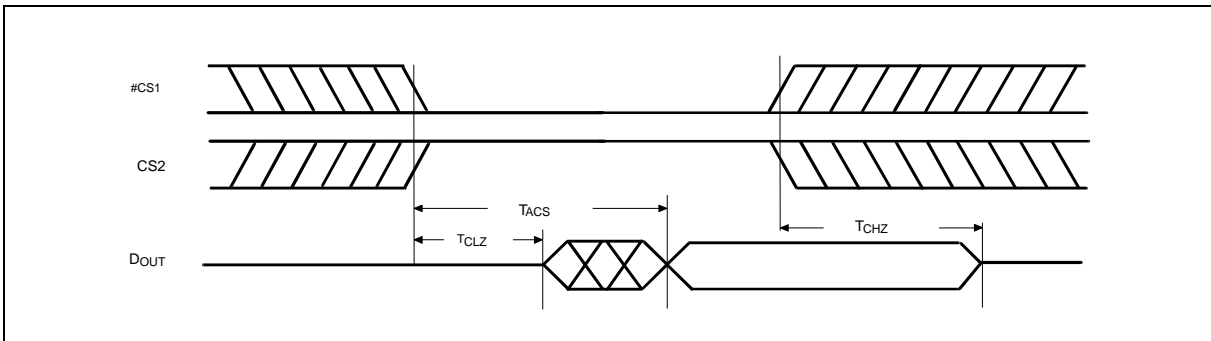
Read Cycle 1

(Address Controlled)



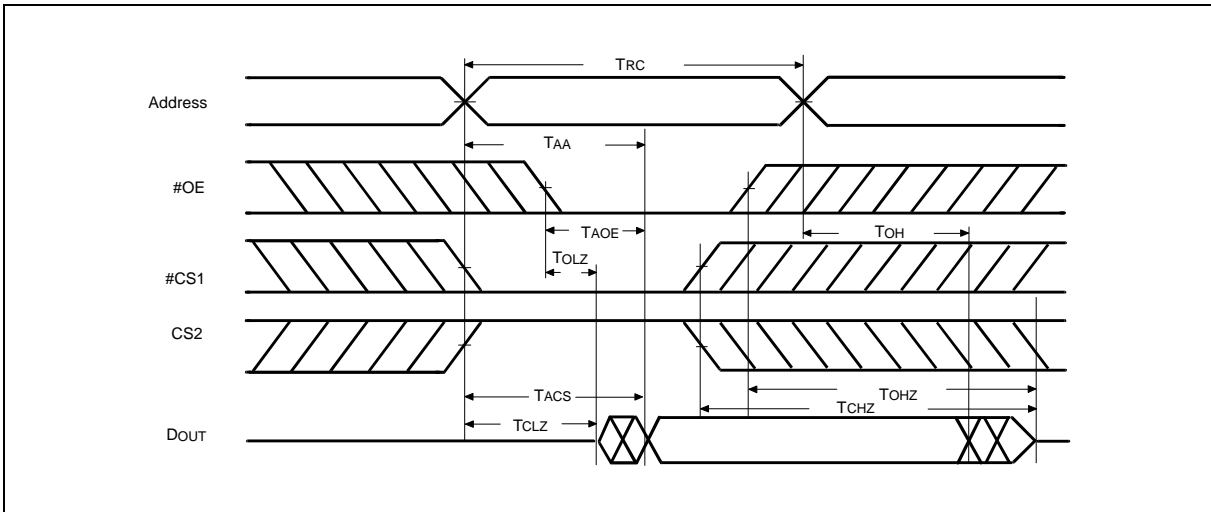
Read Cycle 2

(Chip Select Controlled)



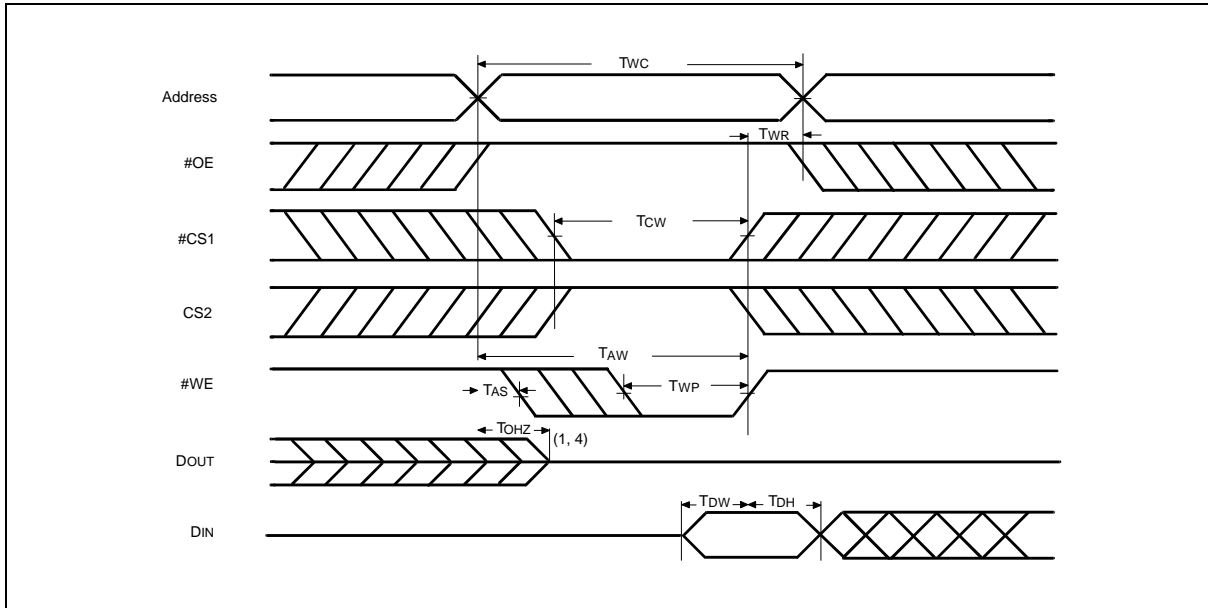
Read Cycle 3

(Output Enable Controlled)



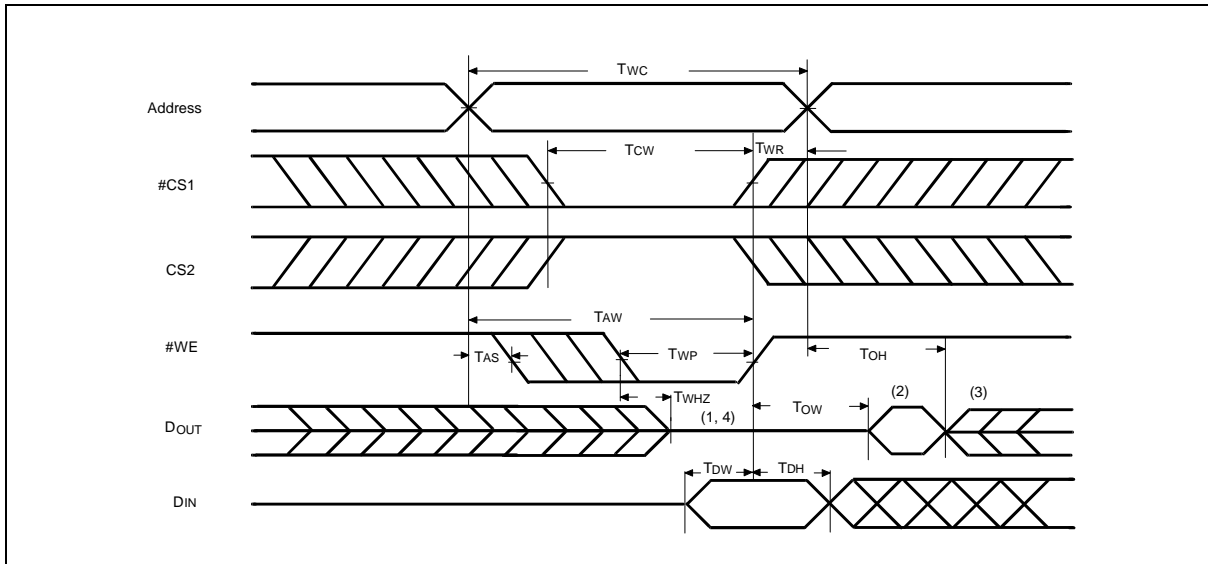
Timing Waveforms, continued

Write Cycle 1



Write Cycle 2

(#OE= VIL Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured ± 500 mV from steady state with $C_L = 5$ pF. This parameter is guaranteed but not 100% tested.

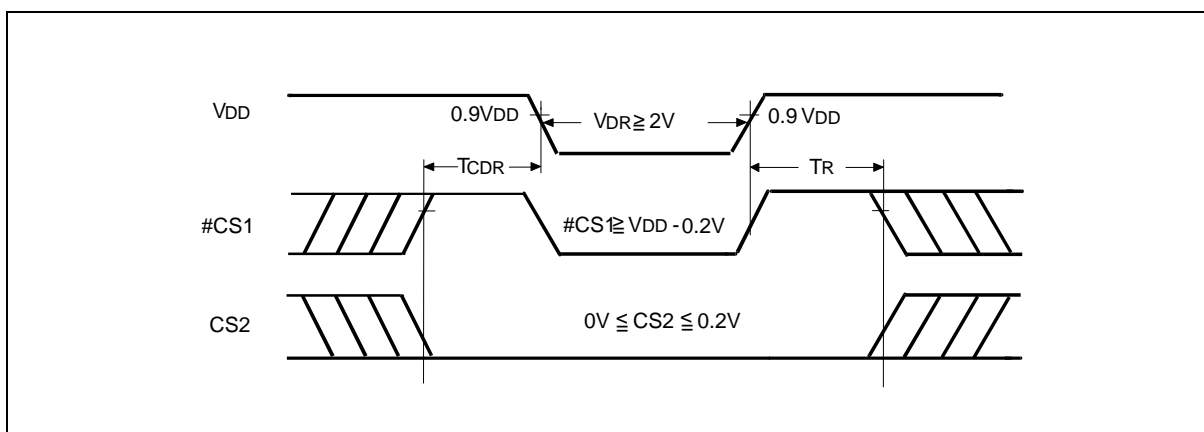
DATA RETENTION CHARACTERISTICS

(T_A (°C) = 0 to 70 for LL, -20 to 85 for LE)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{DD} for Data Retention	VDR	#CS1 ≥ V _{DD} - 0.2V or CS2 ≤ 0.2V	2.0	-	-	V
Data Retention Current	I _{DDDR}	#CS1 ≥ V _{DD} - 0.2V or CS2 ≤ 0.2V, V _{DD} = 3V	-	-	50	μA
Chip Deselect to Data Retention Time	T _{CDR}	See data retention waveform	0	-	-	nS
Operation Recovery Time	T _R		T _{RC} *	-	-	nS

* Read Cycle Time

DATA RETENTION WAVEFORM



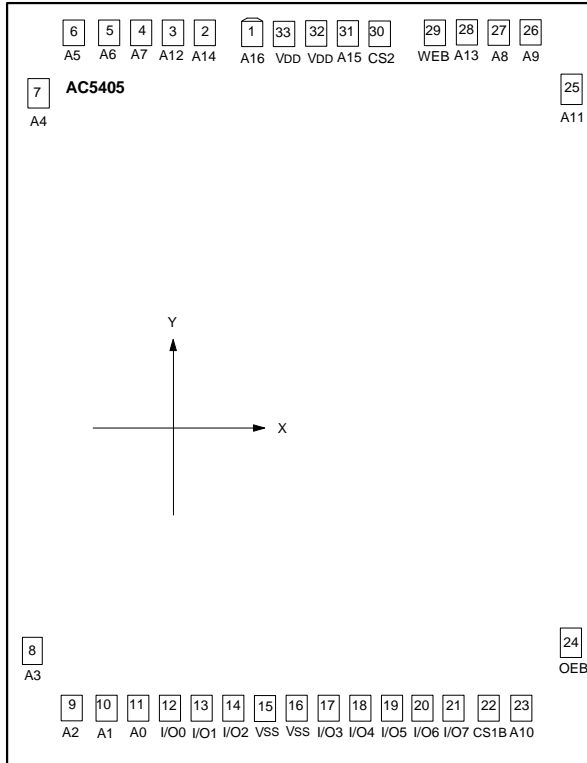
ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	OPERATING VOLTAGE (V)	OPERATING TEMPERATURE (°C)	STANDBY CURRENT MAX. (mA)	PACKAGE
W24L11S-55LE	55	3.3V/5V	-20 to 85	50	450 mil SOP
W24L11T-55LE	55	3.3V/5V	-20 to 85	50	Standard type one TSOP
W24L11Q-55LE	55	3.3V/5V	-20 to 85	50	Small type one TSOP
W24L11S-55LL	55	3.3V/5V	0 to 70	50	450 mil SOP
W24L11T-55LL	55	3.3V/5V	0 to 70	50	Standard type one TSOP
W24L11Q-55LL	55	3.3V/5V	0 to 70	50	Small type one TSOP
W24L11S-55L	55	3.3V/5V	0 to 70	100	450 mil SOP
W24L11T-55L	55	3.3V/5V	0 to 70	100	Standard type one TSOP
W24L11Q-55L	55	3.3V/5V	0 to 70	100	Small type one TSOP
W24L11S-70LE	70	3.3V/5V	-20 to 85	50	450 mil SOP
W24L11T-70LE	70	3.3V/5V	-20 to 85	50	Standard type one TSOP
W24L11Q-70LE	70	3.3V/5V	-20 to 85	50	Small type one TSOP
W24L11S-70LL	70	3.3V/5V	0 to 70	50	450 mil SOP
W24L11T-70LL	70	3.3V/5V	0 to 70	50	Standard type one TSOP
W24L11Q-70LL	70	3.3V/5V	0 to 70	50	Small type one TSOP
W24L11S-70L	70	3.3V/5V	0 to 70	100	450 mil SOP
W24L11T-70L	70	3.3V/5V	0 to 70	100	Standard type one TSOP
W24L11Q-70L	70	3.3V/5V	0 to 70	100	Small type one TSOP

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

BONDING PAD DIAGRAM

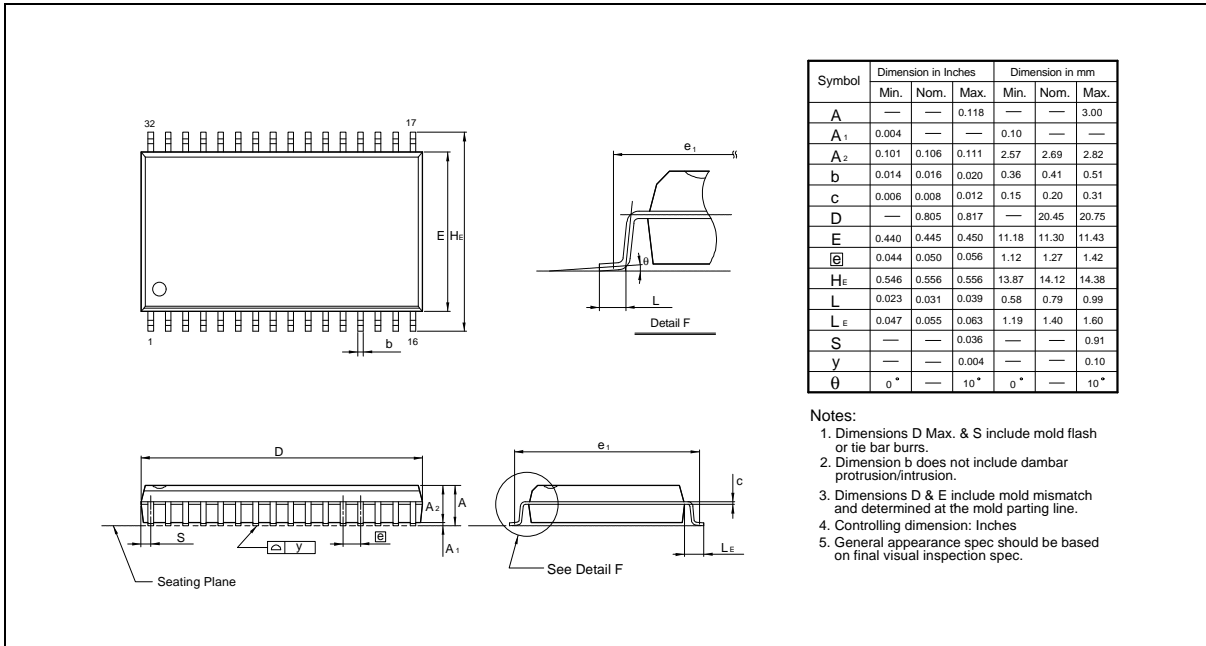


PAD NO.	X	Y
1	-485.31	2376.64
2	-1200.87	2376.64
3	-1341.05	2376.64
4	-1480.80	2376.64
5	-1622.21	2376.64
6	-1767.47	2376.64
7	-1993.03	2228.49
8	-1990.55	-2275.79
9	-1789.57	-2382.05
10	-1556.20	-2382.05
11	-1405.83	-2382.05
12	-1169.73	-2383.00
13	-870.28	-2383.00
14	-567.65	-2383.00
15	-336.94	-2385.00
16	-112.55	-2385.00
17	224.85	-2383.00
18	497.55	-2383.00
19	772.25	-2383.00
20	1044.95	-2383.00
21	1319.65	-2383.00
22	1537.77	-2382.05
23	1773.94	-2382.05
24	1985.78	-2297.62
25	1987.47	2221.27
26	1669.63	2376.64
27	1451.03	2376.64
28	1196.59	2376.64
29	956.65	2376.64
30	219.67	2376.64
31	79.47	2376.64
32	-145.06	2343.58
33	-353.56	2343.58

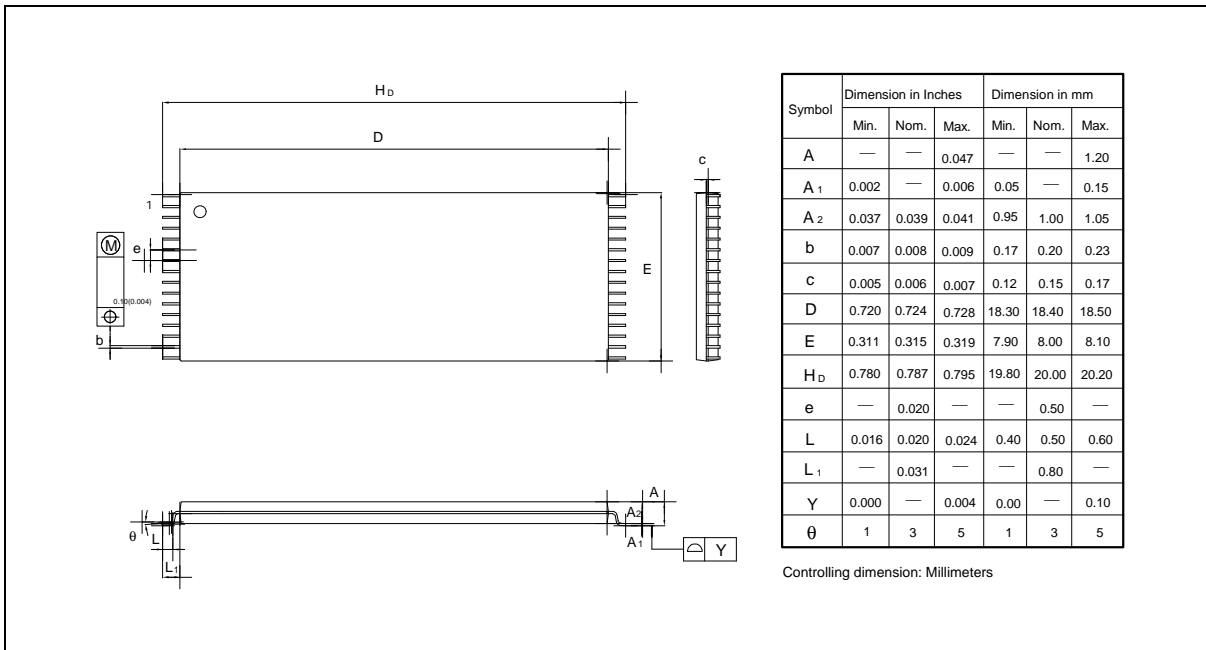
Note: For bare chip form (C.O.B.) applications, the substrate must be connected to VDD or left floating in the PCB layout.

PACKAGE DIMENSIONS

32-pin SOP Wide Body

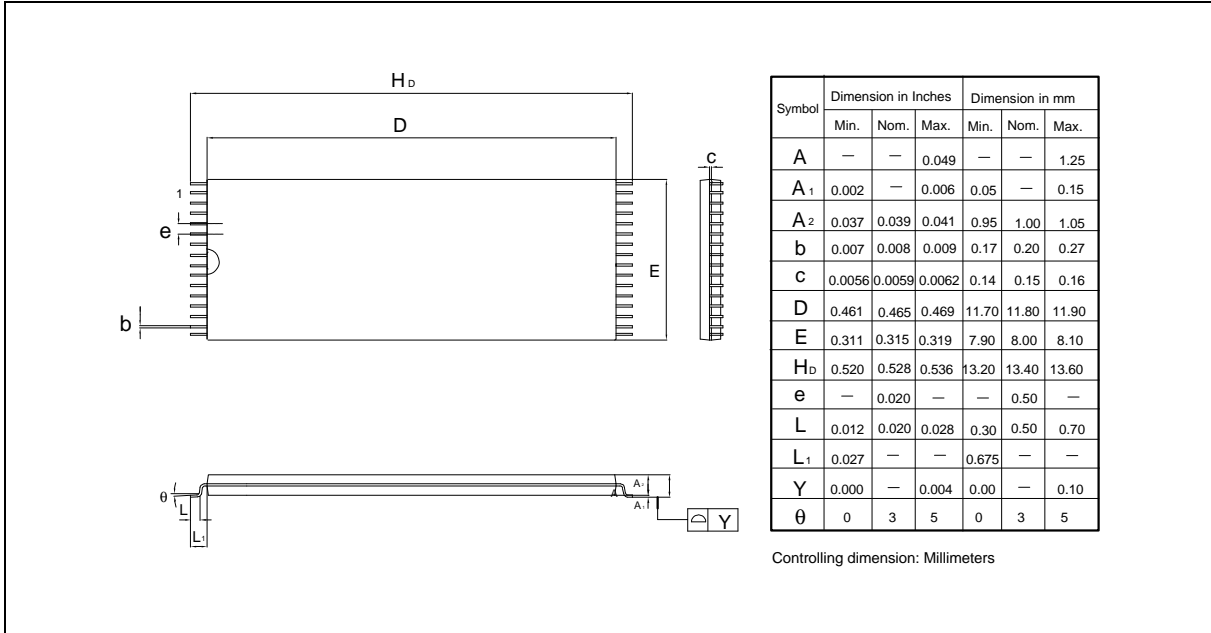


32-pin Standard Type One TSOP



Package Dimensions, continued

32-pin Small Type One TSOP





VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Oct. 1999	-	Initial Issued
A2	May 2000	1, 2, 8, 9	Delete 32-pin P-DIP Package; Add LE in Operating Characteristics, Data Retention Characteristics & Ordering Info.
		9	Add in Bonding Pad Diagram
A3	Dec. 2000	1, 2, 3, 4, 8	Add in 5V specification
A4	August 7, 2001	1	Add access time of 55 nS
		3	Add operating power supply current of 55 nS
		4	Add read cycle & write cycle of 55 nS
		9	Add 55 nS for Ordering Information



Headquarters

No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5792766

<http://www.winbond.com.tw/>

Voice & Fax-on-demand: 886-2-27197006

Taipei Office

11F, No. 115, Sec. 3, Min-Sheng East Rd.,
Taipei, Taiwan
TEL: 886-2-27190505
FAX: 886-2-27197502

Winbond Electronics (H.K.) Ltd.

Unit 9-15, 22F, Millennium City,
No. 378 Kwun Tong Rd;
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064

Winbond Electronics North America Corp.

Winbond Memory Lab.
Winbond Microelectronics Corp.
Winbond Systems Lab.

2727 N. First Street, San Jose,
CA 95134, U.S.A.
TEL: 408-9436666
FAX: 408-5441798

Note: All data and specifications are subject to change without notice.