IS62LV1024LL

128K x 8 LOW POWER and LOW Vcc CMOS STATIC RAM

JANUARY 2001

FEATURES

- Access times of 45, 55, and 70 ns
- Low active power: 60 mW (typical)
- Low standby power: 15 µW (typical) CMOS standby
- Low data retention voltage: 2V (min.)
- Ultra Low Power
- Output Enable ($\overline{OE}$) and two Chip Enable ($\overline{CE1}$ and CE2) inputs for ease in applications
- TTL compatible inputs and outputs
- Single 2.5V to 3.3V
- Industrial temperature available
- Available in 32-pin TSOP (Type I), 32-pin STSOP, and 450-mil SOP

DESCRIPTION

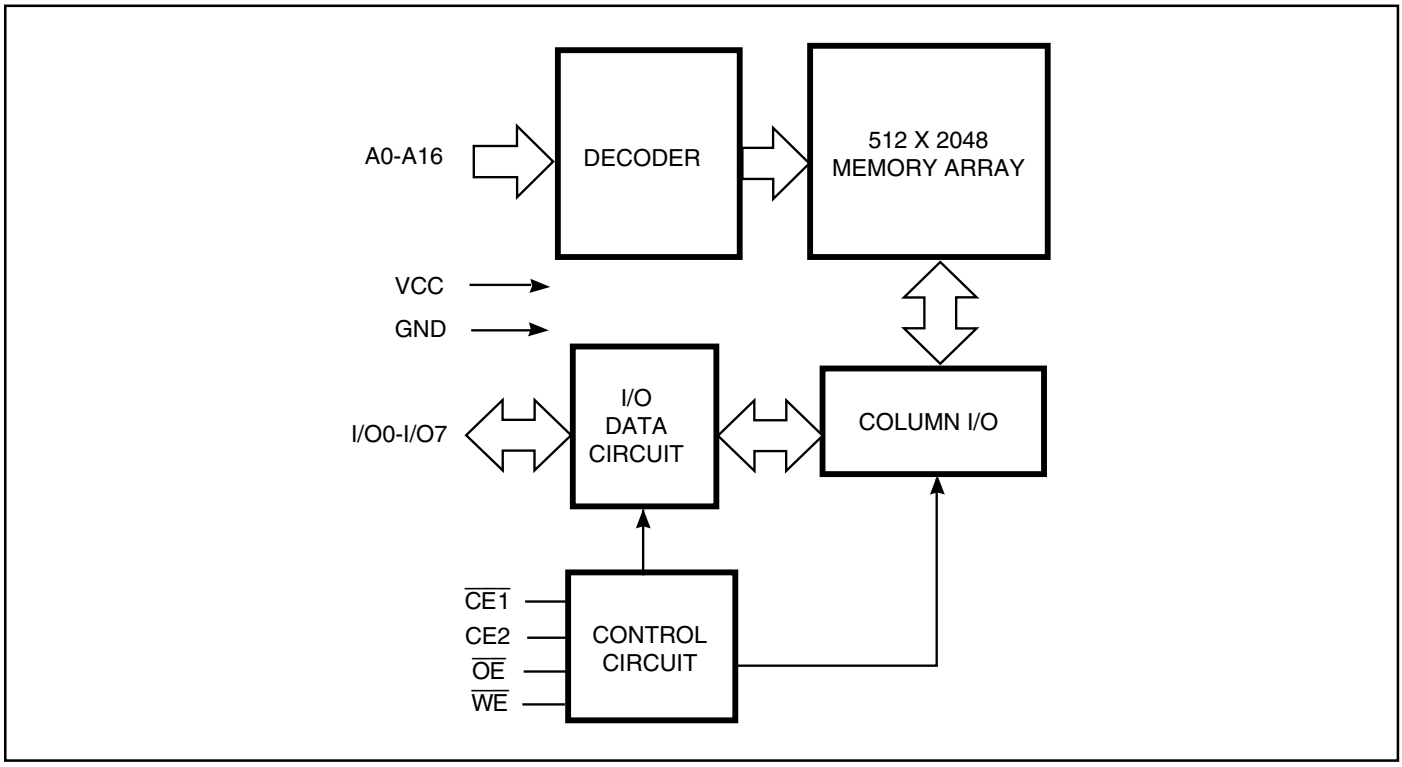
The *ISSI* IS62LV1024LL is a low power and low Vcc,131,072-word by 8-bit CMOS static RAM. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When $\overline{CE1}$ is HIGH or CE2 is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced by using CMOS input levels.

Easy memory expansion is provided by using two Chip Enable inputs, $\overline{CE1}$ and CE2. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

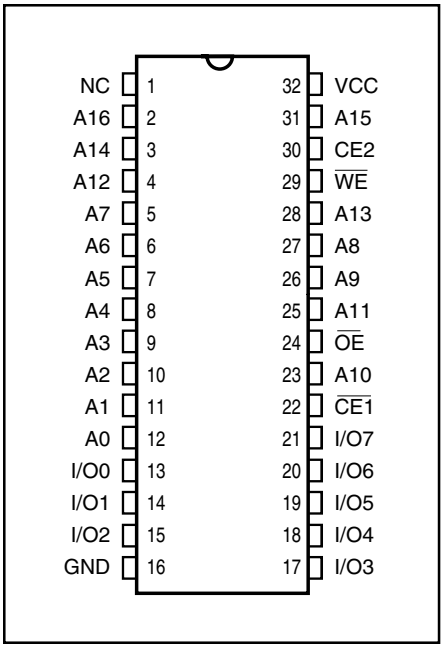
The IS62LV1024LL is available in 32-pin TSOP (Type I), STSOP (8 x 13.4mm), and 450-mil plastic SOP (525-mil pin to pin) packages.

FUNCTIONAL BLOCK DIAGRAM



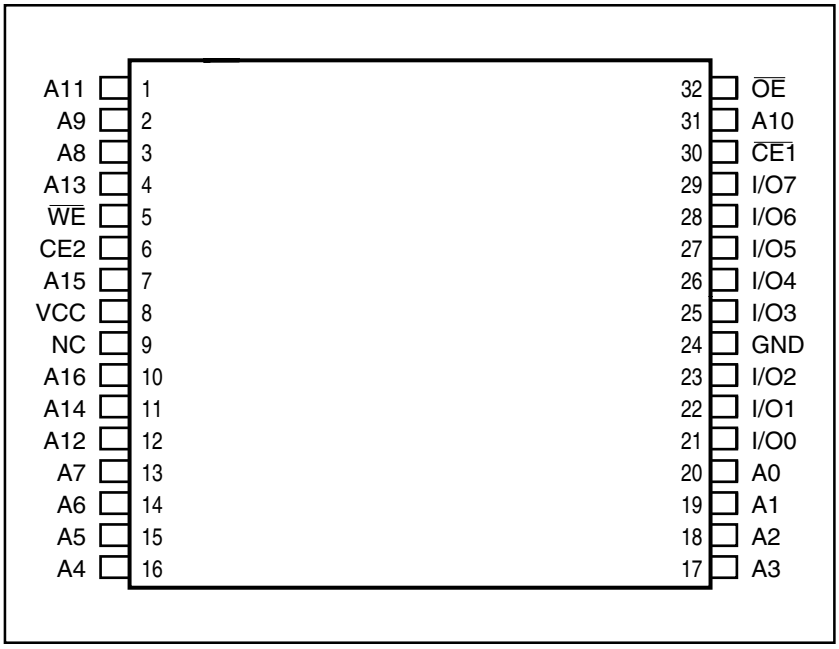
PIN CONFIGURATION

32-Pin SOP (Q)



PIN CONFIGURATION

32-Pin TSOP (Type I) (T) and STSOP (Type 1) (H)



PIN DESCRIPTIONS

A0-A16	Address Inputs
$\overline{CE1}$	Chip Enable 1 Input
CE2	Chip Enable 2 Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
NC	No Connection
Vcc	Power
GND	Ground

OPERATING RANGE

Range	Ambient Temperature	Speed	Vcc
Commercial	0°C to +70°C	-45 ns	2.85V to 3.15V
		-55 ns	2.5V to 3.3V
		-70 ns	2.5V to 3.3V
Industrial	–40°C to +85°C		2.5V to 3.3V

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE1}$	CE2	$\overline{OE}$	I/O Operation	Vcc Current
Not Selected	X	H	X	X	High-Z	I_{SB1}, I_{SB2}
(Power-down)	X	X	L	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	H	High-Z	I_{CC}
Read	H	L	H	L	D_{OUT}	I_{CC}
Write	L	L	H	X	D_{IN}	I_{CC}

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to Vcc + 0.5	V
V_{CC}	Vcc related to GND	–0.3 to +3.6	V
T_{BIAS}	Temperature Under Bias	–40 to +85	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	0.7	W

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, Vcc = 3.0V.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –1.0 mA	2.2	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.1 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + 0.2	V
V_{IL}	Input LOW Voltage[1]		–0.2	0.4	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}	–1	1	µA

Notes:
1. V_{IL} = –3.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

				-45		-55		-70		
Symbol	Parameter	Test Conditions		Min.	Max.	Min.	Max.	Min.	Max.	Unit
I_{CC}	Vcc Dynamic Operating Supply Current	V_{CC} = Max., $\overline{CE}$ = V_{IL} I_{OUT} = 0 mA, f = f_{MAX}	Com. Ind.	— —	35 40	— —	30 35	— —	25 30	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL}, $\overline{CE1}$ ≥ V_{IH} or CE2 ≤ V_{IL}, f = 0	Com. Ind.	— —	0.4 1	— —	0.4 1	— —	0.4 1	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., f = 0 $\overline{CE1}$ ≥ V_{CC} – 0.2V, CE2 ≤ 0.2V, or V_{IN} ≥ V_{CC} – 0.2V, V_{IN} ≤ 0.2V	Com. Ind.	— —	8 10	— —	8 10	— —	8 10	µA

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-45 Min.	-45 Max.	-55 Min.	-55 Max.	-70 Min.	-70 Max.	Unit
t_{RC}	Read Cycle Time	45	—	55	—	70	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	70	ns
t_{OHA}	Output Hold Time	10	—	10	—	10	—	ns
t_{ACE1}	$\overline{CE1}$ Access Time	—	45	—	55	—	70	ns
t_{ACE2}	CE2 Access Time	—	45	—	55	—	70	ns
t_{DOE}	$\overline{OE}$ Access Time	—	20	—	25	—	35	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	5	—	5	—	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	0	15	0	20	0	25	ns
t_{LZCE1}[2]	$\overline{CE1}$ to Low-Z Output	5	—	7	—	10	—	ns
t_{LZCE2}[2]	CE2 to Low-Z Output	5	—	7	—	10	—	ns
t_{HZCE}[2]	$\overline{CE1}$ or CE2 to High-Z Output	0	15	0	20	0	25	ns

Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.3V, input pulse levels of 0.4V to 2.2V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0.4V to 2.2V
Input Rise and Fall Times	5 ns
Input and Output Timing and Reference Level	1.3V
Output Load	See Figures 1 and 2

AC TEST LOADS

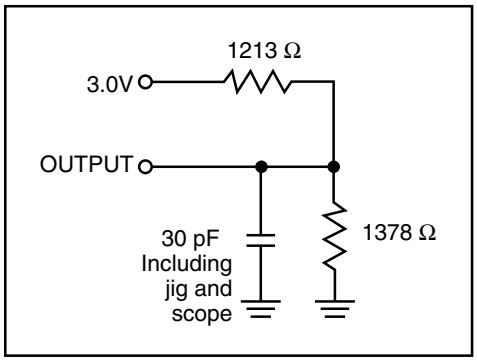


Figure 1.

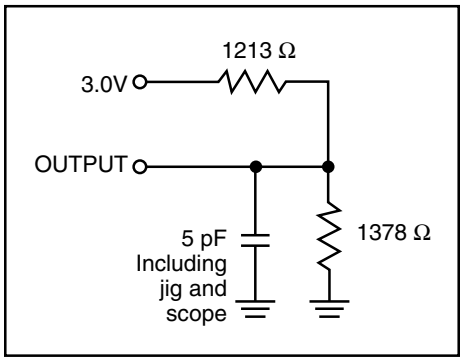
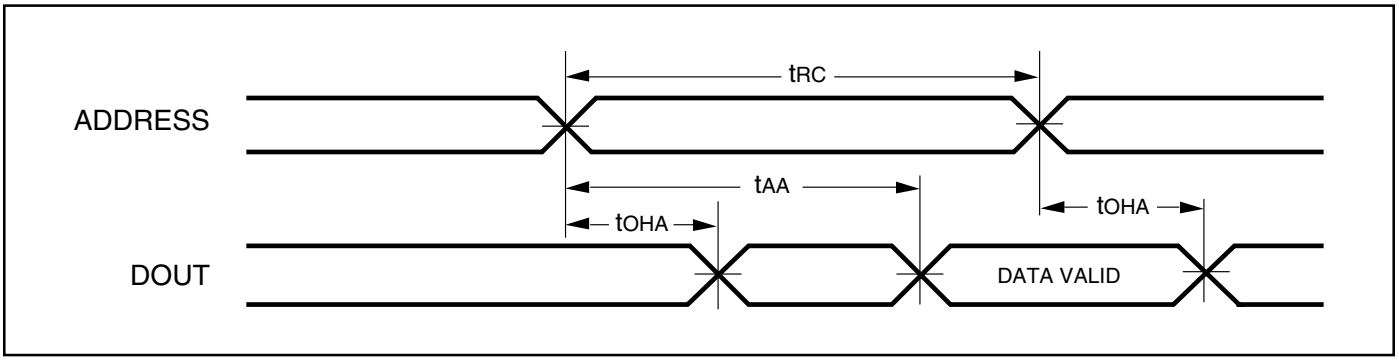


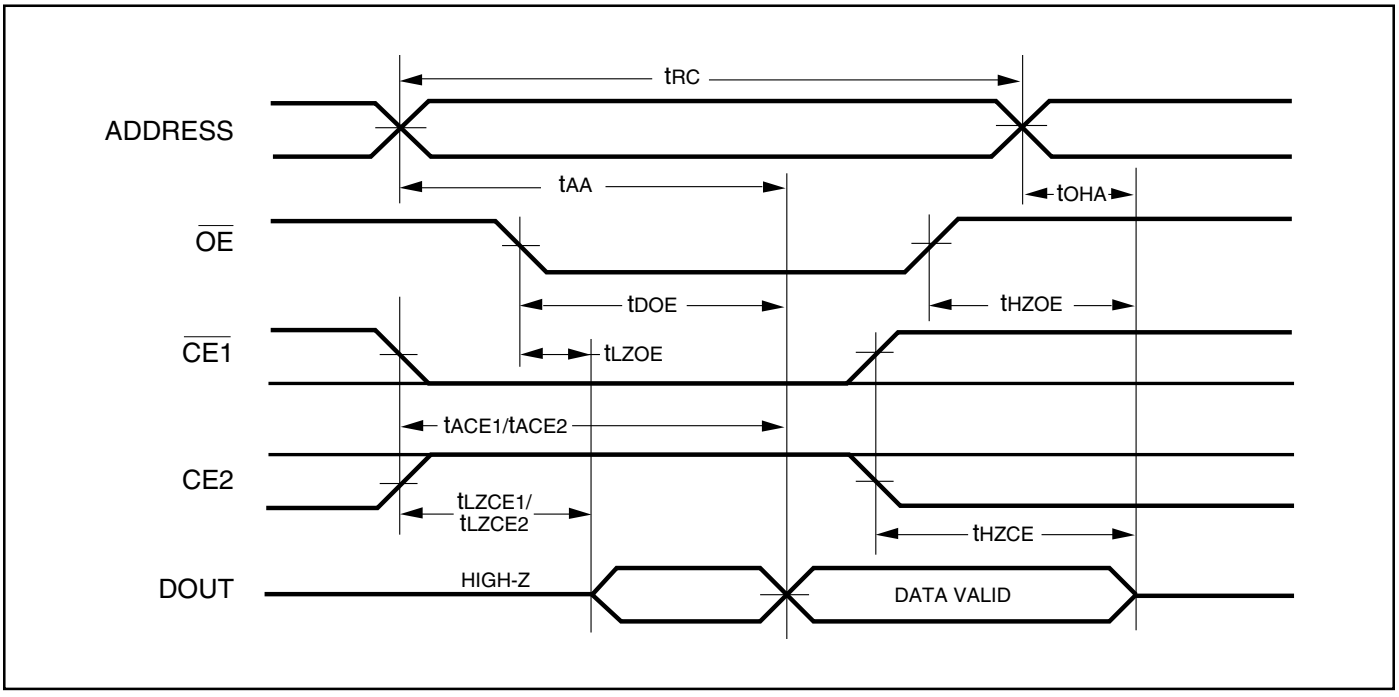
Figure 2.

AC WAVEFORMS

READ CYCLE NO. 1[1,2]



READ CYCLE NO. 2[1,3]



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE1}$ = V_{IL}, CE2 = V_{IH}.
3. Address is valid prior to or coincident with $\overline{CE1}$ LOW and CE2 HIGH transitions.

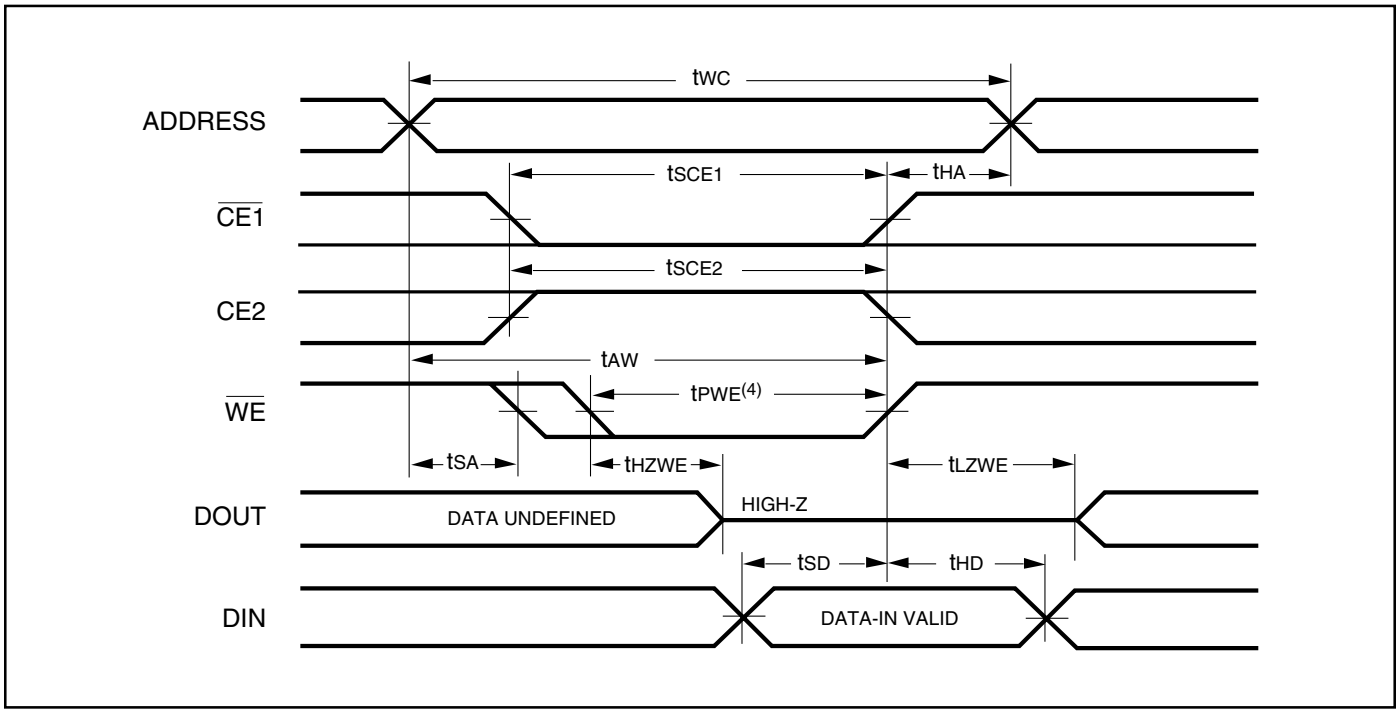
WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range, Standard and Low Power)

Symbol	Parameter	-45 Min.	-45 Max.	-55 Min.	-55 Max.	-70 Min.	-70 Max.	Unit
t_{WC}	Write Cycle Time	45	—	55	—	70	—	ns
t_{SCE1}	$\overline{CE1}$ to Write End	35	—	50	—	60	—	ns
t_{SCE2}	CE2 to Write End	35	—	50	—	60	—	ns
t_{AW}	Address Setup Time to Write End	35	—	50	—	60	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	ns
$t_{PWE1,2}$	$\overline{WE}$ Pulse Width	35	—	40	—	55	—	ns
t_{SD}	Data Setup to Write End	25	—	25	—	30	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	—	15	—	20	0	25	ns
t_{LZWE}[2]	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	5	—	ns

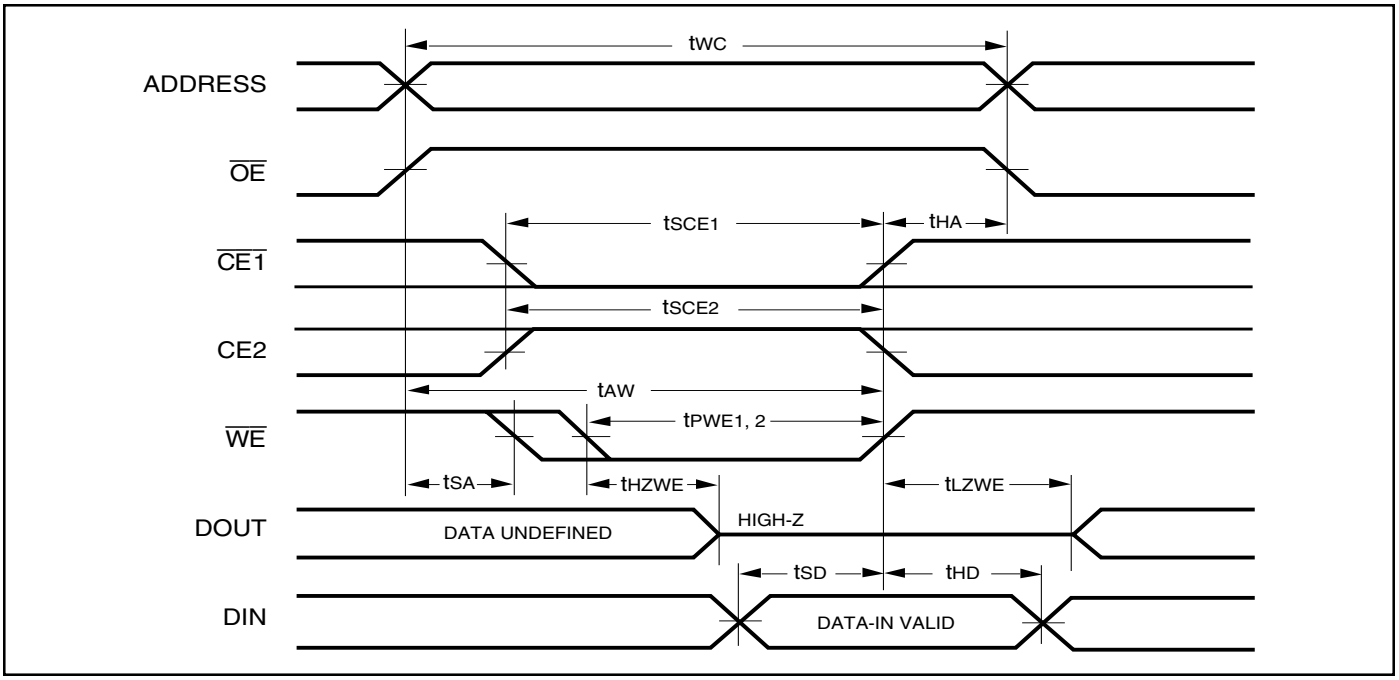
Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.3V, input pulse levels of 0.4V to 2.2V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE1}$ LOW, CE2 HIGH and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.

AC WAVEFORMS

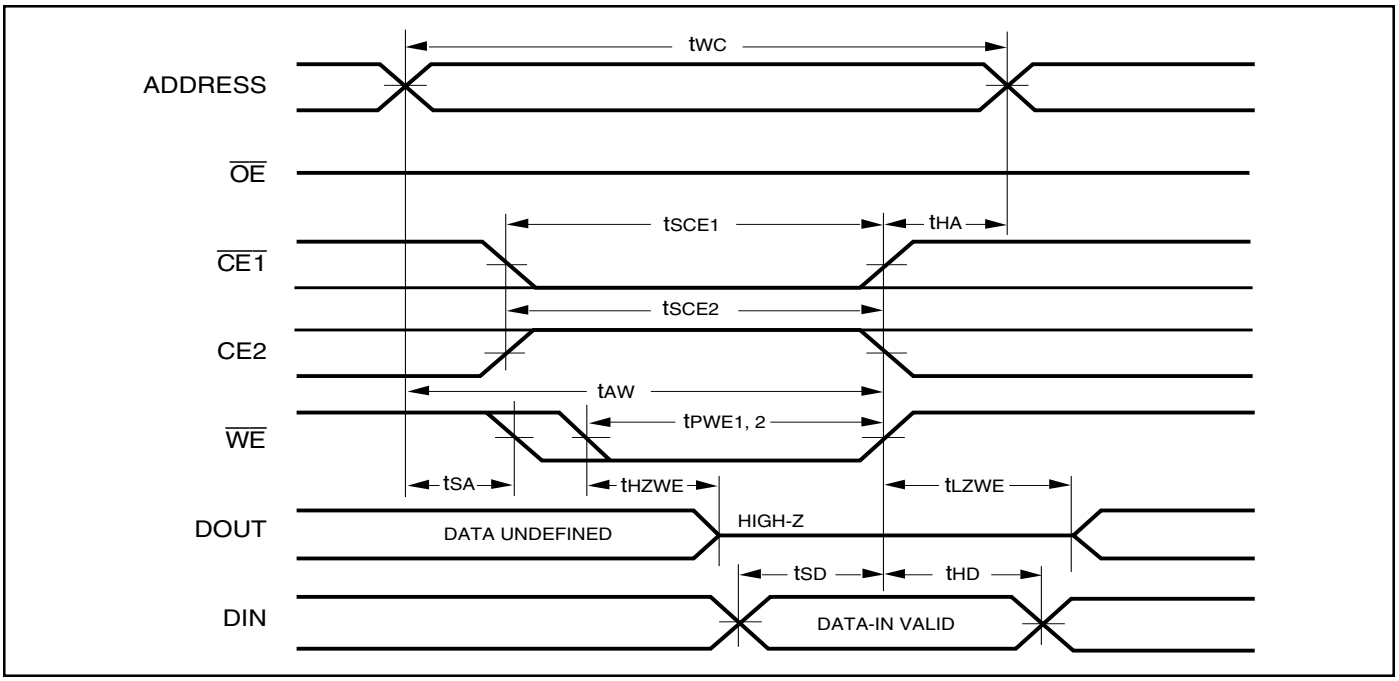
WRITE CYCLE NO. 1 ($\overline{CE1}$, CE2 Controlled, $\overline{OE}$ = HIGH or LOW)[1,2]



WRITE CYCLE NO. 2 ($\overline{WE}$, Controlled: $\overline{OE}$ is HIGH during Write Cycle)[1,2]



WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW during Write Cycle)[1,2]

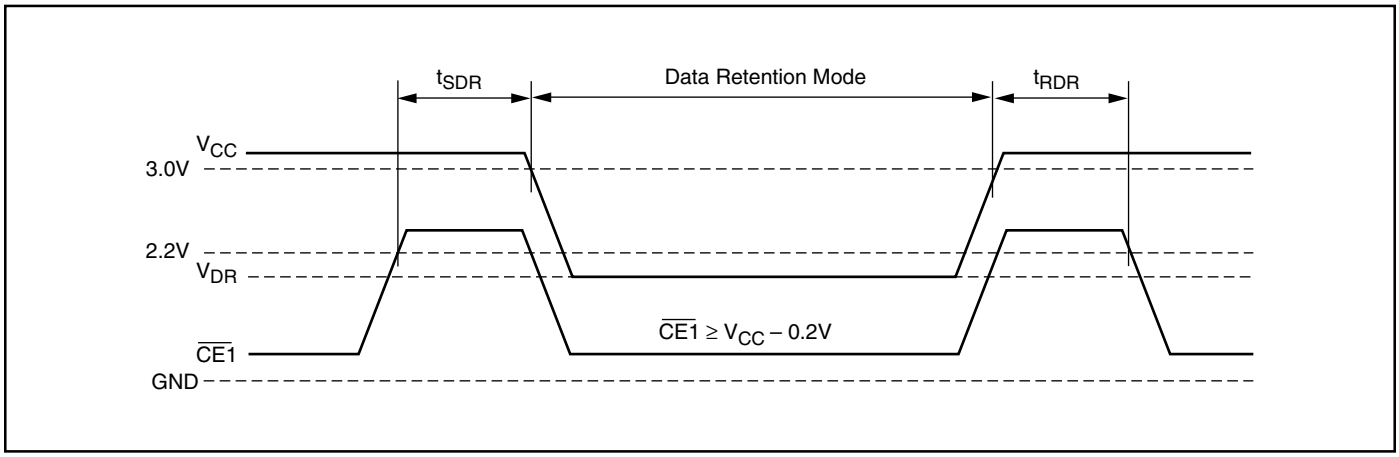


Notes:
1. The internal write time is defined by the overlap of $\overline{CE1}$ LOW, CE2 HIGH and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE}$ = V_{IH}.

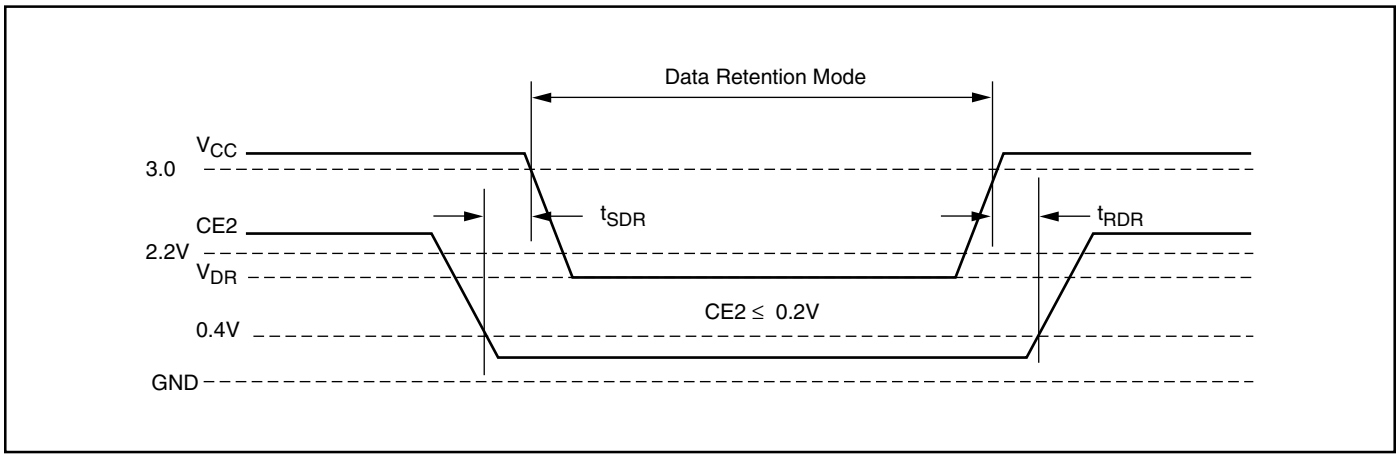
DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Min.	Max.	Unit
V_{DR}	Vcc for Data Retention	See Data Retention Waveform		2.0	3.3	V
I_{DR}	Data Retention Current	Vcc = 2.0V, $\overline{CE1} \geq$ Vcc – 0.2V	Com.	—	8	µA
			Ind.	—	10	µA
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}	—	ns

DATA RETENTION WAVEFORM ($\overline{CE1}$ Controlled)



DATA RETENTION WAVEFORM (CE2 Controlled)



ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
45	IS62LV1024LL-45Q	450-mil Plastic SOP
	IS62LV1024LL-45T	TSOP, Type I
	IS62LV1024LL-45H	STSOP, Type I
55	IS62LV1024LL-55Q	450-mil Plastic SOP
	IS62LV1024LL-55T	TSOP, Type I
	IS62LV1024LL-55H	STSOP, Type I
70	IS62LV1024LL-70Q	450-mil Plastic SOP
	IS62LV1024LL-70T	TSOP, Type I
	IS62LV1024LL-70H	STSOP, Type I

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
45	IS62LV1024LL-45QI	450-mil Plastic SOP
	IS62LV1024LL-45TI	TSOP, Type I
	IS62LV1024LL-45HI	STSOP, Type I
55	IS62LV1024LL-55QI	450-mil Plastic SOP
	IS62LV1024LL-55TI	TSOP, Type I
	IS62LV1024LL-55HI	STSOP, Type I
70	IS62LV1024LL-70QI	450-mil Plastic SOP
	IS62LV1024LL-70TI	TSOP, Type I
	IS62LV1024LL-70HI	STSOP, Type I

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